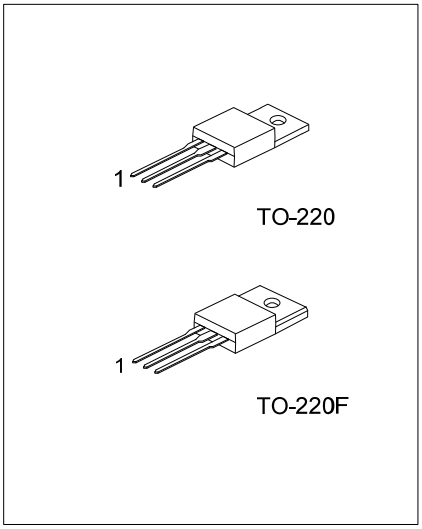
2.5 Amps, 800 Volts
N-CHANNEL POWER MOSFET



Lead-free: 3N80L
Halogen-free: 3N80G

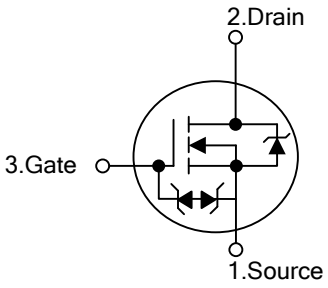
■ DESCRIPTION

The UTC **3N80** uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with low gate voltages. This device is suitable for use as a load switch or in PWM applications.

■ FEATURES

* $R_{DS(ON)}$=3.8Ω @V_{GS}=10 V
* Ultra low gate charge (typical 19 nC)
* Low reverse transfer capacitance (C_{RSS} = typical 11 pF)
* Fast switching capability
* Avalanche energy specified
* Improved dv/dt capability, high ruggedness

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number			Package	Pin Assignment			Packing
Normal	Lead Free	Halogen Free		1	2	3	
3N80-TA3-T	3N80L-TA3-T	3N80G-TA3-T	TO-220	G	D	S	Tube
3N80-TF3-T	3N80L-TF3-T	3N80G-TF3-T	TO-220F	G	D	S	Tube

3N80L-TA3-T (1)Packing Type (2)Package Type (3)Lead Plating	(1) T: Tube (2) TA3: TO-220, TF3: TO-22F (3) G: Halogen Free, L: Lead Free, Blank: Pb/Sn

■ ABSOLUTE MAXIMUM RATINGS (T_C=25℃, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage (V_{GS}=0V)		V_{DSS}	800	V
Drain-Gate Voltage (R_G=20kΩ)		V_{DGR}	800	V
Gate-Source Voltage		V_{GSS}	±30	V
Gate-Source Breakdown Voltage (I_{GS}=±1mA)		BV_{GSO}	30(MIN)	V
Gate Source ESD(HBM-C=100pF, R=1.5KΩ)		$V_{ESD(G-S)}$	2	V
Insulation Withstand Voltage (DC)	TO-220F	V_{ISO}	2500	V
Avalanche Current (Note 2)		I_{AR}	2.5	A
Continuous Drain Current		I_D	2.5	A
Pulsed Drain Current		I_{DM}	10	A
Single Pulse Avalanche Energy (Note 3)		E_{AS}	170	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.5	V/ns
Power Dissipation	TO-220	P_D	70	W
	TO-220F		25	
Junction Temperature		T_J	+150	℃
Storage Temperature		T_{STG}	-55 ~ +150	℃

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Pulse width limited by $T_{J(MAX)}$
3. starting T_J=25 °C, I_D=I_{AR}, V_{DD}=50V
4. I_{SD}≦2.5A, di/dt≦200A/μs, V_{DD}≦BV_{DSS}, T_J≦$T_{J(MAX)}$.

■ THERMAL DATA

PARAMETER		SYMBOL	RATING	UNIT
Junction-to-Ambient	TO-220	$θ_{JA}$	62.5	°C/W
	TO-220F		62.5	
Junction-to-Case	TO-220	$θ_{JC}$	1.78	°C/W
	TO-220F		5	

■ ELECTRICAL CHARACTERISTICS (T_C=25℃, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=1mA	800			V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=800V, V_{GS}=0 V			1	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0 V			±10	μA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=50μA	3	3.75	4.5	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=1.25A		3.8	4.5	Ω
Forward Transconductance (Note 1)	g_{FS}	V_{DS}=15V, I_D=1.25A		2.1		S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	V_{DS}=25V, V_{GS}=0V, f=1MHz		485		pF
Output Capacitance	C_{OSS}			57		pF
Reverse Transfer Capacitance	C_{RSS}			11		pF
Equivalent Output Capacitance (Note 2)	$C_{OSS(EQ)}$	V_{GS}=0V, V_{DS}=0V~640V		22		pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD}=400V, I_D=1.25 A, R_G=4.7Ω, V_{GS}=10 V		17		ns
Turn-On Rise Time	t_R			27		ns
Turn-Off Delay Time	$t_{D(OFF)}$			36		ns
Turn-Off Fall Time	t_F			40		ns
Total Gate Charge	Q_G	V_{DD}=640V, I_D=2.5A, V_{GS}=10V		19		nC
Gate-Source Charge	Q_{GS}			3.2		nC
Gate-Drain Charge	Q_{DD}			10.8		nC

■ ELECTRICAL CHARACTERISTICS(Cont.)

SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Diode Forward Voltage(Note 1)	V_{SD}	I_{SD}=2.5A ,V_{GS}=0V			1.6	V
Source-Drain Current	I_{SD}				2.5	A
Source-Drain Current (Pulsed)	I_{SDM}				10	A
Reverse Recovery Current	I_{RRM}	I_{SD}=2.5A, di/dt=100A/μs, V_{DD}=50V, T_J=25°C		8.4		A
Body Diode Reverse Recovery Time	t_{RR}			384		ns
Body Diode Reverse Recovery Charge	Q_{RR}			1600		nC

Note: 1.Pulse width=300μs, Duty cycle≦1.5%

2.$C_{OSS(EQ)}$ is defined asa constant equivalent capacitance giving the same charging time as C_{OSS} when V_{DS} increases from 0to 80% V_{DSS}.

■ TEST CIRCUITS AND WAVEFORMS

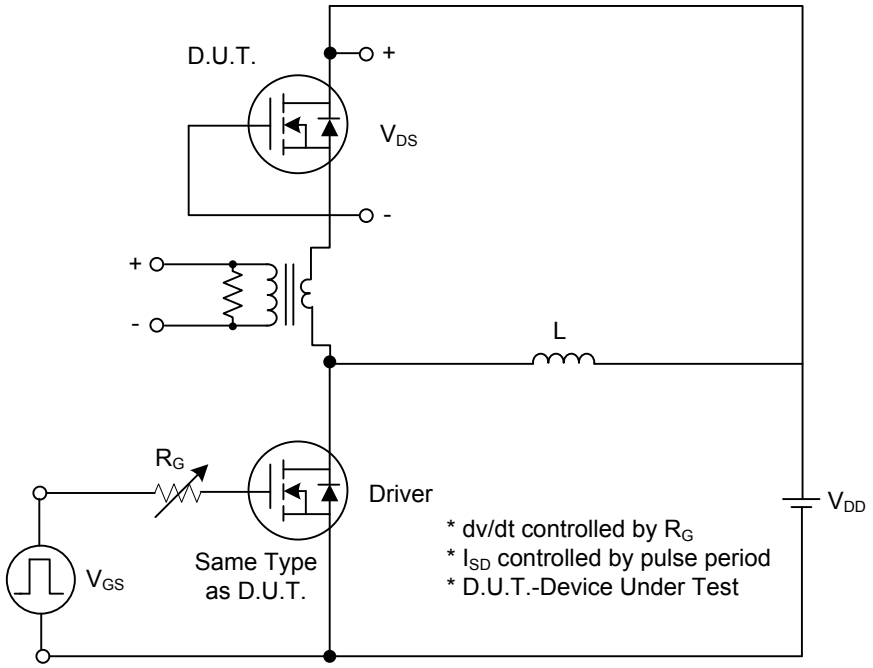


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

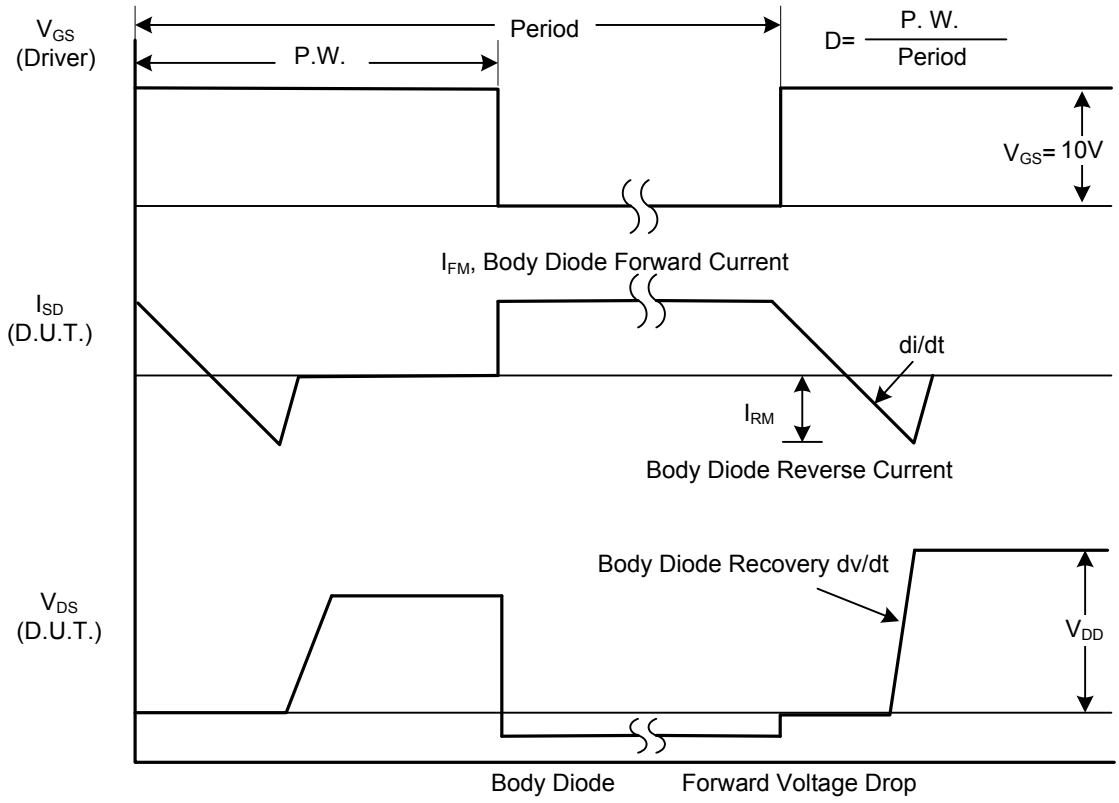


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

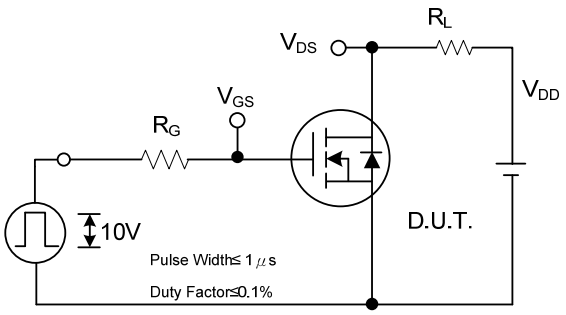


Fig. 2A Switching Test Circuit

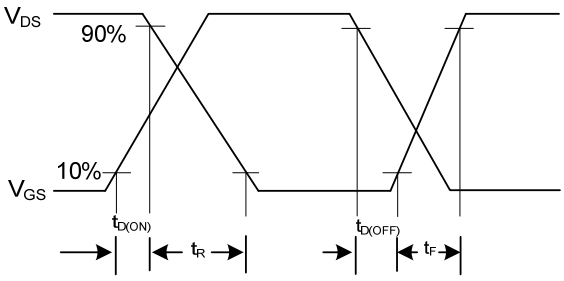


Fig. 2B Switching Waveforms

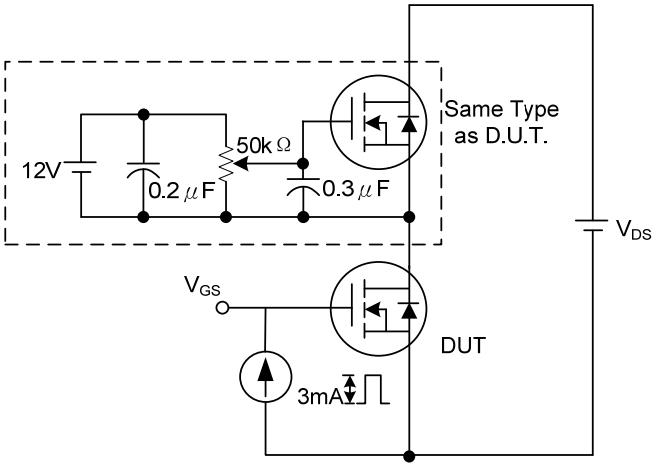


Fig. 3A Gate Charge Test Circuit

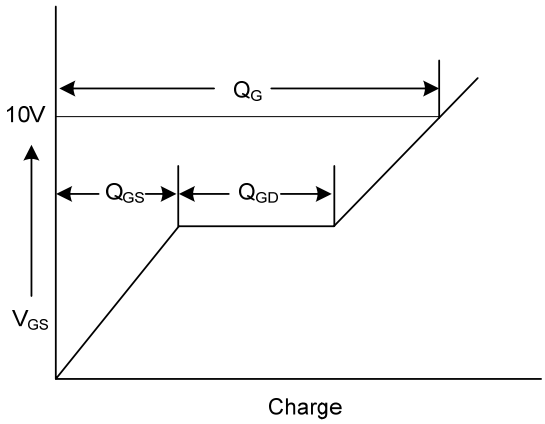


Fig. 3B Gate Charge Waveform

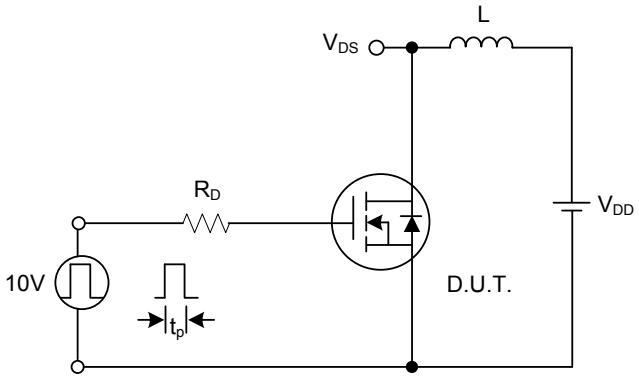


Fig. 4A Unclamped Inductive Switching Test Circuit

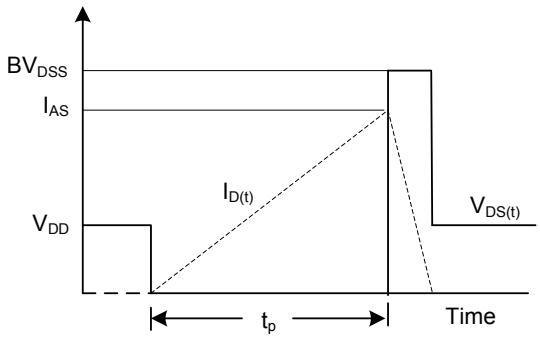


Fig. 4B Unclamped Inductive Switching Waveforms