

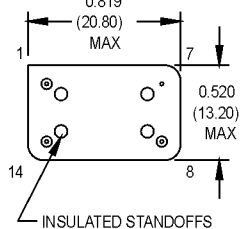
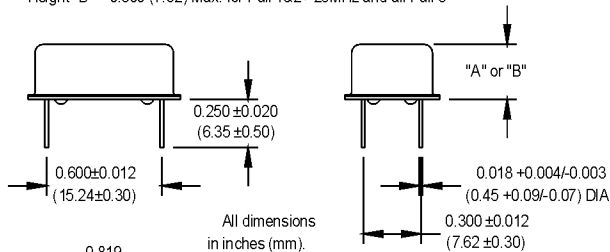
# MV Series

## 14 DIP, 5.0 Volt, HCMOS/TTL, VCXO

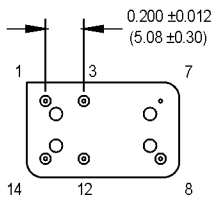


- General purpose VCXO for Phase Lock Loops (PLLs), Clock Recovery, Reference Signal Tracking, and Synthesizers
- Frequencies up to 160 MHz
- Tri-state Option Available

Height "A" = 0.200 (5.08) Max. for Pull 1&2 < 25 MHz  
 Height "B" = 0.300 (7.62) Max. for Pull 1&2 > 25MHz and all Pull 3



OPTIONAL 6-PIN PACKAGE WITH TRISTATE



### Pin Connections

| PIN | FUNCTION                   |
|-----|----------------------------|
| 1   | Control Voltage            |
| 3   | Tristate (6-Pin Pkg. Only) |
| 7   | Ground                     |
| 8   | Output                     |
| 12  | N/C (6-Pin Pkg. Only)      |
| 14  | +Vdd                       |

### Ordering Information

| Product Series | Temperature Range   | Stability   | Output Type                          | Pull Range (Vc = .5 to 4.5V)   | Symmetry/Logic Compatibility        | Package/Lead Configurations                          | RoHS Compliance   | Frequency (customer specified) |
|----------------|---|---|--------------------------------------|--|-------------------------------------|--|---|--------------------------------|
| MV             | 1: 0°C to +70°C<br>2: -40°C to +85°C<br>6: -20°C to +70°C | 1: ±1000 ppm<br>2: ±500 ppm<br>3: ±100 ppm<br>4: ±50 ppm<br>5: ±35 ppm<br>6: ±25 ppm<br>*8: ±20 ppm | V: Voltage Controlled<br>T: Tristate | 1: ±50 ppm min.<br>2: ±100 ppm min.<br>3: ±200 ppm min. ("B" package only) | A: 40/60 CMOS/TTL<br>C: 45/55 HCMOS | D: DIP; Nickel Header<br>G: Gull Wing; Nickel Header | Blank: non-RoHS compliant part<br>-R: RoHS compliant part | 00.0000 MHz                    |

\*Contact factory for availability

| PARAMETER             | Symbol                         | Min.   | Typ.                  | Max.                  | Units                  | Condition/Notes  |                     |
|-----------------------|--------------------------------|--|-----------------------|-----------------------|------------------------|--|---------------------|
| Frequency Range       | F                              | 1.5  |                       | 160                   | MHz                    | See Note 1   |                     |
| Operating Temperature | T <sub>A</sub>                 | (See Ordering Information)   |                       |                       |                        |  |                     |
| Storage Temperature   | T <sub>s</sub>                 | -55  |                       | 125                   | °C                     |  |                     |
| Frequency Stability   | ΔF/F                           | (See Ordering Information)   |                       |                       |                        |  |                     |
| Aging                 |                                |  |                       |                       |                        |  |                     |
| 1st Year              |                                | 0.6  |                       | 0.6                   | ppm                    | < 52 MHz / ≥ 52 MHz                                      |                     |
| Thereafter (per year) |                                | 0.5  |                       | 0.5                   | ppm                    | < 52 MHz / ≥ 52 MHz                                      |                     |
| Pullability/APR       |                                | (See Ordering Information)   |                       |                       |                        |  |                     |
| Control Voltage       | V <sub>c</sub>                 | 0.5  | 2.5                   | 4.5                   | V                      | Over control voltage                                     |                     |
| Linearity             |                                |  |                       | 10                    | %                      | Positive Monotonic Slope                                 |                     |
| Modulation Bandwidth  | f <sub>m</sub>                 | 10   |                       |                       | kHz                    |  |                     |
| Input Impedance       | Z <sub>in</sub>                | 50k  |                       |                       | Ohms                   |  |                     |
| Input Voltage         | V <sub>dd</sub>                | 4.75   | 5                     | 5.25                  | V                      |  |                     |
| Input Current         | I <sub>dd</sub>                |  | 25<br>35<br>55        | 40<br>60<br>90        | mA                     | 1.5 to 24.999 MHz<br>25 to 69.999 MHz<br>70 to 160 MHz   |                     |
| Output Type           |                                | HCMOS/TTL  |                       |                       |                        |  |                     |
| Load                  |                                | 10 TTL or 50 pF<br>5 TTL or 15 pF  |                       |                       |                        |  |                     |
| Symmetry (Duty Cycle) |                                | (See Ordering Information)   |                       |                       |                        |  |                     |
| Logic "1" Level       | V <sub>oh</sub>                | 90% V <sub>dd</sub>  |                       |                       | V                      | HCMOS load<br>TTL load                                   |                     |
| Logic "0" Level       | V <sub>ol</sub>                |  |                       | 10% V <sub>dd</sub>   | V                      | HCMOS load<br>TTL load                                   |                     |
| Rise/Fall Time        | T <sub>r</sub> /T <sub>f</sub> |  |                       | 6 / 10<br>1.5 / 5     | ns                     | See Note 4<br>TTL/HCMOS<br>TTL/HCMOS                     |                     |
| Tri-state Function    |                                | Input Logic "1" or floating: output active<br>Input Logic "0": output disables to high-Z |                       |                       |                        |  |                     |
| Start up Time         |                                |  | 5                     |                       | ms                     |  |                     |
| Phase Jitter          | φ <sub>J</sub>                 |  | 0.3<br>10             | 1<br>15               | ps RMS<br>ps RMS       | Integrated 12 kHz - 20 MHz<br>Integrated 12 kHz - 20 MHz |                     |
| Phase Noise (Typical) |                                | 10 Hz<br>-71<br>-62  | 100 Hz<br>-104<br>-93 | 1 kHz<br>-134<br>-113 | 10 kHz<br>-151<br>-115 | 100 kHz<br>-153<br>-114                                  | Offset from carrier |

1. Frequencies above 90 MHz utilize a PPL design. Fundamental and PLL designs are available for other frequencies. Contact factory.
2. TTL load – see load circuit diagram #1. HCMOS load – see load circuit diagram #2
3. Symmetry is measured at 1.4 V with TTL load, and at 50% with HCMOS load.
4. Rise/Fall times are measured between 0.5 V and 2.4 V for TTL load, and between 10% V<sub>dd</sub> and 90% V<sub>dd</sub> for HCMOS load.

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