High Efficiency USB Power Manager with Dual Buck and Buck-Boost DC/DCs

FEATURES

POWER MANAGER

- **High Efficiency Switching PowerPath™ Controller with Bat-Track™ Adaptive Output Control**
- **Programmable USB or Wall Current Limit (100mA/500mA/1A)**
- **Full Featured Li-Ion/Polymer Battery Charger**
- **Instant-On Operation with a Discharged Battery**
- 1.5A Maximum Charge Current
- Internal 180mΩ Ideal Diode Plus External Ideal Diode Controller Powers Load in Battery Mode
- Low No-Load I_Q when Powered from BAT (<30µA)

DC/DCs

- **Dual High Efficiency Buck DC/DCs (400mA/400mA I_{OUT})**
- **High Efficiency Buck-Boost DC/DC (1A I_{OUT})**
- **All Regulators Operate at 2.25MHz**
- Dynamic Voltage Scaling on Two Buck Outputs
- I^2C Control of Enables, Mode, Two V_{OUT} Settings
- ENALL Pin with Power-Up Sequence Control
- Low No-Load Quiescent Current: 20µA Each

APPLICATIONS

- HDD-Based MP3 Players, PDAs, GPS, PMPs
- Other USB-Based Handheld Products

DESCRIPTION

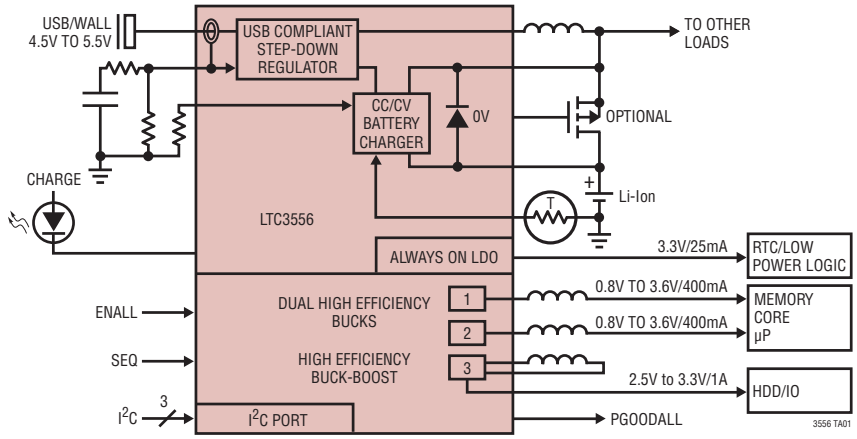
The LTC®3556 is a highly integrated power management and battery charger IC for Li-Ion/Polymer battery applications. It includes a high efficiency current limited switching PowerPath manager with automatic load prioritization, a battery charger, an ideal diode, and three synchronous switching regulators (two bucks and one buck-boost). Designed specifically for USB applications, the LTC3556's switching power manager automatically limits input current to a maximum of either 100mA or 500mA for USB applications or 1A for adapter-powered applications.

The LTC3556's switching input stage transmits nearly all of the 2.5W available from the USB port to the system load with minimal power wasted as heat. This feature allows the LTC3556 to provide more power to the application and eases the constraint of thermal budgeting in small spaces. The two buck regulators can provide up to 400mA each and the buck-boost can deliver 1A.

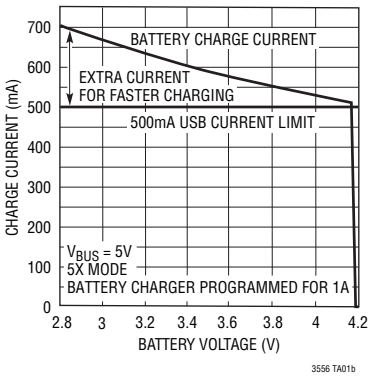
The LTC3556 is available in the low profile 28-pin (4mm × 5mm × 0.75mm) QFN surface mount package.

TYPICAL APPLICATION

High Efficiency PowerPath Manager, Dual Buck, Buck-Boost and LDO



Battery Charge Current vs Battery Voltage

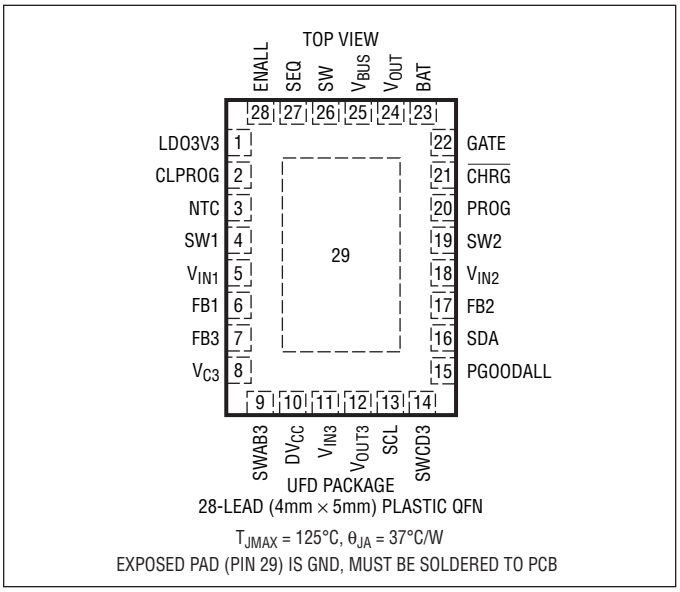


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{BUS} (Transient) t < 1ms, Duty Cycle < 1% .. –0.3V to 7V
V_{IN1}, V_{IN2}, V_{IN3}, V_{BUS} (Static), DV_{CC},
FB1, FB2, NTC, BAT, ENALL, SCL, SDA,
PGOODALL, $\overline{CHRG}$ ..... –0.3V to 6V
SEQ ..... –0.3V to Lesser of 6V or (V_{OUT} + 0.3V)
FB3, V_{C3} ..... –0.3V to Lesser of 6V or (V_{IN3} + 0.3V)
I_{CLPROG} 3mA
$I_{PGOODALL}$, $I_{\overline{CHRG}}$ 50mA
I_{PROG} 2mA
I_{LDO3V3} 30mA
I_{SW1}, I_{SW2} 600mA
I_{SW}, I_{BAT}, I_{VOUT} 2A
I_{SWAB3}, I_{SWCD3}, I_{VOUT3} 2.5A
Operating Temperature Range (Note 2) .... –40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3556EUFD#PBF	LTC3556EUFD#TRPBF	3556	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BUS} = 5V, V_{IN1} = V_{IN2} = V_{IN3} = V_{OUT3} = 3.8V, BAT = 3.8V, DV_{CC} = 3.3V, R_{PROG} = 1k, R_{CLPROG} = 3.01k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PowerPath Switching Regulator							
V_{BUS}	Input Supply Voltage			4.35		5.5	V
I_{BUSLIM}	Total Input Current	1x Mode, V_{OUT} = BAT	●	87	95	100	mA
		5x Mode, V_{OUT} = BAT	●	436	460	500	mA
		10x Mode, V_{OUT} = BAT	●	800	860	1000	mA
		Suspend Mode, V_{OUT} = BAT	●	0.31	0.38	0.50	mA
I_{VBUSQ}	V_{BUS} Quiescent Current	1x Mode, I_{OUT} = 0mA			7		mA
		5x Mode, I_{OUT} = 0mA			15		mA
		10x Mode, I_{OUT} = 0mA			15		mA
		Suspend Mode, I_{OUT} = 0mA			0.044		mA
h_{CLPROG} (Note 4)	Ratio of Measured V_{BUS} Current to CLPROG Program Current	1x Mode			224		mA/mA
		5x Mode			1133		mA/mA
		10x Mode			2140		mA/mA
		Suspend Mode			11.3		mA/mA

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{OUT(POWERPATH)}$	V_{OUT} Current Available Before Loading BAT	1x Mode, BAT = 3.3V 5x Mode, BAT = 3.3V 10x Mode, BAT = 3.3V Suspend Mode			135 672 1251 0.32		mA mA mA mA
V_{CLPROG}	CLPROG Servo Voltage in Current Limit	1x, 5x, 10x Modes Suspend Mode			1.188 100		V mV
V_{UVLO_VBUS}	V_{BUS} Undervoltage Lockout	Rising Threshold Falling Threshold		 3.95	4.30 4.00	4.35	V V
$V_{UVLO\_VBUS-BAT}$	V_{BUS} to BAT Differential Undervoltage Lockout	Rising Threshold Falling Threshold			200 50		mV mV
V_{OUT}	V_{OUT} Voltage	1x, 5x, 10x Modes, 0V < BAT < 4.2V, I_{OUT} = 0mA, Battery Charger Off		3.4	BAT + 0.3	4.7	V
		USB Suspend Mode, I_{OUT} = 250µA		4.5	4.6	4.7	V
f_{OSC}	Switching Frequency		●	1.8	2.25	2.7	MHz
$R_{PMOS\_POWERPATH}$	PMOS On-Resistance				0.18		Ω
$R_{NMOS\_POWERPATH}$	NMOS On-Resistance				0.30		Ω
$I_{PEAK\_POWERPATH}$	Peak Switch Current Limit	1x, 5x Modes 10x Mode			2 3		A A
Battery Charger							
V_{FLOAT}	BAT Regulated Output Voltage		 ●	4.179 4.165	4.200 4.200	4.221 4.235	V V
I_{CHG}	Constant Current Mode Charge Current	 R_{PROG} = 5k		980 185	1022 204	1065 223	mA mA
I_{BAT}	Battery Drain Current	V_{BUS} > V_{UVLO}, Battery Charger Off, I_{OUT} = 0µA V_{BUS} = 0V, I_{OUT} = 0µA (Ideal Diode Mode)		2	3.5 27	5 38	µA µA
V_{PROG}	PROG Pin Servo Voltage				1.000		V
V_{PROG_TRKL}	PROG Pin Servo Voltage in Trickle Charge	BAT < V_{TRKL}			0.100		V
$V_{C/10}$	C/10 Threshold Voltage at PROG				100		mV
h_{PROG}	Ratio of I_{BAT} to PROG Pin Current				1022		mA/mA
I_{TRKL}	Trickle Charge Current	BAT < V_{TRKL}			100		mA
V_{TRKL}	Trickle Charge Threshold Voltage	BAT Rising		2.7	2.85	3.0	V
ΔV_{TRKL}	Trickle Charge Hysteresis Voltage				135		mV
V_{RECHRG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{FLOAT}		–75	–100	–125	mV
t_{TERM}	Safety Timer Termination	Timer Starts When BAT = V_{FLOAT}		3.3	4	5	Hour
t_{BADBAT}	Bad Battery Termination Time	BAT < V_{TRKL}		0.42	0.5	0.63	Hour
$h_{C/10}$	End of Charge Indication Current Ratio	(Note 5)		0.088	0.1	0.112	mA/mA
$V_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Output Low Voltage	$I_{\overline{CHRG}}$ = 5mA			65	100	mV
$I_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Leakage Current	$V_{\overline{CHRG}}$ = 5V				1	µA
R_{ON_CHG}	Battery Charger Power FET On-Resistance (Between V_{OUT} and BAT)				0.18		Ω
T_{LIM}	Junction Temperature in Constant Temperature Mode				110		°C

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
NTC							
V_{COLD}	Cold Temperature Fault Threshold Voltage Hysteresis	Rising Threshold		75.0	76.5 1.5	78.0	$\%V_{BUS}$ $\%V_{BUS}$
V_{HOT}	Hot Temperature Fault Threshold Voltage Hysteresis	Falling Threshold		33.4	34.9 1.5	36.4	$\%V_{BUS}$ $\%V_{BUS}$
V_{DIS}	NTC Disable Threshold Voltage Hysteresis	Falling Threshold		0.7	1.7 50	2.7	$\%V_{BUS}$ mV
I_{NTC}	NTC Leakage Current	V_{NTC} = V_{BUS} = 5V		–50		50	nA
Ideal Diode							
V_{FWD}	Forward Voltage	V_{BUS} = 0V, I_{OUT} = 10mA I_{OUT} = 10mA			2 15		mV mV
$R_{DROPOUT}$	Internal Diode On-Resistance, Dropout	V_{BUS} = 0V			0.18		Ω
I_{MAX_DIODE}	Internal Diode Current Limit			1.6			A
Always On 3.3V Supply							
V_{LDO3V3}	Regulated Output Voltage	0mA < I_{LDO3V3} < 25mA		3.1	3.3	3.5	V
R_{CL_LDO3V3}	Closed-Loop Output Resistance				4		Ω
R_{OL_LDO3V3}	Dropout Output Resistance				23		Ω
Logic (ENALL, PGOODALL)							
V_{IL}	Logic Low Input Voltage	ENALL Pin				0.4	V
V_{IH}	Logic High Input Voltage	ENALL Pin		1.2			V
R_{PD}	Pull-Down Resistance	ENALL Pin			4.5		MΩ
V_{OL}	Logic Low Output Voltage	PGOODALL Pin, $I_{PULL-UP}$ = 5mA			0.07	0.2	V
I_{OH}	Logic High Leakage Current	PGOODALL Pin, $V_{PGOODALL}$ = 5V				1	µA
$t_{PGOODALL}$	PGOODALL Assertion Delay				230		ms
I^2C Port (Note 9)							
DV_{CC}	Input Supply Voltage			1.6		5.5	V
I_{DVCC}	DV_{CC} Current	SCL/SDA = 0kHz			0.3	1	µA
V_{DVCC_UVLO}	DV_{CC} UVLO				1.0		V
ADDRESS	I^2C Address				0001 001[0]		
V_{IH} SDA, SCL V_{IL} SDA, SCL	Input High Voltage Input Low Voltage			70		 30	$\%DV_{CC}$ $\%DV_{CC}$
I_{IH}, I_{IL} SDA, SCL	Input High/Low Current			–1	0	1	µA
V_{OL} SDA	SDA Output Low Voltage	I_{SDA} = 3mA				0.4	V
f_{SCL}	Clock Operating Frequency					400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition			1.3			µs
t_{HD_STA}	Hold Time After (Repeated) Start Condition			0.6			µs
t_{SU_STA}	Repeated Start Condition Setup Time			0.6			µs
t_{SU_STO}	Stop Condition Setup Time			0.6			µs
$t_{HD\_DAT(O)}$	Data Hold Time Output			0		900	ns

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{HD\_DAT(I)}$	Data Hold Time Input			0			ns
t_{SU_DAT}	Data Setup Time			100			ns
t_{LOW}	SCL Clock Low Period			1.3			µs
t_{HIGH}	SCL Clock High Period			0.6			µs
t_f	Clock/Data Fall Time	C_B = Capacitance of One BUS Line (pF)		20 + 0.1C_B		300	ns
t_r	Clock/Data Rise Time	C_B = Capacitance of One BUS Line (pF)		20 + 0.1C_B		300	ns
t_{SP}	Input Spike Suppression Pulse Width					50	ns
Switching Regulators 1, 2 and 3							
$V_{IN1,2,3}$	Input Supply Voltage			2.7		5.5	V
$V_{OUTUVLO}$	V_{OUT} UVLO—V_{OUT} Falling V_{OUT} UVLO—V_{OUT} Rising	$V_{IN1,2,3}$ Connected to V_{OUT} Through Low Impedance. Switching Regulators are Disabled in UVLO		2.5	2.6 2.8	 2.9	V V
f_{OSC}	Oscillator Frequency		●	1.8	2.25	2.7	MHz
Switching Regulator 1 (Buck)							
I_{VIN1}	Pulse Skip Mode Input Current Burst Mode® Input Current Forced Burst Mode Input Current LDO Mode Input Current Shutdown Input Current	I_{OUT1} = 0µA (Note 6) I_{OUT1} = 0µA (Note 6) I_{OUT1} = 0µA (Note 6) I_{OUT1} = 0µA (Note 6) I_{OUT1} = 0µA, FB1 = 0V			225 35 20 20	400 60 35 35 1	µA µA µA µA µA
I_{LIM1}	PMOS Switch Current Limit	Pulse Skip/Burst Mode Operation		600	800	1100	mA
I_{OUT1}	Available Output Current	Pulse Skip/Burst Mode Operation (Note 9) Forced Burst Mode Operation (Note 9) LDO Mode (Note 9)		400 60 50			mA mA mA
$V_{FBHIGH1}$	Maximum Servo Voltage	Full Scale (1, 1, 1, 1) (Note 7)	●	0.780	0.800	0.820	V
V_{FBLOW1}	Minimum Servo Voltage	Zero Scale (0, 0, 0, 0) (Note 7)	●	0.405	0.425	0.445	V
V_{LSB1}	V_{FB1} Servo Voltage Step Size				25		mV
R_{P1}	PMOS $R_{DS(ON)}$				0.6		Ω
R_{N1}	NMOS $R_{DS(ON)}$				0.7		Ω
R_{LDO_CL1}	LDO Mode Closed-Loop R_{OUT}				0.25		Ω
R_{LDO_OL1}	LDO Mode Open-Loop R_{OUT}	(Note 8)			2.5		Ω
I_{FB1}	FB1 Input Current	V_{FB1} = 0.85V		–50		50	nA
D1	Maximum Duty Cycle		●	100			%
R_{SW1}	SW1 Pull-Down in Shutdown				10		kΩ
Switching Regulator 2 (Buck)							
I_{VIN2}	Pulse Skip Mode Input Current Burst Mode Input Current Forced Burst Mode Input Current LDO Mode Input Current Shutdown Input Current	I_{OUT2} = 0µA (Note 6) I_{OUT2} = 0µA (Note 6) I_{OUT2} = 0µA (Note 6) I_{OUT2} = 0µA (Note 6) I_{OUT2} = 0µA, FB2 = 0V				225 35 20 20	400 60 35 35 1	µA µA µA µA µA
I_{LIM2}	PMOS Switch Current Limit	Pulse Skip/Burst Mode Operation		600	800	1100	mA
I_{OUT2}	Available Output Current	Pulse Skip/Burst Mode Operation (Note 9) Forced Burst Mode Operation (Note 9) LDO Mode (Note 9)		400 60 50			mA mA mA

Burst Mode is a registered trademark of Linear Technology Corporation.

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{FB2}	V_{FB2} Servo Voltage	(Note 7)	●	0.780	0.800	0.820	V
R_{P2}	PMOS $R_{DS(ON)}$				0.6		Ω
R_{N2}	NMOS $R_{DS(ON)}$				0.7		Ω
R_{LDO_CL2}	LDO Mode Closed-Loop R_{OUT}				0.25		Ω
R_{LDO_OL2}	LDO Mode Open-Loop R_{OUT}	(Note 8)			2.5		Ω
I_{FB2}	FB2 Input Current	V_{FB2} = 0.85V		–50		50	nA
D2	Maximum Duty Cycle		●	100			%
R_{SW2}	SW2 Pull-Down in Shutdown				10		kΩ
Switching Regulator 3 (Buck-Boost)							
I_{VIN3}	Input Current	PWM Mode, I_{OUT3} = 0µA Burst Mode Operation, I_{OUT3} = 0µA Shutdown			220 13 0	400 20 1	µA µA µA
$V_{OUT3(LOW)}$	Minimum Regulated Output Voltage	For Burst Mode Operation or Synchronous PWM Operation			2.65	2.75	V
$V_{OUT3(HIGH)}$	Maximum Regulated Output Voltage			5.50	5.60		V
I_{LIMF3}	Forward Current Limit (Switch A)	PWM Mode	●	2	2.5	3	A
$I_{PEAK3(BURST)}$	Forward Burst Current Limit (Switch A)	Burst Mode Operation	●	200	275	350	mA
$I_{ZERO3(BURST)}$	Reverse Burst Current Limit (Switch D)	Burst Mode Operation	●	–30	0	30	mA
$I_{MAX3(BURST)}$	Maximum Deliverable Output Current in Burst Mode Operation	2.7V ≤ V_{IN3} ≤ 5.5V, 2.75V ≤ V_{OUT3} ≤ 5.5V (Note 9)		50			mA
$V_{FBHIGH3}$	Maximum Servo Voltage	Full Scale (1, 1, 1, 1)	●	0.780	0.800	0.820	V
V_{FBLOW3}	Minimum Servo Voltage	Zero Scale (0, 0, 0, 0)	●	0.405	0.425	0.445	V
V_{LSB3}	V_{FB3} Servo Voltage Step Size				25		mV
I_{FB3}	FB3 Input Current	V_{FB3} = 0.8V		–50		50	nA
$R_{DS(ON)P}$	PMOS $R_{DS(ON)}$	Switches A, D			0.22		Ω
$R_{DS(ON)N}$	NMOS $R_{DS(ON)}$	Switches B, C			0.17		Ω
$I_{LEAK(P)}$	PMOS Switch Leakage	Switches A, D		–1		1	µA
$I_{LEAK(N)}$	NMOS Switch Leakage	Switches B, C		–1		1	µA
R_{VOUT3}	V_{OUT3} Pull-Down in Shutdown				10		kΩ
$D_{BUCK(MAX)}$	Maximum Buck Duty Cycle	PWM Mode	●	100			%
$D_{BOOST(MAX)}$	Maximum Boost Duty Cycle	PWM Mode			75		%
t_{SS3}	Soft-Start Time				0.5		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3556E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: The LTC3556E includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Total input current is the sum of quiescent current, I_{VBUSQ}, and measured current given by:

$V_{CLPROG}/R_{CLPROG} \bullet (h_{CLPROG} + 1)$

Note 5: $h_{C/10}$ is expressed as a fraction of measured full charge current with indicated PROG resistor.

Note 6: FBx above regulation such that regulator is in sleep. Specification does not include resistive divider current reflected back to V_{INx}.

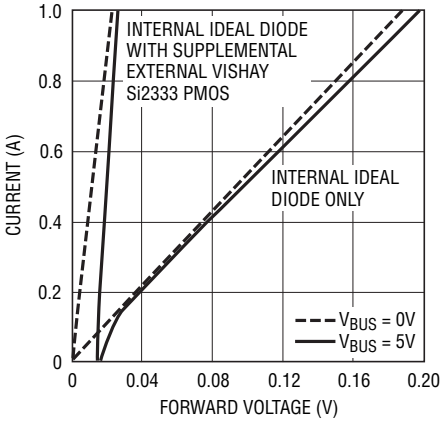
Note 7: Applies to Pulse Skip, Burst Mode operation and Forced Burst Mode operation only.

Note 8: Inductor series resistance adds to open-loop R_{OUT}.

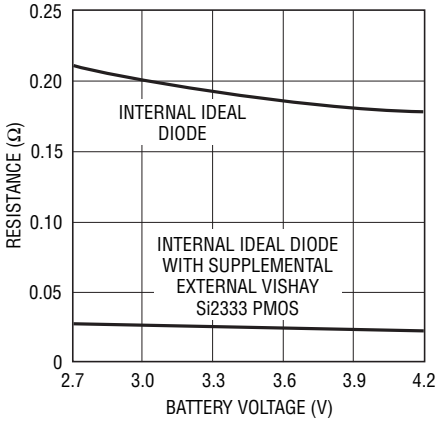
Note 9: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

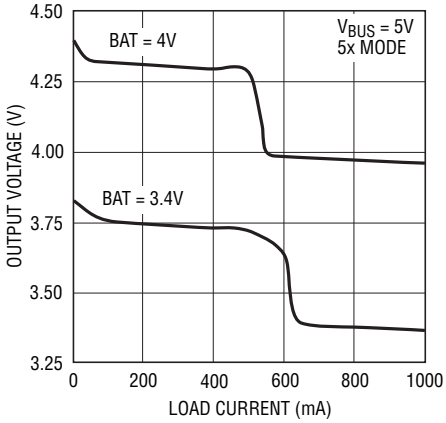
Ideal Diode V-I Characteristics



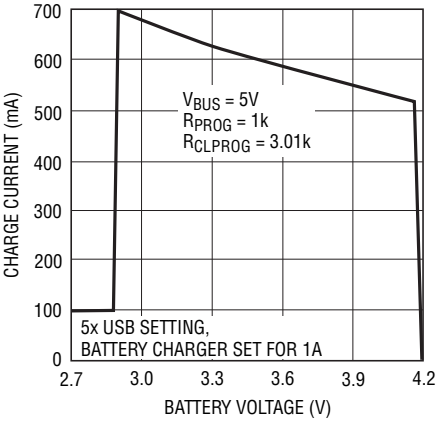
Ideal Diode Resistance vs Battery Voltage



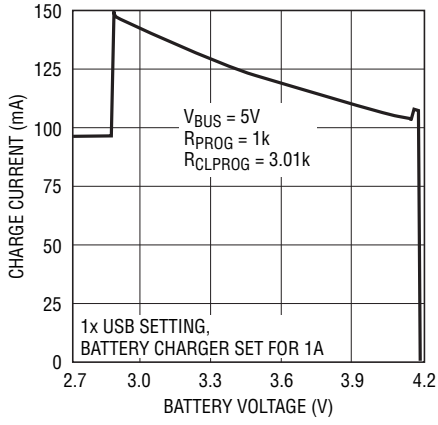
Output Voltage vs Load Current (Battery Charger Disabled)



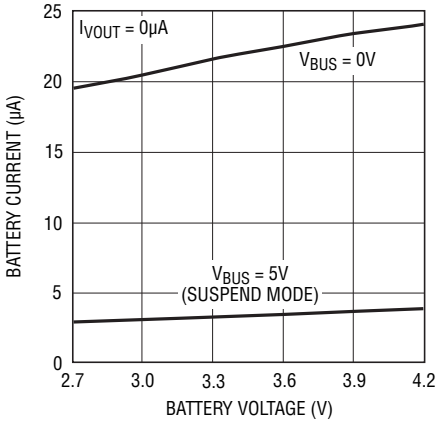
USB Limited Battery Charge Current vs Battery Voltage



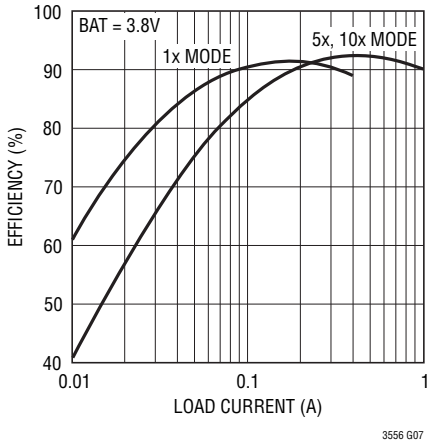
USB Limited Battery Charge Current vs Battery Voltage



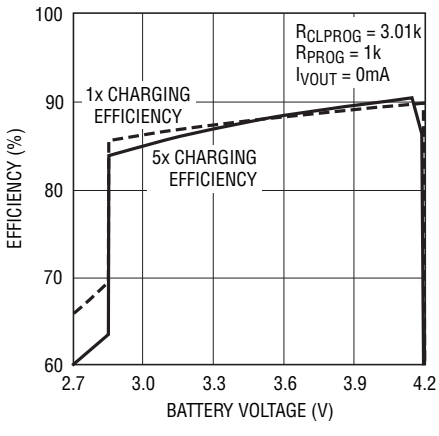
Battery Drain Current vs Battery Voltage



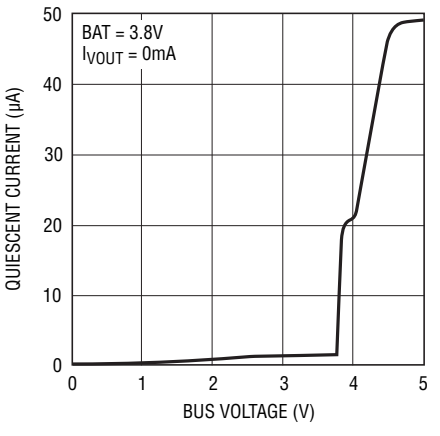
PowerPath Switching Regulator Efficiency vs Load Current



Battery Charging Efficiency vs Battery Voltage with No External Load (P_{BAT}/P_{BUS})

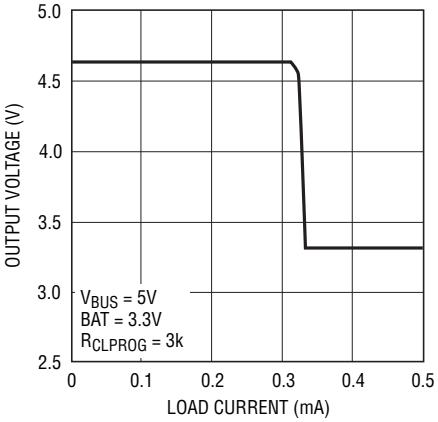


V_{BUS} Current vs V_{BUS} Voltage (Suspend)



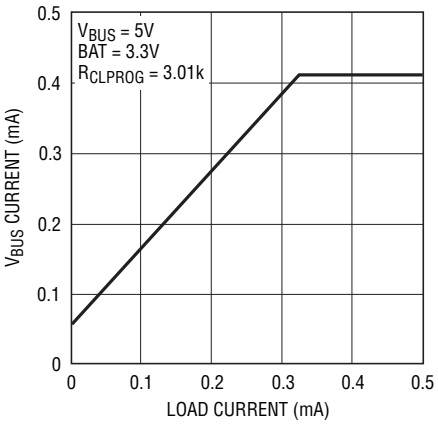
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage vs Load Current in Suspend



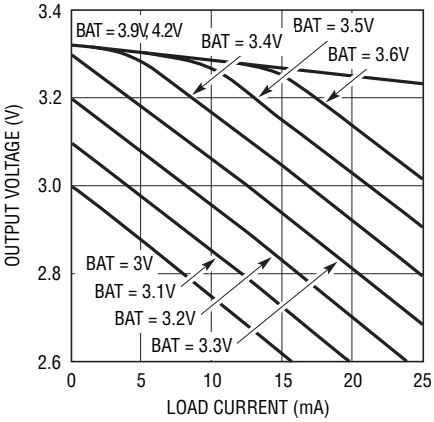
3556 G10

V_{BUS} Current vs Load Current in Suspend



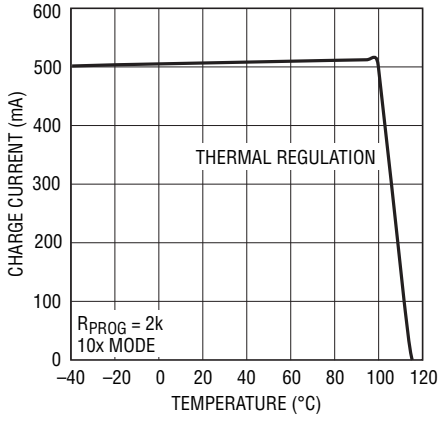
3556 G11

3.3V LDO Output Voltage vs Load Current, V_{BUS} = 0V



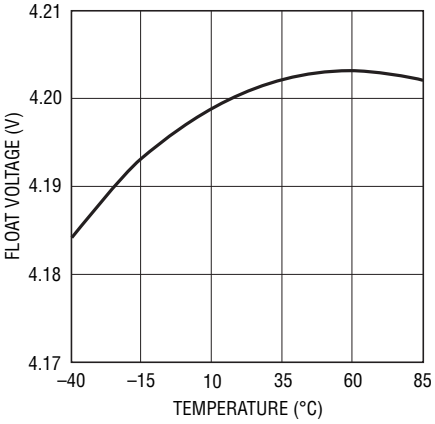
3556 G12

Battery Charge Current vs Temperature



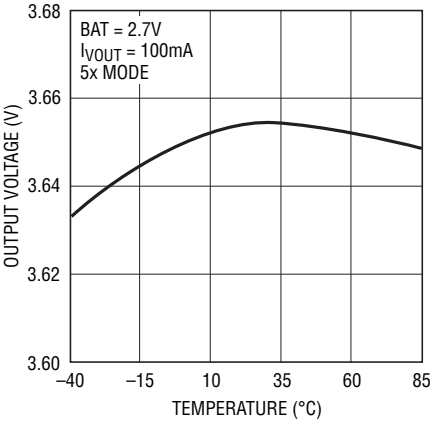
3556 G13

Battery Charger Float Voltage vs Temperature



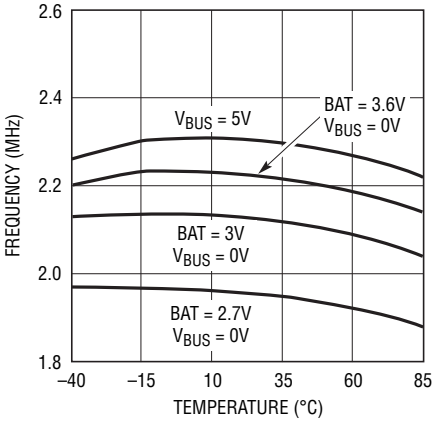
3556 G14

Low-Battery (Instant On) Output Voltage vs Temperature



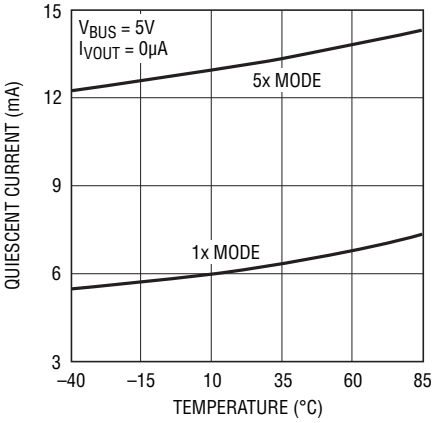
3556 G15

Oscillator Frequency vs Temperature



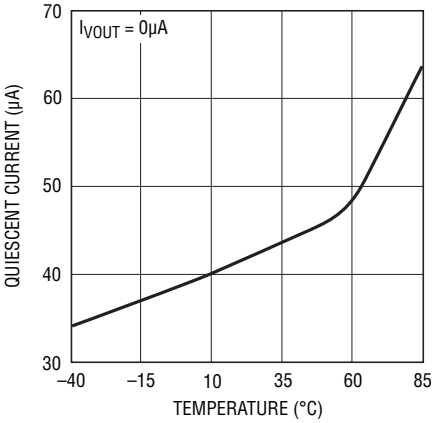
3556 G16

V_{BUS} Quiescent Current vs Temperature



3556 G17

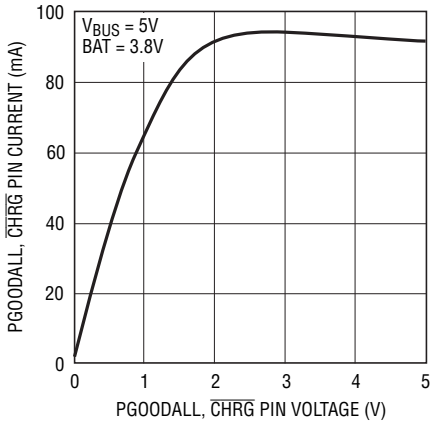
V_{BUS} Quiescent Current in Suspend vs Temperature



3556 G18

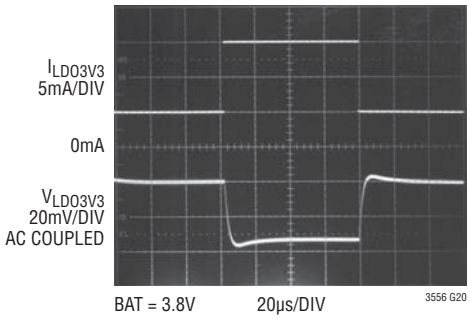
TYPICAL PERFORMANCE CHARACTERISTICS

PGOODALL, $\overline{CHRG}$ Pin Current vs Voltage (Pull-Down State)



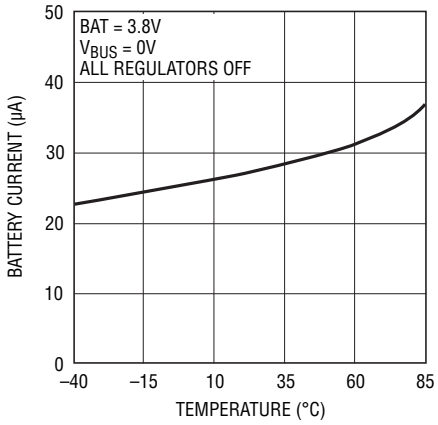
3556 G19

3.3V LDO Step Response (5mA to 15mA)



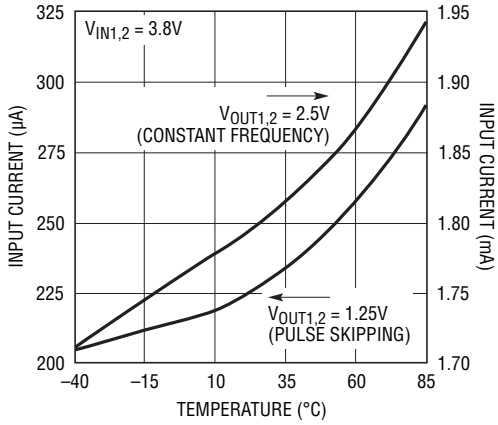
3556 G20

Battery Drain Current vs Temperature



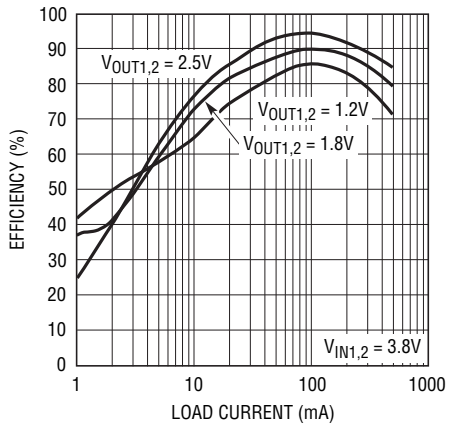
3556 G21

Switching Regulators 1, 2 Pulse Skip Mode Quiescent Currents



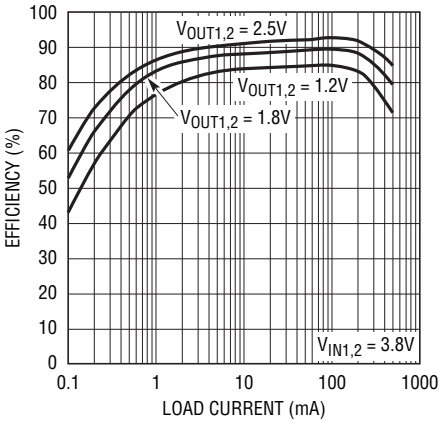
3556 G22

Switching Regulators 1, 2 Pulse Skip Mode Efficiency



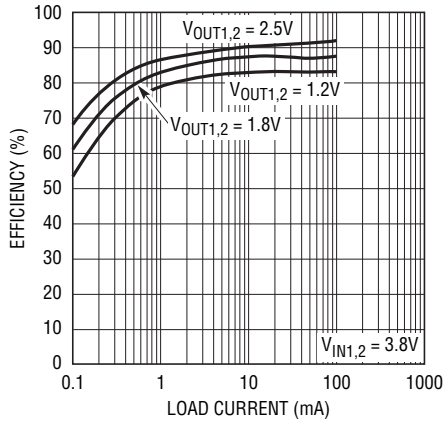
3556 G23

Switching Regulators 1, 2 Burst Mode Efficiency



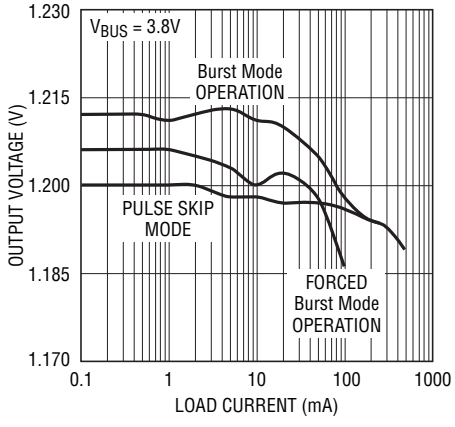
3556 G24

Switching Regulators 1, 2 Forced Burst Mode Efficiency



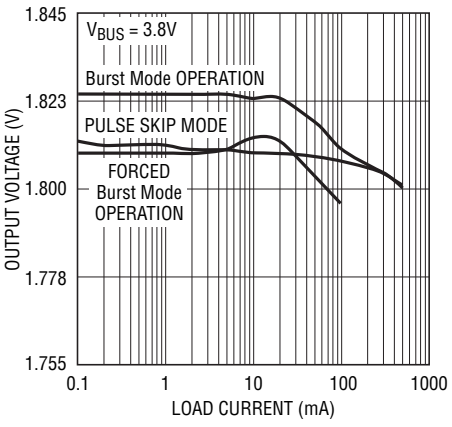
3556 G25

Switching Regulators 1, 2 Load Regulation at $V_{OUT1,2}$ = 1.2V



3556 G26

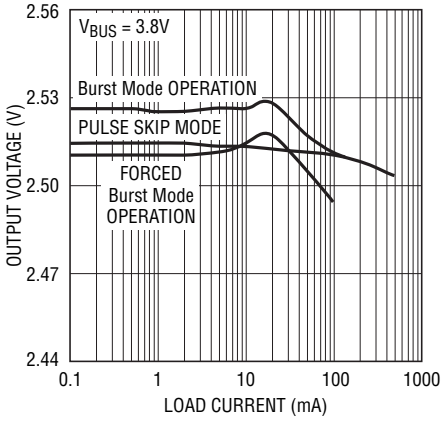
Switching Regulators 1, 2 Load Regulation at $V_{OUT1,2}$ = 1.8V



3556 G27

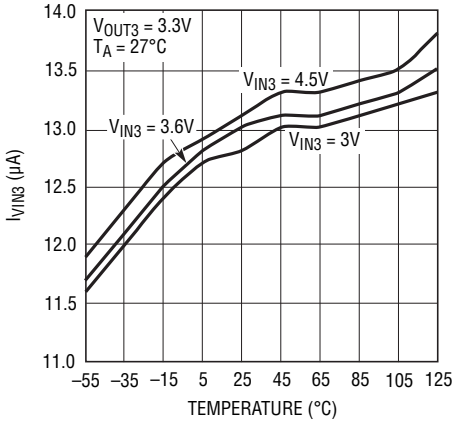
TYPICAL PERFORMANCE CHARACTERISTICS

Switching Regulators 1, 2 Load Regulation at $V_{OUT1,2}$ = 2.5V



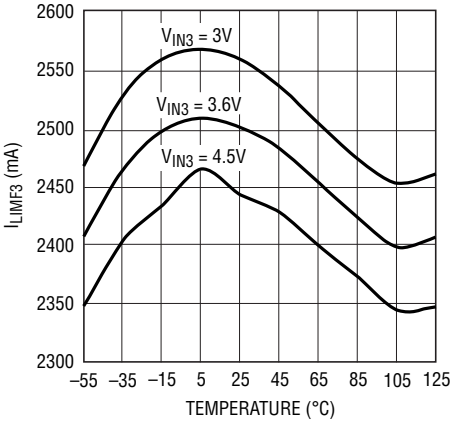
3556 G28

Switching Regulator 3 Burst Mode Operation Input Quiescent Current



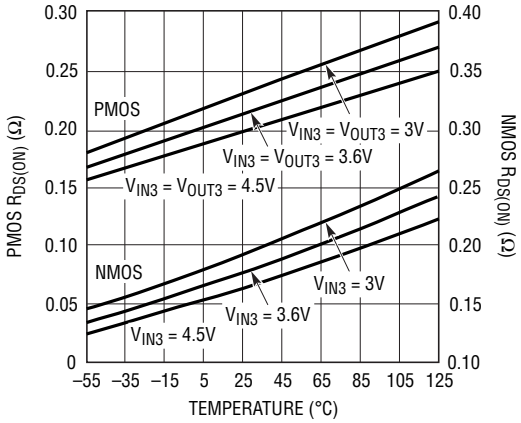
3556 G29

Switching Regulator 3 Forward Current Limit vs Temperature



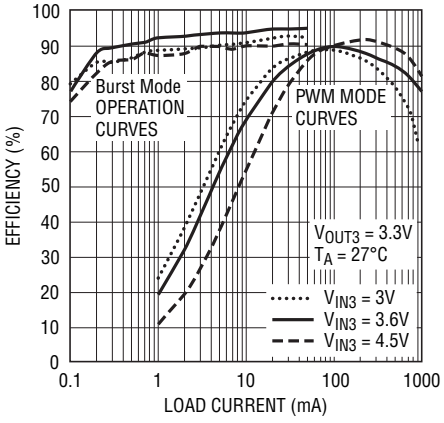
3556 G30

$R_{DS(ON)}$'s for Switching Regulator 3 vs Temperature



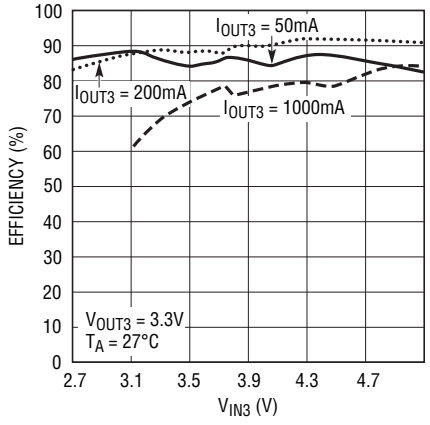
3556 G31

Switching Regulator 3 Efficiency vs Load Current



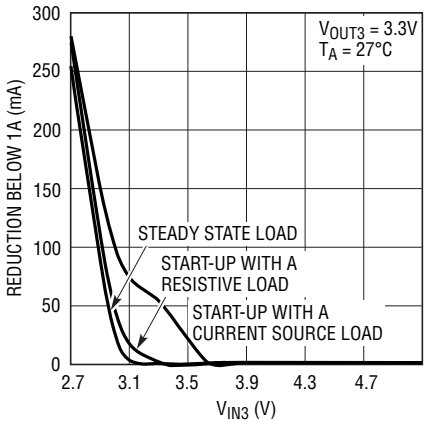
3556 G32

Switching Regulator 3 PWM Mode Efficiency vs Input Voltage



3556 G33

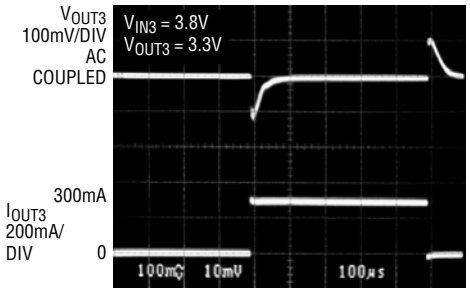
Switching Regulator 3 Reduction in Current Deliverability at Low V_{IN3}



3556 G34

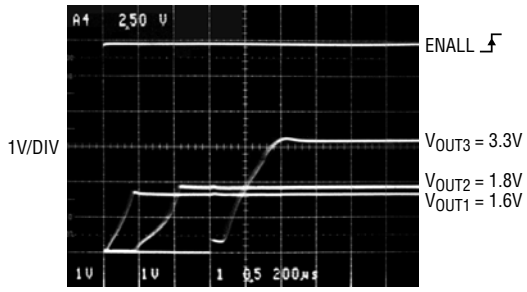
TYPICAL PERFORMANCE CHARACTERISTICS

Switching Regulator 3 Step Response (0mA to 300mA)



100µs/DIV

Start-Up Sequencing with SEQ = 0V
V_{IN1} = V_{IN2} = V_{IN3} = 4.2V
All Outputs Loaded with 5mA



200µs/DIV

PIN FUNCTIONS

LDO3V3 (Pin 1): 3.3V LDO Output Pin. This pin provides a regulated, always-on, 3.3V supply voltage. LDO3V3 gets its power from V_{OUT}. It may be used for light loads such as a watchdog microprocessor or real time clock. A 1µF capacitor is required from LDO3V3 to ground. If the LDO3V3 output is not used it should be disabled by connecting it to V_{OUT}.

CLPROG (Pin 2): USB Current Limit Program and Monitor Pin. A resistor from CLPROG to ground determines the upper limit of the current drawn from the V_{BUS} pin. A fraction of the V_{BUS} current is sent to the CLPROG pin when the synchronous switch of the PowerPath switching regulator is on. The switching regulator delivers power until the CLPROG pin reaches 1.188V. Several V_{BUS} current limit settings are available via user input which will typically correspond to the 500mA and 100mA USB specifications. A multilayer ceramic averaging capacitor or R-C network is required at CLPROG for filtering.

NTC (Pin 3): Input to the Thermistor Monitoring Circuits. The NTC pin connects to a battery's thermistor to determine if the battery is too hot or too cold to charge. If the battery's temperature is out of range, charging is paused until it re-enters the valid range. A low drift bias resistor is required from V_{BUS} to NTC and a thermistor is required from NTC to ground. If the NTC function is not desired, the NTC pin should be grounded.

SW1 (Pin 4): Power Transmission Pin for (Buck) Switching Regulator 1.

V_{IN1} (Pin 5): Power Input for (Buck) Switching Regulator 1. This pin will generally be connected to V_{OUT}. A 1µF MLCC capacitor is recommended on this pin.

FB1 (Pin 6): Feedback Input for (Buck) Switching Regulator 1. When regulator 1's control loop is complete, this pin servos to 1 of 16 possible set-points based on the commanded value from the I^2C serial port. See Table 4.

FB3 (Pin 7): Feedback Input for (Buck-Boost) Switching Regulator 3. When regulator 3's control loop is complete, this pin servos to 1 of 16 possible set-points based on the commanded value from the I^2C serial port. See Table 4.

V_{C3} (Pin 8): Output of the Error Amplifier and Voltage Compensation Node for (Buck-Boost) Switching Regulator 3. External Type I or Type III compensation (to FB3) connects to this pin. See Applications Information section for selecting buck-boost compensation components.

SWAB3 (Pin 9): Switch Node for (Buck-Boost) Switching Regulator 3. Connected to internal power switches A and B. External inductor connects between this node and SWCD3.

DV_{CC} (Pin 10): Logic Supply for the I^2C Serial Port.

V_{IN3} (Pin 11): Power Input for (Buck-Boost) Switching Regulator 3. This pin will generally be connected to V_{OUT}. A 1µF (min) MLCC capacitor is recommended on this pin.

V_{OUT3} (Pin 12): Regulated Output Voltage for (Buck-Boost) Switching Regulator 3.

PIN FUNCTIONS

SCL (Pin 13): Clock Input Pin for the I^2C Serial Port. The I^2C logic levels are scaled with respect to DV_{CC}.

SWCD3 (Pin 14): Switch Node for (Buck-Boost) Switching Regulator 3. Connected to internal power switches C and D. External inductor connects between this node and SWAB3.

PGOODALL (Pin 15): Logic Output. This in an open-drain output which indicates that all enabled switching regulators have settled to their final value. It can be used as a power-on reset for the primary microprocessor.

SDA (Pin 16): Data Input Pin for the I^2C Serial Port. The I^2C logic levels are scaled with respect to DV_{CC}.

FB2 (Pin 17): Feedback Input for (Buck) Switching Regulator 2. When regulator 2's control loop is complete, this pin servos to a fixed voltage of 0.8V.

V_{IN2} (Pin 18): Power Input for (Buck) Switching Regulator 2. This pin will generally be connected to V_{OUT}. A 1µF MLCC capacitor is recommended on this pin.

SW2 (Pin 19): Power Transmission Pin for (Buck) Switching Regulator 2.

PROG (Pin 20): Charge Current Program and Charge Current Monitor Pin. Connecting a resistor from PROG to ground programs the charge current. If sufficient input power is available in constant-current mode, this pin servos to 1V. The voltage on this pin always represents the actual charge current.

$\overline{CHRG}$ (Pin 21): Open-Drain Charge Status Output. The $\overline{CHRG}$ pin indicates the status of the battery charger. Four possible states are represented by $\overline{CHRG}$: charging, not charging, unresponsive battery and battery temperature out of range. $\overline{CHRG}$ is modulated at 35kHz and switches between a low and a high duty cycle for easy recognition by either humans or microprocessors. See Table 1. $\overline{CHRG}$ requires a pull-up resistor and/or LED to provide indication.

GATE (Pin 22): Analog Output. This pin controls the gate of an optional external P-channel MOSFET transistor used to supplement the ideal diode between V_{OUT} and BAT. The external ideal diode operates in parallel with the internal ideal diode. The source of the P-channel MOSFET should be connected to V_{OUT} and the drain should be connected to BAT. If the external ideal diode FET is not used, GATE should be left floating.

BAT (Pin 23): Single Cell Li-Ion Battery Pin. Depending on available V_{BUS} power, a Li-Ion battery on BAT will either deliver power to V_{OUT} through the ideal diode or be charged from V_{OUT} via the battery charger.

V_{OUT} (Pin 24): Output Voltage of the Switching Power-Path Controller and Input Voltage of the Battery Charger. The majority of the portable product should be powered from V_{OUT}. The LTC3556 will partition the available power between the external load on V_{OUT} and the internal battery charger. Priority is given to the external load and any extra power is used to charge the battery. An ideal diode from BAT to V_{OUT} ensures that V_{OUT} is powered even if the load exceeds the allotted power from V_{BUS} or if the V_{BUS} power source is removed. V_{OUT} should be bypassed with a low impedance ceramic capacitor.

V_{BUS} (Pin 25): Primary Input Power Pin. This pin delivers power to V_{OUT} via the SW pin by drawing controlled current from a DC source such as a USB port or wall adapter.

SW (Pin 26): Power Transmission Pin for the USB Power Path. The SW pin delivers power from V_{BUS} to V_{OUT} via the step-down switching regulator. A 3.3µH inductor should be connected from SW to V_{OUT}.

SEQ (Pin 27): Sequence Select Logic Input. Three-state input which determines start-up sequence after ENALL is asserted.

If tied to GND, start-up sequence is:

Buck 1 → Buck 2 → Buck-Boost

If tied to V_{OUT}, start-up sequence is:

Buck 1 → Buck-Boost → Buck 2

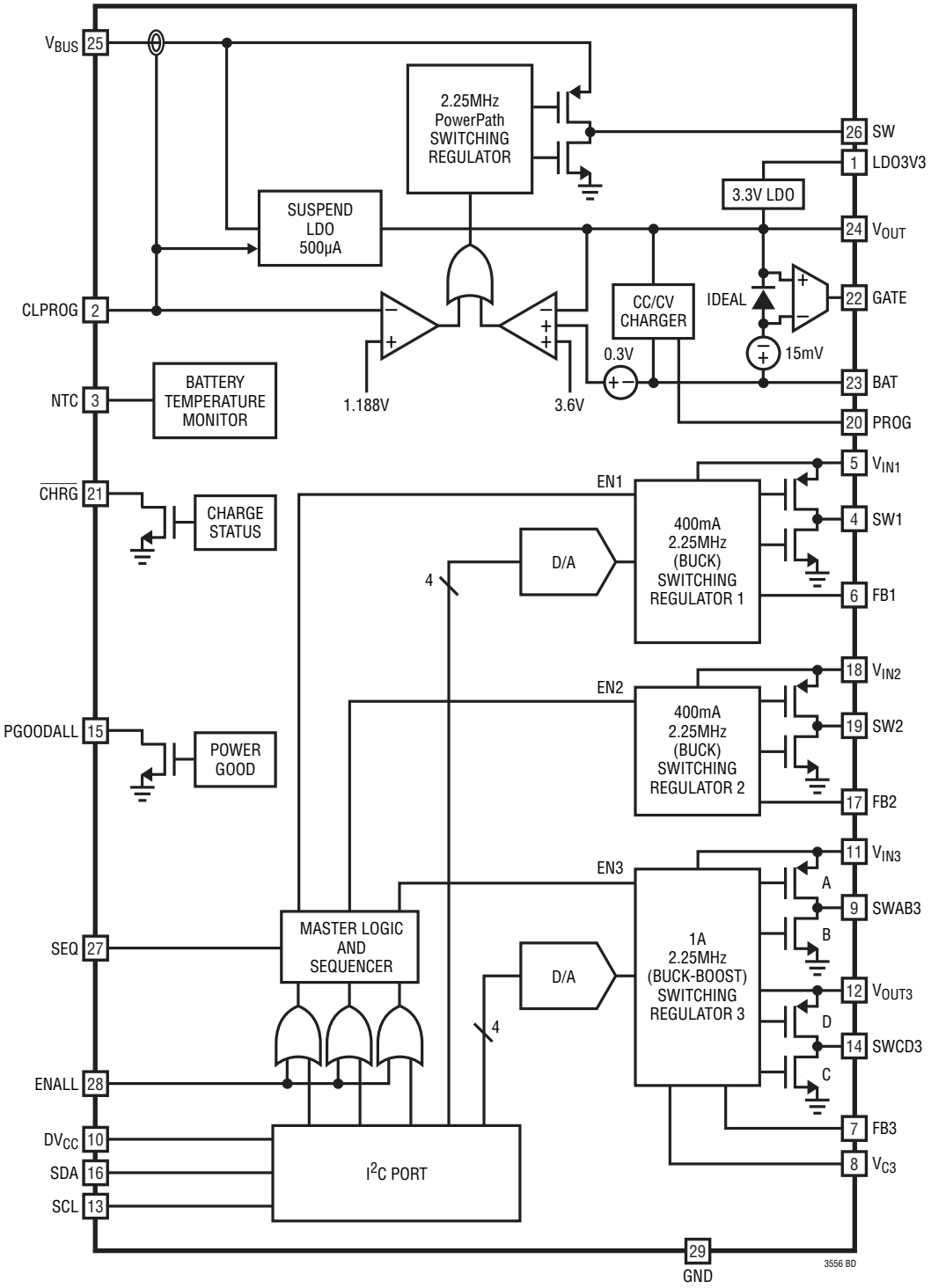
If left floating, start-up sequence is:

Buck-Boost → Buck 1 → Buck 2

ENALL (Pin 28): Enable All Logic Input. Enables all three switching regulators in sequence according to the state of the SEQ pin. Active high. Has a 5.5M internal pull-down resistor. Alternately, all switching regulators can be individually enabled via the I^2C serial port.

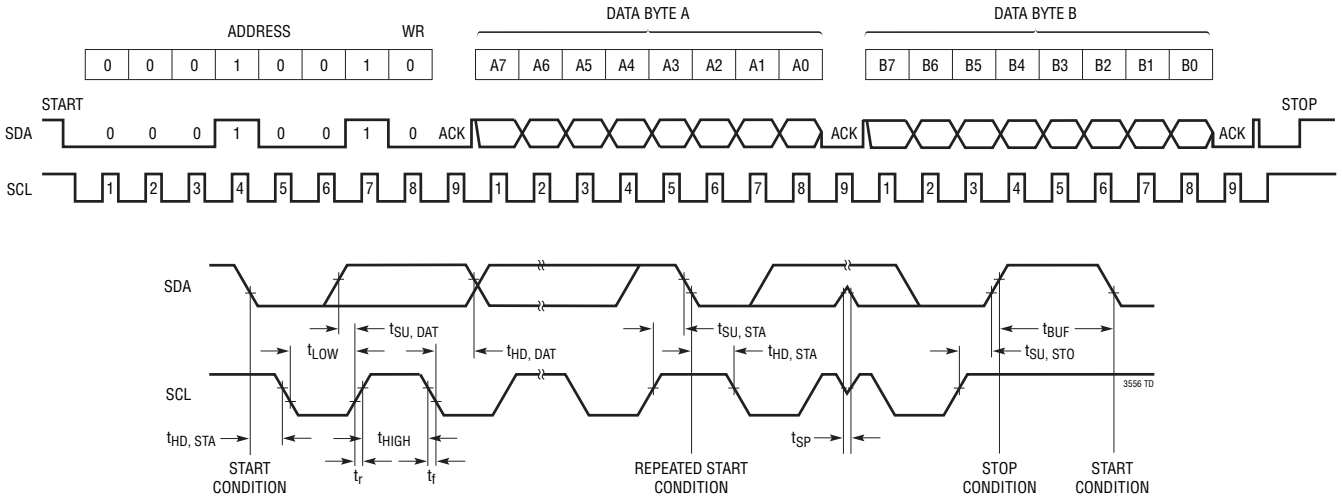
Exposed Pad (Pin 29): Ground. The Exposed Pad should be connected to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the LTC3556.

BLOCK DIAGRAM



TIMING DIAGRAM

I²C Timing Diagram



OPERATION

Introduction

The LTC3556 is a highly integrated power management IC which includes a high efficiency switch mode PowerPath controller, a battery charger, an ideal diode, an always-on LDO, two 400mA buck switching regulators and a 1A buck-boost switching regulator. The entire chip is controllable via an I²C serial port.

Designed specifically for USB applications, the PowerPath controller incorporates a precision average input current step-down switching regulator to make maximum use of the allowable USB power. Because power is conserved, the LTC3556 allows the load current on V_{OUT} to exceed the current drawn by the USB port without exceeding the USB load specifications.

The PowerPath switching regulator and battery charger communicate to ensure that the input current never violates the USB specifications.

The ideal diode from BAT to V_{OUT} guarantees that ample power is always available to V_{OUT} even if there is insufficient or absent power at V_{BUS}.

An "always-on" LDO provides a regulated 3.3V from available power at V_{OUT}. Drawing very little quiescent current, this LDO will be on at all times and can be used to supply up to 25mA.

The three switching regulators can be enabled together in any desired sequence via the ENALL and SEQ pins or can be independently enabled via the I²C serial port. Under I²C control, one of the 400mA bucks and the 1A buck-boost have adjustable set-points so that voltages can be reduced when high processor performance is not needed. Along with constant frequency PWM mode, all three switching regulators have a low power burst-only mode setting for significantly reduced quiescent current under light load conditions. Additionally, the 400mA bucks can be configured for automatic Burst Mode operation or LDO mode.

High Efficiency Switching PowerPath Controller

Whenever V_{BUS} is available and the PowerPath switching regulator is enabled, power is delivered from V_{BUS} to V_{OUT} via SW. V_{OUT} drives the combination of the external load (including switching regulators 1, 2 and 3) and the battery charger.

If the combined load does not exceed the PowerPath switching regulator's programmed input current limit, V_{OUT} will track 0.3V above the battery (Bat-Track). By keeping the voltage across the battery charger low, efficiency is optimized because power lost to the linear battery charger is minimized. Power available to the external load is therefore optimized.

OPERATION

If the combined load at V_{OUT} is large enough to cause the switching power supply to reach the programmed input current limit, the battery charger will reduce its charge current by that amount necessary to enable the external load to be satisfied. Even if the battery charge current is set to exceed the allowable USB current, the USB specification will not be violated. The switching regulator will limit the average input current so that the USB specification is never violated. Furthermore, load current at V_{OUT} will always be prioritized and only remaining available power will be used to charge the battery.

If the voltage at BAT is below 3.3V, or the battery is not present and the load requirement does not cause the switching regulator to exceed the USB specification, V_{OUT} will regulate at 3.6V, thereby providing instant-on operation. If the load exceeds the available power, V_{OUT} will drop to a voltage between 3.6V and the battery voltage. If there is no battery present when the load exceeds the available USB power, V_{OUT} can drop toward ground.

The power delivered from V_{BUS} to V_{OUT} is controlled by a 2.25MHz constant-frequency step-down switching regulator. To meet the USB maximum load specification, the switching regulator includes a control loop which ensures that the average input current is below the level programmed at CLPROG.

The current at CLPROG is a fraction (h_{CLPROG}^{-1}) of the V_{BUS} current. When a programming resistor and an averaging capacitor are connected from CLPROG to GND, the voltage on CLPROG represents the average input current of the switching regulator. When the input current approaches the programmed limit, CLPROG reaches V_{CLPROG}, 1.188V and power out is held constant. The input current limit is programmed by the B1 and B0 bits of the I^2C serial port. It can be configured to limit average input current to one of several possible settings as well as be deactivated (USB Suspend). The input current limit will be set by the V_{CLPROG} servo voltage and the resistor on CLPROG according to the following expression:

$$I_{VBUS} = I_{VBUSQ} + \frac{V_{CLPROG}}{R_{CLPROG}} \bullet (h_{CLPROG} + 1)$$

Figure 1 shows the range of possible voltages at V_{OUT} as a function of battery voltage.

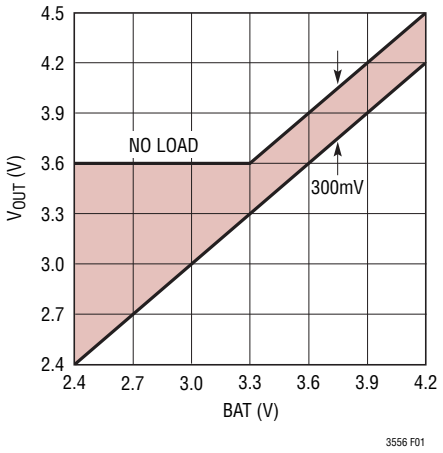


Figure 1. V_{OUT} vs BAT

Ideal Diode from BAT to V_{OUT}

The LTC3556 has an internal ideal diode as well as a controller for an optional external ideal diode. The ideal diode controller is always on and will respond quickly whenever V_{OUT} drops below BAT.

If the load current increases beyond the power allowed from the switching regulator, additional power will be pulled from the battery via the ideal diode. Furthermore, if power to V_{BUS} (USB or wall power) is removed, then all of the application power will be provided by the battery via the ideal diode. The transition from input power to battery power at V_{OUT} will be quick enough to allow only the 10µF capacitor to keep V_{OUT} from drooping. The ideal diode consists of a precision amplifier that enables a large on-chip P-channel MOSFET transistor whenever the voltage at

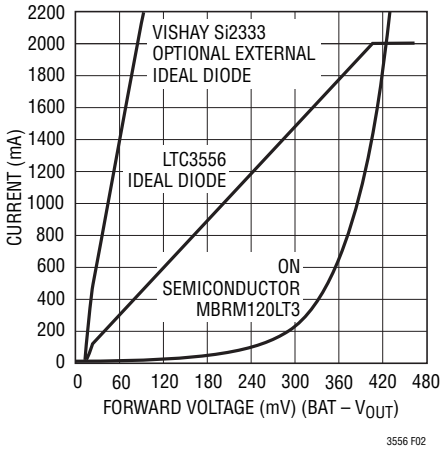


Figure 2. Ideal Diode Operation

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V_{OUT} is approximately 15mV (V_{FWD}) below the voltage at BAT. The resistance of the internal ideal diode is approximately 180mΩ. If this is sufficient for the application, then no external components are necessary. However, if more conductance is needed, an external P-channel MOSFET transistor can be added from BAT to V_{OUT}.

When an external P-channel MOSFET transistor is present, the GATE pin of the LTC3556 drives its gate for automatic ideal diode control. The source of the external P-channel MOSFET should be connected to V_{OUT} and the drain should be connected to BAT. Capable of driving a 1nF load, the GATE pin can control an external P-channel MOSFET transistor having an on-resistance of 40mΩ or lower.

Suspend LDO

If the LTC3556 is configured for USB suspend mode, the switching regulator is disabled and the suspend LDO provides power to the V_{OUT} pin (presuming there is power available to V_{BUS}). This LDO will prevent the battery from running down when the portable product has access to a suspended USB port. Regulating at 4.6V, this LDO only becomes active when the switching converter is disabled (suspended). To remain compliant with the USB specification, the input to the LDO is current limited so that it will not exceed the 500µA low power suspend specification.

If the load on V_{OUT} exceeds the suspend current limit, the additional current will come from the battery via the ideal diode.

3.3V Always-On Supply

The LTC3556 includes a low quiescent current low dropout regulator that is always powered. This LDO can be used to provide power to a system pushbutton controller, standby microcontroller or real time clock. Designed to deliver up to 25mA, the always-on LDO requires at least a 1µF low impedance ceramic bypass capacitor for compensation. The LDO is powered from V_{OUT}, and therefore will enter dropout at loads less than 25mA as V_{OUT} falls near 3.3V. If the LDO3V3 output is not used, it should be disabled by connecting it to V_{OUT}.

V_{BUS} Undervoltage Lockout (UVLO)

An internal undervoltage lockout circuit monitors V_{BUS} and keeps the PowerPath switching regulator off until V_{BUS} rises above 4.30V and is about 200mV above the battery voltage. Hysteresis on the UVLO turns off the regulator if V_{BUS} drops below 4.00V or to within 50mV of BAT. When this happens, system power at V_{OUT} will be drawn from the battery via the ideal diode.

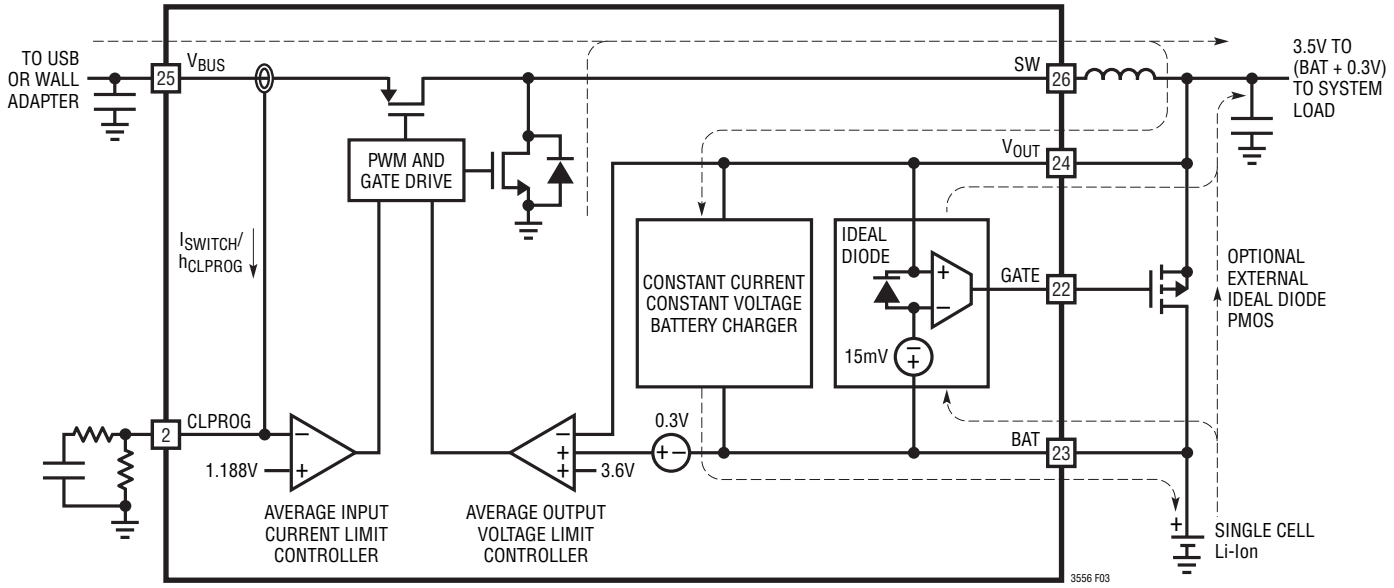

Figure 3. PowerPath Block Diagram

OPERATION

Battery Charger

The LTC3556 includes a constant-current/constant-voltage battery charger with automatic recharge, automatic termination by safety timer, low voltage trickle charging, bad cell detection and thermistor sensor input for out-of-temperature charge pausing.

Battery Preconditioning

When a battery charge cycle begins, the battery charger first determines if the battery is deeply discharged. If the battery voltage is below V_{TRKL}, typically 2.85V, an automatic trickle charge feature sets the battery charge current to 10% of the programmed value. If the low voltage persists for more than 1/2 hour, the battery charger automatically terminates and indicates via the $\overline{CHRG}$ pin that the battery was unresponsive.

Once the battery voltage is above 2.85V, the battery charger begins charging in full power constant-current mode. The current delivered to the battery will try to reach 1022V/R_{PROG}. Depending on available input power and external load conditions, the battery charger may or may not be able to charge at the full programmed rate. The external load will always be prioritized over the battery charge current. The USB current limit programming will always be observed and only additional power will be available to charge the battery. When system loads are light, battery charge current will be maximized.

Charge Termination

The battery charger has a built-in safety timer. When the voltage on the battery reaches the pre-programmed float voltage of 4.200V, the battery charger will regulate the battery voltage and the charge current will decrease naturally. Once the battery charger detects that the battery has reached 4.200V, the four hour safety timer is started. After the safety timer expires, charging of the battery will discontinue and no more current will be delivered.

Automatic Recharge

After the battery charger terminates, it will remain off drawing only microamperes of current from the battery. If the portable product remains in this state long enough, the battery will eventually self discharge. To ensure that the battery is always topped off, a charge cycle will automatically begin when the battery voltage falls below 4.1V. In the event that the safety timer is running when the battery voltage falls below 4.1V, it will reset back to zero. To prevent brief excursions below 4.1V from resetting the safety timer, the battery voltage must be below 4.1V for more than 1.3ms. The charge cycle and safety timer will also restart if the V_{BUS} UVLO cycles low and then high (e.g., V_{BUS} is removed and then replaced), or if the battery charger is cycled on and off by the I^2C port.

Charge Current

The charge current is programmed using a single resistor from PROG to ground. 1/1022th of the battery charge current is sent to PROG which will attempt to servo to 1.000V. Thus, the battery charge current will try to reach 1022 times the current in the PROG pin. The program resistor and the charge current are calculated using the following equations:

$$R_{PROG} = \frac{1022V}{I_{CHRG}},\ I_{CHRG} = \frac{1022V}{R_{PROG}}$$

In either the constant-current or constant-voltage charging modes, the voltage at the PROG pin will be proportional to the actual charge current delivered to the battery. Therefore, the actual charge current can be determined at any time by monitoring the PROG pin voltage and using the following equation:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1022$$

In many cases, the actual battery charge current, I_{BAT}, will be lower than I_{CHRG} due to limited input power available and prioritization with the system load drawn from V_{OUT}.

Charge Status Indication

The $\overline{CHRG}$ pin indicates the status of the battery charger. Four possible states are represented by $\overline{CHRG}$ which include charging, not charging, unresponsive battery, and battery temperature out of range.

The signal at the $\overline{CHRG}$ pin can be easily recognized as one of the above four states by either a human or a microprocessor. An open-drain output, the $\overline{CHRG}$ pin can

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drive an indicator LED through a current limiting resistor for human interfacing or simply a pull-up resistor for microprocessor interfacing.

To make the $\overline{CHRG}$ pin easily recognized by both humans and microprocessors, the pin is either Low for charging, High for not charging, or it is switched at high frequency (35kHz) to indicate the two possible faults, unresponsive battery and battery temperature out of range.

When charging begins, $\overline{CHRG}$ is pulled low and remains low for the duration of a normal charge cycle. When charging is complete, i.e., the BAT pin reaches 4.200V and the charge current has dropped to one tenth of the programmed value, the $\overline{CHRG}$ pin is released (Hi-Z). If a fault occurs, the pin is switched at 35kHz. While switching, its duty cycle is modulated between a high and low value at a very low frequency. The low and high duty cycles are disparate enough to make an LED appear to be on or off thus giving the appearance of "blinking". Each of the two faults has its own unique "blink" rate for human recognition as well as two unique duty cycles for machine recognition.

The $\overline{CHRG}$ pin does not respond to the C/10 threshold if the LTC3556 is in V_{BUS} current limit. This prevents false end of charge indications due to insufficient power available to the battery charger.

Table 1 illustrates the four possible states of the $\overline{CHRG}$ pin when the battery charger is active.

Table 1. $\overline{CHRG}$ Signal

STATUS	FREQUENCY	MODULATION (BLINK) FREQUENCY	DUTY CYCLES
Charging	0Hz	0Hz (Lo-Z)	100%
Not Charging	0Hz	0Hz (Hi-Z)	0%
NTC Fault	35kHz	1.5Hz at 50%	6.25%, 93.75%
Bad Battery	35kHz	6.1Hz at 50%	12.5%, 87.5%

An NTC fault is represented by a 35kHz pulse train whose duty cycle alternates between 6.25% and 93.75% at a 1.5Hz rate. A human will easily recognize the 1.5Hz rate as a "slow" blinking which indicates the out-of-range battery temperature while a microprocessor will be able to decode either the 6.25% or 93.75% duty cycles as an NTC fault.

If a battery is found to be unresponsive to charging (i.e., its voltage remains below 2.85V for 1/2 hour), the $\overline{CHRG}$ pin gives the battery fault indication. For this fault, a human would easily recognize the frantic 6.1Hz "fast" blink of the LED while a microprocessor would be able to decode either the 12.5% or 87.5% duty cycles as a bad battery fault.

Note that the LTC3556 is a 3-terminal PowerPath product where system load is always prioritized over battery charging. Due to excessive system load, there may not be sufficient power to charge the battery beyond the trickle charge threshold voltage within the bad battery timeout period. In this case, the battery charger will falsely indicate a bad battery. System software may then reduce the load and reset the battery charger to try again.

Although very improbable, it is possible that a duty cycle reading could be taken at the bright-dim transition (low duty cycle to high duty cycle). When this happens the duty cycle reading will be precisely 50%. If the duty cycle reading is 50%, system software should disqualify it and take a new duty cycle reading.

NTC Thermistor

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack.

To use this feature, connect the NTC thermistor, R_{NTC}, between the NTC pin and ground and a resistor, R_{NOM}, from V_{BUS} to the NTC pin. R_{NOM} should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C (R25). A 100k thermistor is recommended since thermistor current is not measured by the LTC3556 and will have to be budgeted for USB compliance.

The LTC3556 will pause charging when the resistance of the NTC thermistor drops to 0.54 times the value of R25 or approximately 54k. For Vishay "Curve 1" thermistor, this corresponds to approximately 40°C. If the battery charger is in constant-voltage (float) mode, the safety timer also pauses until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The LTC3556 is also designed to pause charging when the value of the NTC thermistor increases to 3.25 times the value of R25. For Vishay "Curve 1" this resistance, 325k, corresponds to approximately 0°C. The hot and cold comparators each

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have approximately 3°C of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin disables the NTC charge pausing function.

Thermal Regulation

To optimize charging time, an internal thermal feedback loop may automatically decrease the programmed charge current. This will occur if the die temperature rises to approximately 110°C. Thermal regulation protects the LTC3556 from excessive temperature due to high power operation or high ambient thermal conditions and allows the user to push the limits of the power handling capability with a given circuit board design without risk of damaging the LTC3556 or external components. The benefit of the LTC3556 thermal regulation loop is that charge current can be set according to actual conditions rather than worst-case conditions with the assurance that the battery charger will automatically reduce the current in worst-case conditions.

I²C Interface

The LTC3556 may receive commands from a host (master) using the standard I²C 2-wire interface. The Timing Diagram shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 I²C accelerator, are required on these lines. The LTC3556 is a receive-only (slave) device. The I²C control signals, SDA and SCL are scaled internally to the DV_{CC} supply. DV_{CC} should be connected to the same power supply as the microcontroller generating the I²C signals.

The I²C port has an undervoltage lockout on the DV_{CC} pin. When DV_{CC} is below approximately 1V, the I²C serial port is cleared and switching regulators 1 and 3 are set to full scale.

Bus Speed

The I²C port is designed to be operated at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I²C compliant master device. It also contains input filters designed to suppress glitches should the bus become corrupted.

Start and Stop Condition

A bus master signals the beginning of a communication to a slave device by transmitting a Start condition. A Start condition is generated by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a Stop condition by transitioning SDA from low to high while SCL is high. The bus is then free for communication with another I²C device.

Byte Format

Each byte sent to the LTC3556 must be eight bits long followed by an extra clock cycle for the Acknowledge bit to be returned by the LTC3556. The data should be sent to the LTC3556 most significant bit (MSb) first.

Acknowledge

The Acknowledge signal is used for handshaking between the master and the slave. An Acknowledge (active low) generated by the slave (LTC3556) lets the master know that the latest byte of information was received. The Acknowledge related clock pulse is generated by the master. The master releases the SDA line (high) during the Acknowledge clock cycle. The slave receiver must pull down the SDA line during the Acknowledge clock pulse so that it remains a stable Low during the High period of this clock pulse.

Slave Address

The LTC3556 responds to only one 7-bit address which has been factory programmed to 0001001. The LSb of the address byte is 1 for Read and 0 for Write. This device is write only corresponding to an address byte of 00010010 (0×12). If the correct seven bit address is given but the R/W bit is 1, the LTC3556 will not respond.

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Table 2. I^2C Serial Port Mapping (Defaults to 0xFF00 in Reset State or if DV_{CC} = 0V)

A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
Switching Regulator 1 Voltage (See Table 4)				Switching Regulator 3 Voltage (See Table 4)				Disable Battery Charger	Switching Regulator Modes (See Table 5)		Enable Regulator 1	Enable Regulator 2	Enable Regulator 3	Input Current Limit (See Table 3)	

Table 3. USB Current Limit Settings

B1	B0	USB SETTING
0	1	10x Mode (Wall 1A Limit)
1	1	5x Mode (USB 500mA Limit)
0	0	1x Mode (USB 100mA Limit)
1	0	Suspend

Table 4. Switching Regulator Servo Voltage

A7	A6	A5	A4	SWITCHING REGULATOR 1 SERVO VOLTAGE
A3	A2	A1	A0	SWITCHING REGULATOR 3 SERVO VOLTAGE
0	0	0	0	0.425V
0	0	0	1	0.450V
0	0	1	0	0.475V
0	0	1	1	0.500V
0	1	0	0	0.525V
0	1	0	1	0.550V
0	1	1	0	0.575V
0	1	1	1	0.600V
1	0	0	0	0.625V
1	0	0	1	0.650V
1	0	1	0	0.675V
1	0	1	1	0.700V
1	1	0	0	0.725V
1	1	0	1	0.750V
1	1	1	0	0.775V
1	1	1	1	0.800V

Table 5. Switching Regulator Modes

B6	B5	MODE OF (BUCK) SWITCHING REGULATORS 1 AND 2	MODE OF (BUCK-BOOST) SWITCHING REGULATOR 3
0	0	Pulse Skip Mode	PWM Mode
1	1	Burst Mode Operation	
0	1	Forced Burst Mode Operation	Burst Mode Operation
1	0	LDO Mode	

Bus Write Operation

The master initiates communication with the LTC3556 with a Start condition and a 7-bit address followed by the Write Bit R/W = 0. If the address matches that of the LTC3556, the LTC3556 returns an Acknowledge. The master should then deliver the most significant data byte. Again the LTC3556 acknowledges and the cycle is repeated for a total of one address byte and two data bytes. Each data byte is transferred to an internal holding latch upon the return of an Acknowledge. After both data bytes have been transferred to the LTC3556, the master may terminate the communication with a Stop condition. Alternatively, a Repeat-Start condition can be initiated by the master and another chip on the I^2C bus can be addressed. This cycle can continue indefinitely and the LTC3556 will remember the last input of valid data that it received. Once all chips on the bus have been addressed and sent valid data, a global Stop condition can be sent and the LTC3556 will update its command latch with the data that it had received.

In certain circumstances the data on the I^2C bus may become corrupted. In these cases the LTC3556 responds appropriately by preserving only the last set of complete data that it has received. For example, assume the LTC3556 has been successfully addressed and is receiving data when a Stop condition mistakenly occurs. The LTC3556 will ignore this stop condition and will not respond until a new Start condition, correct address, new set of data and Stop condition are transmitted.

Likewise, with only one exception, if the LTC3556 was previously addressed and sent valid data but not updated with a Stop, it will respond to any Stop that appears on the bus, independent of the number of Repeat-Starts that have occurred. If a Repeat-Start is given and the LTC3556 successfully acknowledges its address and first byte, it will not respond to a Stop until both bytes of the new data have been received and acknowledged.

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Disabling the I²C Port

The I²C serial port can be disabled by grounding the DV_{CC} pin. In this mode, control automatically passes to the individual logic input pins ENALL and SEQ. However, considerable functionality is not available in this mode such as the ability to independently enable the three switching regulators and disable the battery charger. In addition, with the I²C port disabled, both programmable switching regulators default to a fixed servo voltage of 0.8V, both 400mA bucks default to pulse skip mode, the 1A buck-boost defaults to PWM mode, and the USB input current limit defaults to 1x mode (100mA Limit).

PGOODALL Pin

The PGOODALL pin is an open-drain output used to indicate that all enabled switching regulators have reached their final voltage. PGOODALL remains low impedance until the last enabled regulator in the sequence reaches 92% of its regulation value. A 230ms delay is included to allow a system microcontroller ample time to reset itself. PGOODALL may be used as a power-on reset to the microprocessor powered by one (or more) of the three regulated outputs. PGOODALL is an open-drain output and requires a pull-up resistor to the input voltage of the monitoring microprocessor or another appropriate power source.

400mA Step-Down Switching Regulators

The LTC3556 contains two 2.25MHz step-down (buck) constant-frequency current mode switching regulators. Each buck regulator can provide up to 400mA of output current. Both buck regulators can be programmed for a minimum output voltage of 0.8V and can be used to power a microcontroller core, microcontroller I/O, memory, disk drive or other logic circuitry. One of the buck regulators has I²C programmable set-points for on-the-fly power savings. Both buck converters support 100% duty cycle operation (low dropout mode) when their input voltage drops very close to their output voltage. To suit a variety of applications, selectable mode functions can be used to trade off noise for efficiency. Four modes are available to control the operation of the LTC3556's buck regulators. At moderate to heavy loads, the pulse skip mode provides the least noise switching solution. At lighter loads, either Burst Mode operation, forced Burst Mode operation or LDO mode may be selected. The buck regulators include soft-start to limit inrush current when powering on, short-circuit current protection and switch node slew limiting circuitry to reduce radiated EMI. No external compensation components are required. The operating mode of the buck regulators can be set by I²C control and defaults to pulse skip mode if the I²C port is not used. Both buck converters are enabled (along with the buck-boost) when the ENALL pin is asserted or each may be individually enabled by the I²C port. Buck regulator 1 has a programmable feedback servo voltage via I²C control (which defaults to 800mV if the I²C port is not used) whereas buck regulator 2 has a fixed feedback servo voltage of 800mV. The buck regulator input supplies V_{IN1} and V_{IN2} will generally be connected to the system load pin V_{OUT}.

Buck Regulator Output Voltage Programming

Both buck regulators can be programmed for output voltages greater than 0.8V. The full-scale output voltage for each buck regulator is programmed using a resistor divider from the buck regulator output connected to the feedback pins (FB1 and FB2) such that:

$$V_{OUTX} = V_{FBX}\left(\frac{R1}{R2}+1\right)$$

where V_{FBX} ranges from 0.425V to 0.8V for buck regulator 1 and V_{FBX} is fixed at 0.8V for buck regulator 2. See Figure 4.

Typical values for R1 are in the range of 40k to 1M. The capacitor, C_{FB}, cancels the pole created by feedback resistors and the input capacitance of the FBx pin and also helps to improve transient response for output voltages much

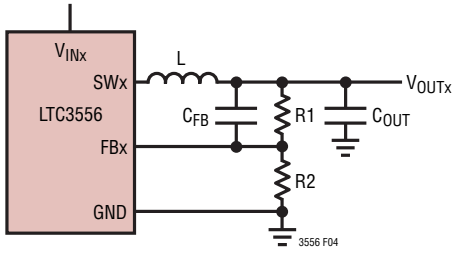

Figure 4. Buck Converter Application Circuit

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greater than 0.8V. A variety of capacitor sizes can be used for C_{FB} but a value of 10pF is recommended for most applications. Experimentation with capacitor sizes between 2pF and 22pF may yield improved transient response.

Buck Regulator Operating Modes

The LTC3556's buck regulators include four possible operating modes to meet the noise/power needs of a variety of applications.

In pulse skip mode, an internal latch is set at the start of every cycle which turns on the main P-channel MOSFET switch. During each cycle, a current comparator compares the peak inductor current to the output of an error amplifier. The output of the current comparator resets the internal latch which causes the main P-channel MOSFET switch to turn off and the N-channel MOSFET synchronous rectifier to turn on. The N-channel MOSFET synchronous rectifier turns off at the end of the 2.25MHz cycle or if the current through the N-channel MOSFET synchronous rectifier drops to zero. Using this method of operation, the error amplifier adjusts the peak inductor current to deliver the required output power. All necessary compensation is internal to the switching regulator requiring only a single ceramic output capacitor for stability. At light loads in PWM mode, the inductor current may reach zero on each pulse which will turn off the N-channel MOSFET synchronous rectifier. In this case, the switch node (SW) goes high impedance and the switch node voltage will "ring." This is discontinuous mode operation and is normal behavior for a switching regulator. At very light loads in pulse skip mode, the buck regulators will automatically skip pulses as needed to maintain output regulation.

At high duty cycles ($V_{OUTx} > V_{INx}/2$) it is possible for the inductor current to reverse, causing the buck regulator to operate continuously at light loads. This is normal and regulation is maintained, but the supply current will increase to several milliamperes due to continuous switching.

In forced Burst Mode operation, the buck regulators use a constant-current algorithm to control the inductor current. By controlling the inductor current directly and using a hysteretic control loop, both noise and switching losses are minimized. In this mode output power is limited. While in forced Burst Mode operation, the output capacitor is charged to a voltage slightly higher than the regulation point. The step-down converter then goes into sleep mode, during which the output capacitor provides the load current. In sleep mode, most of the regulator's circuitry is powered down, helping conserve battery power. When the output voltage drops below a predetermined value, the buck regulator circuitry is powered on and another burst cycle begins. The duration for which the buck regulator operates in sleep mode depends on the load current. The sleep time decreases as the load current increases. The maximum output current in forced Burst Mode operation is about 100mA for buck regulators 1 and 2. The buck regulators will not enter sleep mode if the maximum output current is exceeded in forced Burst Mode operation and the output will drop out of regulation. Forced Burst Mode operation provides a significant improvement in efficiency at light loads at the expense of higher output ripple when compared to pulse skip mode. For many noise-sensitive systems, forced Burst Mode operation might be undesirable at certain times (i.e., during a transmit or receive cycle of a wireless device), but highly desirable at others (i.e., when the device is in low power standby mode). The I^2C port can be used to enable or disable forced Burst Mode operation at any time, offering both low noise and low power operation when they are needed.

In Burst Mode operation, the buck regulator automatically switches between fixed frequency PWM operation and hysteretic control as a function of the load current. At light loads, the buck regulators operate in hysteretic mode in much the same way as described for the forced Burst Mode operation. Burst Mode operation provides slightly less output ripple at the expense of slightly lower efficiency than forced Burst Mode operation. At heavy loads, the buck regulator operates in the same manner as pulse skip operation does at high loads. For applications that can tolerate some output ripple at low output currents, Burst Mode operation provides better efficiency than pulse skip at light loads while still providing the full specified output current of the buck regulator.

Finally, the buck regulators have an LDO mode that gives a DC option for regulating their output voltages. In LDO mode, the buck regulators are converted to linear regula-

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tors and deliver continuous power from their SWx pins through their respective inductors. This mode gives the lowest possible output noise as well as low quiescent current at light loads.

The buck regulators allow mode transition on the fly, providing seamless transition between modes even under load. This allows the user to switch back and forth between modes to reduce output ripple or increase low current efficiency as needed.

Buck Regulator in Shutdown

The buck regulators are in shutdown when not enabled for operation. In shutdown, all circuitry in the buck regulator is disconnected from the buck regulator input supply leaving only a few nanoamperes of leakage current. The buck regulator outputs are individually pulled to ground through a 10k resistor on the switch pins (SW1 and SW2) when in shutdown.

Buck Regulator Dropout Operation

It is possible for a buck regulator's input voltage, V_{INX}, to approach its programmed output voltage (e.g., a battery voltage of 3.4V with a programmed output voltage of 3.3V). When this happens, the PMOS switch duty cycle increases until it is turned on continuously at 100%. In this dropout condition, the respective output voltage equals the buck regulator's input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor.

Buck Regulator Soft-Start Operation

Soft-start is accomplished by gradually increasing the peak inductor current for each buck regulator over a 500µs period. This allows each output to rise slowly, helping minimize the battery surge current. A soft-start cycle occurs whenever a given buck regulator is enabled, or after a fault condition has occurred (thermal shutdown or UVLO). A soft-start cycle is not triggered by changing operating modes. This allows seamless output operation when transitioning between forced Burst Mode, Burst Mode, pulse skip mode or LDO operation.

Buck Regulator Switching Slew Rate Control

The buck regulators contain new patent pending circuitry to limit the slew rate of the switch node (SW1 and SW2). This new circuitry is designed to transition the switch node over a period of a couple of nanoseconds, significantly reducing radiated EMI and conducted supply noise.

Low Supply Operation

The LTC3556 incorporates an undervoltage lockout circuit on V_{OUT} which shuts down both buck regulators (as well as the buck-boost) when V_{OUT} drops below $V_{OUTUVLO}$. This UVLO prevents unstable operation.

Buck-Boost DC/DC Switching Regulator

The LTC3556 contains a 2.25MHz constant-frequency voltage mode buck-boost switching regulator. The regulator provides up to 1A of output load current. The buck-boost can be programmed to a minimum output voltage of 2.5V and can be used to power a microcontroller core, microcontroller I/O, memory, disk drive or other logic circuitry. When controlled by I^2C, the buck-boost has programmable set-points for on-the-fly power savings. To suit a variety of applications, a selectable mode function allows the user to trade off noise for efficiency. Two modes are available to control the operation of the LTC3556's buck-boost regulator. At moderate to heavy loads, the constant frequency PWM mode provides the least noise switching solution. At lighter loads Burst Mode operation may be selected. The full-scale output voltage is programmed by a user-supplied resistive divider returned to the FB3 pin. An error amplifier compares the divided output voltage with a reference and adjusts the compensation voltage accordingly until the FB3 has stabilized to the selected reference voltage (0.425V to 0.8V). The buck-boost regulator also includes a soft-start to limit inrush current and voltage overshoot when powering on, short circuit current protection, and switch node slew limiting circuitry for reduced radiated EMI.

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Input Current Limit

The input current limit comparator will shut the input PMOS switch off once current exceeds 2.5A (typical). The 2.5A input current limit also protects against a grounded V_{OUT3} node.

Output Overvoltage Protection

If the FB3 node were inadvertently shorted to ground, then the output would increase indefinitely with the maximum current that could be sourced from V_{IN3}. The LTC3556 protects against this by shutting off the input PMOS if the output voltage exceeds 5.6V (typical).

Low Output Voltage Operation

When the output voltage is below 2.65V (typical) during startup, Burst Mode operation is disabled and switch D is turned off (allowing forward current through the well diode and limiting reverse current to 0mA).

Buck-Boost Regulator PWM Operating Mode

In PWM mode the voltage seen at FB3 is compared to the selected reference voltage (0.425V to 0.8V). From the FB3 voltage an error amplifier generates an error signal seen at V_{C3}. This error signal commands PWM waveforms that modulate switches A, B, C and D. Switches A and B operate synchronously as do switches C and D. If V_{IN3} is significantly greater than the programmed V_{OUT3}, then the converter will operate in buck mode. In this case switches A and B will be modulated, with switch D always on (and switch C always off), to step down the input voltage to the programmed output. If V_{IN3} is significantly less than the programmed V_{OUT3}, then the converter will operate in boost mode. In this case switches C and D are modulated, with switch A always on (and switch B always off), to step up the input voltage to the programmed output. If V_{IN3} is close to the programmed V_{OUT3}, then the converter will operate in 4-switch mode. In this mode the switches sequence through the pattern of AD, AC, BD to either step the input voltage up or down to the programmed output.

Buck-Boost Regulator Burst Mode Operation

In Burst Mode operation, the buck-boost regulator uses a hysteretic FB3 voltage algorithm to control the output voltage. By limiting FET switching and using a hysteretic control loop, switching losses are greatly reduced. In this mode output current is limited to 50mA typical. While operating in Burst Mode operation, the output capacitor is charged to a voltage slightly higher than the regulation point. The buck-boost converter then goes into a sleep state, during which the output capacitor provides the load current. The output capacitor is charged by charging the inductor until the input current reaches 250mA typical and then discharging the inductor until the reverse current reaches 0mA typical. This process is repeated until the feedback voltage has charged to 6mV above the regulation point. In the sleep state, most of the regulator's circuitry is powered down, helping to conserve battery power. When the feedback voltage drops 6mV below the regulation point, the switching regulator circuitry is powered on and another burst cycle begins. The duration for which the regulator sleeps depends on the load current and output capacitor value. The sleep time decreases as the load current increases. The maximum load current in Burst Mode operation is 50mA typical. The buck-boost regulator will not go to sleep if the current is greater than 50mA, and if the load current increases beyond this point while in Burst Mode operation the output will lose regulation. Burst Mode operation provides a significant improvement in efficiency at light loads at the expense of higher output ripple when compared to PWM mode. For many noise-sensitive systems, Burst Mode operation might be undesirable at certain times (i.e., during a transmit or receive cycle of a wireless device), but highly desirable at others (i.e., when the device is in low power standby mode). The B6 and B5 bits of the I^2C port are used to enable or disable Burst Mode operation at any time, offering both low noise and low power operation when they are needed.

OPERATION

Buck-Boost Regulator Soft-Start Operation

Soft-start is accomplished by gradually increasing the reference voltage input to the error amplifier over a 0.5ms (typical) period. This limits transient inrush currents during start-up because the output voltage is always "in regulation." Ramping the reference voltage input also limits the rate of increase in the V_{C3} voltage which helps minimize output overshoot during start-up. A soft-start cycle occurs whenever the buck-boost is enabled, or after a fault condition has occurred (thermal shutdown or UVLO). A soft-start cycle is not triggered by changing operating modes. This allows seamless operation when transitioning between Burst Mode operation and PWM mode.

Low Supply Operation

The LTC3556 incorporates an undervoltage lockout circuit on V_{OUT} (connected to V_{IN3}) which shuts down the buck-boost regulator when V_{OUT} drops below 2.6V. This UVLO prevents unstable operation.

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CLPROG Resistor and Capacitor

As described in the High Efficiency Switching PowerPath Controller section, the resistor on the CLPROG pin determines the average input current limit when the switching regulator is set to either the 1x mode (USB 100mA), the 5x mode (USB 500mA) or the 10x mode. The input current will be comprised of two components, the current that is used to drive V_{OUT} and the quiescent current of the switching regulator. To ensure that the USB specification is strictly met, both components of input current should be considered. The Electrical Characteristics table gives values for quiescent currents in either setting as well as current limit programming accuracy. To get as close to the 500mA or 100mA specifications as possible, a 1% resistor should be used. Recall that $I_{VBUS} = I_{VBUSQ} + V_{CLPROG}/R_{CLPPROG} \bullet (h_{CLPROG} +1)$.

An averaging capacitor or an R-C combination is required in parallel with the CLPROG resistor so that the switching regulator can determine the average input current. This network also provides the dominant pole for the feedback loop when current limit is reached. To ensure stability, the capacitor on CLPROG should be 0.47µF or larger. Alternatively, faster transient response may be achieved with 0.1µF in series with 8.2Ω.

Choosing the PowerPath Inductor

Because the input voltage range and output voltage range of the power path switching regulator are both fairly narrow, the LTC3556 was designed for a specific inductance value of 3.3µH. Some inductors which may be suitable for this application are listed in Table 6.

Table 6. Recommended Inductors for PowerPath Controller

INDUCTOR TYPE	L (µH)	MAX I_{DC} (A)	MAX DCR (Ω)	SIZE IN mm (L × W × H)	MANUFACTURER
LPS4018	3.3	2.2	0.08	3.9 × 3.9 × 1.7	Coilcraft www.coilcraft.com
D53LC DB318C	3.3 3.3	2.26 1.55	0.034 0.070	5.0 × 5.0 × 3.0 3.8 × 3.8 × 1.8	Toko www.toko.com
WE-TPC Type M1	3.3	1.95	0.065	4.8 × 4.8 × 1.8	Würth Elektronik www.we-online.com
CDRH6D12 CDRH6D38	3.3 3.3	2.2 3.5	0.0625 0.020	6.7 × 6.7 × 1.5 7.0 × 7.0 × 4.0	Sumida www.sumida.com

V_{BUS} and V_{OUT} Bypass Capacitors

The style and value of capacitors used with the LTC3556 determine several important parameters such as regulator control-loop stability and input voltage ripple. Because the LTC3556 uses a step-down switching power supply from V_{BUS} to V_{OUT}, its input current waveform contains high frequency components. It is strongly recommended that a low equivalent series resistance (ESR) multilayer ceramic capacitor be used to bypass V_{BUS}. Tantalum and aluminum capacitors are not recommended because of their high ESR. The value of the capacitor on V_{BUS} directly controls the amount of input ripple for a given load current. Increasing the size of this capacitor will reduce the input ripple.

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To prevent large V_{OUT} voltage steps during transient load conditions, it is also recommended that a ceramic capacitor be used to bypass V_{OUT}. The output capacitor is used in the compensation of the switching regulator. At least 4µF of actual capacitance with low ESR are required on V_{OUT}. Additional capacitance will improve load transient performance and stability.

Multilayer ceramic chip capacitors typically have exceptional ESR performance. MLCCs combined with a tight board layout and an unbroken ground plane will yield very good performance and low EMI emissions.

There are several types of ceramic capacitors available, each having considerably different characteristics. For example, X7R ceramic capacitors have the best voltage and temperature stability. X5R ceramic capacitors have apparently higher packing density but poorer performance over their rated voltage and temperature ranges. Y5V ceramic capacitors have the highest packing density, but must be used with caution, because of their extreme nonlinear characteristic of capacitance vs voltage. The actual in-circuit capacitance of a ceramic capacitor should be measured with a small AC signal (ideally less than 200mV) as is expected in-circuit. Many vendors specify the capacitance vs voltage with a $1V_{RMS}$ AC test signal and as a result overstate the capacitance that the capacitor will present in the application. Using similar operating conditions as the application, the user must measure or request from the vendor the actual capacitance to determine if the selected capacitor meets the minimum capacitance that the application requires.

400mA Step-Down Switching Regulator Inductor Selection

Many different sizes and shapes of inductors are available from numerous manufacturers. Choosing the right inductor from such a large selection of devices can be overwhelming, but following a few basic guidelines will make the selection process much simpler.

The buck converters are designed to work with inductors in the range of 2.2µH to 10µH. For most applications a 4.7µH inductor is suggested for both buck regulators. Larger value inductors reduce ripple current which improves output ripple voltage. Lower value inductors result in higher ripple current and improved transient response time. To maximize efficiency, choose an inductor with a low DC resistance. For a 1.2V output, efficiency is reduced about 2% for 100mΩ series resistance at 400mA load current, and about 2% for 300mΩ series resistance at 100mA load current. Choose an inductor with a DC current rating at least 1.5 times larger than the maximum load current to ensure that the inductor does not saturate during normal operation. If output short-circuit is a possible condition, the inductor should be rated to handle the maximum peak current specified for the buck converters.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or Permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. Inductors that are very thin or have a very small volume typically have much higher core and DCR losses, and will not give the best efficiency. The choice of which style inductor to use often depends more on the price vs size, performance and any radiated EMI requirements than on what the LTC3556 requires to operate.

The inductor value also has an effect on forced burst and Burst Mode operations. Lower inductor values will cause the Burst Mode and forced Burst Mode switching frequencies to increase.

Table 7 shows several inductors that work well with the LTC3556's buck regulators. These inductors offer a good compromise in current rating, DCR and physical size. Consult each manufacturer for detailed information on their entire selection of inductors.

Table 7. Recommended Inductors for 400mA Step-Down Switching Regulators

NDUCTOR TYPE	L (µH)	MAX I_{DC} (A)	MAX DCR (Ω)	SIZE IN mm (L × W × H)	MANUFACTURER
DE2818C	4.7	1.25	0.072*	3.0 × 2.8 × 1.8	Toko www.toko.com
DE2812C	4.7	1.15	0.13*	3.0 × 2.8 × 1.2	
CDRH3D16	4.7	0.9	0.11	4.0 × 4.0 × 1.8	Sumida www.sumida.com
SD3118	4.7	1.3	0.162	3.1 × 3.1 × 1.8	Cooper www.cooperet.com
SD3112	4.7	0.8	0.246	3.1 × 3.1 × 1.2	
LPS3015	4.7	1.1	0.2	3.0 × 3.0 × 1.5	Coilcraft www.coilcraft.com

*Typical DCR

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400mA Step-Down Switching Regulator Input/Output Capacitor Selection

Low ESR (equivalent series resistance) MLCC capacitors should be used at both buck regulator outputs as well as at each buck regulator input supply (V_{IN1} and V_{IN2}). Only X5R or X7R ceramic capacitors should be used because they retain their capacitance over wider voltage and temperature ranges than other ceramic types. A 10µF output capacitor is sufficient for most applications. For good transient response and stability the output capacitor should retain at least 4µF of capacitance over operating temperature and bias voltage. Each buck regulator input supply should be bypassed with a 1µF capacitor. Consult with capacitor manufacturers for detailed information on their selection and specifications of ceramic capacitors. Many manufacturers now offer very thin (<1mm tall) ceramic capacitors ideal for use in height-restricted designs. Table 8 shows a list of several ceramic capacitor manufacturers.

Table 8. Recommended Ceramic Capacitor Manufacturers

AVX	www.avxcorp.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay Siliconix	www.vishay.com
TDK	www.tdk.com

Buck-Boost Regulator Inductor Selection

Inductor selection criteria for the buck-boost are similar to those given for the 400mA step-down switching regulators. The buck-boost converter is designed to work with inductors in the range of 1µH to 5µH. For most applications a 2.2µH inductor will suffice. Choose an inductor with a DC current rating at least 2 times larger than the maximum load current to ensure that the inductor does not saturate during normal operation. If output short circuit is a possible condition, the inductor should be rated to handle the maximum peak current specified for the buck-boost converter.

Table 9 shows several inductors that work well with the LTC3556's buck-boost regulator. These inductors offer a good compromise in current rating, DCR and physical size. Consult each manufacturer for detailed information on their entire selection of inductors.

Table 9. Recommended Inductors for Buck-Boost Regulator

INDUCTOR TYPE	L (µH)	MAX I_{DC} (A)	MAX DCR (Ω)	SIZE IN mm (L × W × H)	MANUFACTURER
LPS4018	3.3 2.2	2.2 2.5	0.08 0.07	3.9 × 3.9 × 1.7 3.9 × 3.9 × 1.7	Coilcraft www.coilcraft.com
D53LC	2.0	3.25	0.02	5.0 × 5.0 × 3.0	Toko www.toko.com
7440430022	2.2	2.5	0.028	4.8 × 4.8 × 2.8	Würth-Elektronik www.we-online.com
CDRH4D22/HP	2.2	2.4	0.044	4.7 × 4.7 × 2.4	Sumida www.sumida.com
SD14	2.0	2.56	0.045	5.2 × 5.2 × 1.45	Cooper www.cooperet.com

Buck-Boost Regulator Input/Output Capacitor Selection

Low ESR MLCC capacitors should also be used at both the buck-boost regulator output (V_{OUT3}) and the buck-boost regulator input supply (V_{IN3}). Again, only X5R or X7R ceramic capacitors should be used because they retain their capacitance over wider voltage and temperature ranges than other ceramic types. A 22µF output capacitor is sufficient for most applications. The buck-boost regulator input supply should be bypassed with a 2.2µF capacitor. Refer to Table 8 for recommended ceramic capacitor manufacturers.

Buck-Boost Regulator Output Voltage Programming

The buck-boost regulator can be programmed for output voltages greater than 2.75V and less than 5.5V. The full-scale output voltage is programmed using a resistor divider from the V_{OUT3} pin connected to the FB3 pin such that:

$$V_{OUT3} = V_{FB3}\left(\frac{R1}{R2} + 1\right)$$

where V_{FB3} ranges from 0.425V to 0.8V.

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Closing the Feedback Loop

The LTC3556 incorporates voltage mode PWM control. The control to output gain varies with operation region (buck, boost, buck-boost), but is usually no greater than 20. The output filter exhibits a double-pole response given by:

$$f_{FILTER\_POLE} = \frac{1}{2 \bullet \pi \bullet \sqrt{L \bullet C_{OUT}}} \text{ Hz}$$

where C_{OUT} is the output filter capacitor.

The output filter zero is given by:

$$f_{FILTER\_ZERO} = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}} \text{ Hz}$$

where R_{ESR} is the capacitor equivalent series resistance.

A troublesome feature in boost mode is the right-half plane zero (RHP), and is given by:

$$f_{RHPZ} = \frac{V_{IN}^2}{2 \bullet \pi \bullet I_{OUT} \bullet L \bullet V_{OUT}} \text{ Hz}$$

The loop gain is typically rolled off before the RHP zero frequency.

A simple Type I compensation network (as shown in Figure 5) can be incorporated to stabilize the loop but at the cost of reduced bandwidth and slower transient response. To ensure proper phase margin, the loop must cross unity-gain a decade before the LC double pole.

The unity-gain frequency of the error amplifier with the Type I compensation is given by:

$$f_{UG} = \frac{1}{2 \bullet \pi \bullet R1 \bullet CP1} \text{ Hz}$$

Most applications demand an improved transient response to allow a smaller output filter capacitor. To achieve a higher bandwidth, Type III compensation is required. Two zeros are required to compensate for the double-pole response. Type III compensation also reduces any V_{OUT3} overshoot at start-up.

The compensation network depicted in Figure 6 yields the transfer function:

$$\frac{V_{C3}}{V_{OUT3}} = \frac{1}{R1\,(C1+C2)} \bullet \frac{(1+sR2C2)\,[1+s(R1+R3)C3]}{s\left[1+sR2(C1||C2)\right](1+sR3C3)}$$

A Type III compensation network attempts to introduce a phase bump at a higher frequency than the LC double pole. This allows the system to cross unity gain after the LC double pole, and achieve a higher bandwidth. While attempting to cross over after the LC double pole, the system must still cross over before the boost right-half plane zero. If unity gain is not reached sufficiently before the right-half plane zero, then the –180° of phase lag from

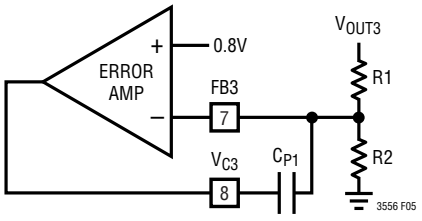

Figure 5. Error Amplifier with Type I Compensation

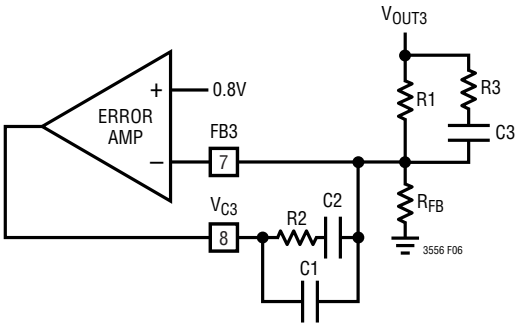

Figure 6. Error Amplifier with Type III Compensation

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the LC double pole combined with the –90° of phase lag from the right-half plane zero will result in negating the phase bump of the compensator.

The compensator zeros should be placed either before or only slightly after the LC double pole such that their positive phase contributions offset the –180° that occurs at the filter double pole. If they are placed at too low of a frequency, they will introduce too much gain to the system and the crossover frequency will be too high. The two high frequency poles should be placed such that the system crosses unity gain during the phase bump introduced by the zeros and before the boost right-half plane zero and such that the compensator bandwidth is less than the bandwidth of the error amp (typically 900kHz). If the gain of the compensation network is ever greater than the gain of the error amplifier, then the error amplifier no longer acts as an ideal op amp, and another pole will be introduced at the same point.

Recommended Type III compensation components for a 3.3V output:

R1: 324kΩ

R_{FB}: 105kΩ

C1: 10pF

R2: 15kΩ

C2: 330pF

R3: 121kΩ

C3: 33pF

C_{OUT}: 22µF

L_{OUT}: 2.2µH

Over-Programming the Battery Charger

The USB high power specification allows for up to 2.5W to be drawn from the USB port (5V×500mA). The PowerPath switching regulator transforms the voltage at V_{BUS} to just above the voltage at BAT with high efficiency, while limiting power to less than the amount programmed at CLPROG. In some cases the battery charger may be programmed (with the PROG pin) to deliver the maximum safe charging current without regard to the USB specifications. If there is insufficient current available to charge the battery at the programmed rate, the PowerPath regulator will reduce charge current until the system load on V_{OUT} is satisfied and the V_{BUS} current limit is satisfied. Programming the battery charger for more current than is available will not cause the average input current limit to be violated. It will merely allow the battery charger to make use of all available power to charge the battery as quickly as possible, and with minimal power dissipation within the battery charger.

Alternate NTC Thermistors and Biasing

The LTC3556 provides temperature qualified charging if a grounded thermistor and a bias resistor are connected to NTC. By using a bias resistor whose value is equal to the room temperature resistance of the thermistor (R25) the upper and lower temperatures are pre-programmed to approximately 40°C and 0°C, respectively (assuming a Vishay “Curve 1” thermistor).

The upper and lower temperature thresholds can be adjusted by either a modification of the bias resistor value or by adding a second adjustment resistor to the circuit. If only the bias resistor is adjusted, then either the upper or the lower threshold can be modified but not both. The other trip point will be determined by the characteristics of the thermistor. Using the bias resistor in addition to an adjustment resistor, both the upper and the lower temperature trip points can be independently programmed with the constraint that the difference between the upper and lower temperature thresholds cannot decrease. Examples of each technique follow.

NTC thermistors have temperature characteristics which are indicated on resistance-temperature conversion tables. The Vishay-Dale thermistor NTHS0603N011-N1003F, used

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in the following examples, has a nominal value of 100k and follows the Vishay "Curve 1" resistance-temperature characteristic.

In the explanation below, the following notation is used.

R25 = Value of the thermistor at 25°C

$R_{NTC|COLD}$ = Value of thermistor at the cold trip point

$R_{NTC|HOT}$ = Value of thermistor at the hot trip point

r_{COLD} = Ratio of $R_{NTC|COLD}$ to R25

r_{HOT} = Ratio of $R_{NTC|COLD}$ to R25

R_{NOM} = Primary thermistor bias resistor (see Figure 7a)
R1 = Optional temperature range adjustment resistor (see Figure 7b)

The trip points for the LTC3556's temperature qualification are internally programmed at 0.349 • V_{BUS} for the hot threshold and 0.765 • V_{BUS} for the cold threshold.

Therefore, the hot trip point is set when:

$$\frac{R_{NTC|HOT}}{R_{NOM}+R_{NTC|HOT}} \bullet V_{BUS} = 0.349 \bullet V_{BUS}$$

and the cold trip point is set when:

$$\frac{R_{NTC|COLD}}{R_{NOM}+R_{NTC|COLD}} \bullet V_{BUS} = 0.765 \bullet V_{BUS}$$

Solving these equations for $R_{NTC|COLD}$ and $R_{NTC|HOT}$ results in the following:

$R_{NTC|HOT} = 0.536 \bullet R_{NOM}$

and

$R_{NTC|COLD} = 3.25 \bullet R_{NOM}$

By setting R_{NOM} equal to R25, the above equations result in $r_{HOT} = 0.536$ and $r_{COLD} = 3.25$. Referencing these ratios to the Vishay Resistance-Temperature Curve 1 chart gives a hot trip point of about 40°C and a cold trip point of about 0°C. The difference between the hot and cold trip points is approximately 40°C.

By using a bias resistor, R_{NOM}, different in value from R25, the hot and cold trip points can be moved in either direction. The temperature span will change somewhat due to the nonlinear behavior of the thermistor. The following equations can be used to easily calculate a new value for the bias resistor:

$$R_{NOM} = \frac{r_{HOT}}{0.536} \bullet R25$$

$$R_{NOM} = \frac{r_{COLD}}{3.25} \bullet R25$$

where r_{HOT} and r_{COLD} are the resistance ratios at the desired hot and cold trip points. Note that these equations are linked. Therefore, only one of the two trip points can be chosen, the other is determined by the default ratios designed in the IC. Consider an example where a 60°C hot trip point is desired.

From the Vishay Curve 1 R-T characteristics, r_{HOT} is 0.2488 at 60°C. Using the above equation, R_{NOM} should be set to 46.4k. With this value of R_{NOM}, the cold trip point is about 16°C. Notice that the span is now 44°C rather than the previous 40°C. This is due to the decrease in "temperature gain" of the thermistor as absolute temperature increases.

The upper and lower temperature trip points can be independently programmed by using an additional bias resistor as shown in Figure 7b. The following formulas can be used to compute the values of R_{NOM} and R1:

$$R_{NOM} = \frac{r_{COLD} - r_{HOT}}{2.714} \bullet R25$$

$$R1 = 0.536 \bullet R_{NOM} - r_{HOT} \bullet R25$$

For example, to set the trip points to 0°C and 45°C with a Vishay Curve 1 thermistor choose:

$$R_{NOM} = \frac{3.266 - 0.4368}{2.714} \bullet 100k = 104.2k$$

The nearest 1% value is 105k.

$R1 = 0.536 \bullet 105k - 0.4368 \bullet 100k = 12.6k$

The nearest 1% value is 12.7k. The final solution is shown in Figure 7b and results in an upper trip point of 45°C and a lower trip point of 0°C.

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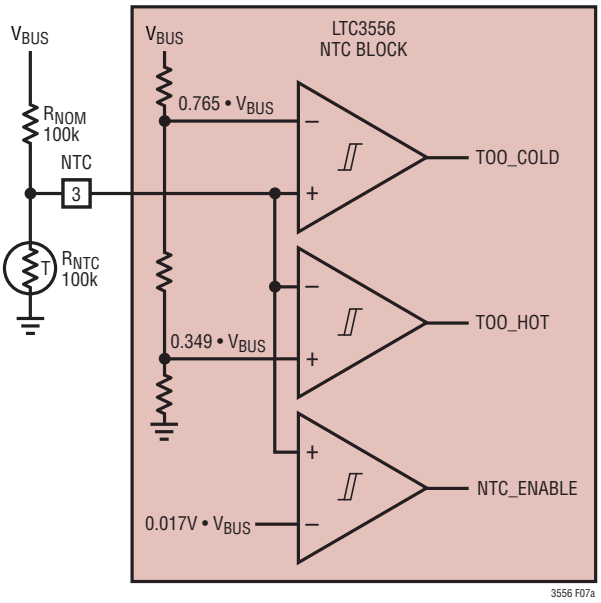
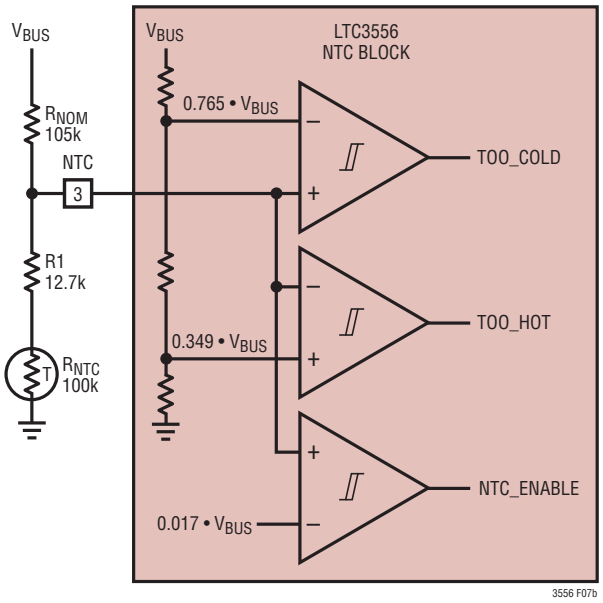


(7a)



(7b)

Figure 7. NTC Circuits

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USB Inrush Limiting

When a USB cable is plugged into a portable product, the inductance of the cable and the high-Q ceramic input capacitor form an L-C resonant circuit. If the cable does not have adequate mutual coupling or if there is not much impedance in the cable, it is possible for the voltage at the input of the product to reach as high as twice the USB voltage (~10V) before it settles out. To prevent excessive voltage from damaging the LTC3556 during a hot insertion, it is best to have a low voltage coefficient capacitor at the V_{BUS} pin to the LTC3556. This is achievable by selecting an MLCC capacitor that has a higher voltage rating than that required for the application. For example, a 16V, X5R, 10µF capacitor in a 1206 case would be a more conservative choice than a 6.3V, X5R, 10µF capacitor in a smaller 0805 case. The size of the input overshoot will be determined by the "Q" of the resonant tank circuit formed by C_{IN} and the input lead inductance. It is recommended to measure the input ringing with the selected components to verify compliance with the Absolute Maximum specifications.

Alternatively, the following soft connect circuit (Figure 8) can be employed. In this circuit, capacitor C1 holds MP1 off when the cable is first connected. Eventually C1 begins to charge up to the USB input voltage applying increasing gate support to MP1. The long time constant of R1 and C1 prevent the current from building up in the cable too fast thus dampening out any resonant overshoot.

Printed Circuit Board Layout Considerations

In order to be able to deliver maximum current under all conditions, it is critical that the Exposed Pad on the backside of the LTC3556 package be soldered to the PC board ground. Failure to make thermal contact between the Exposed Pad on the backside of the package and the copper board will result in higher thermal resistances.

Furthermore, due to its high frequency switching circuitry, it is imperative that the input capacitors, inductors and output capacitors be as close to the LTC3556 as possible and that there be an unbroken ground plane under the LTC3556 and all of its external high frequency components. High frequency currents such as the V_{BUS}, V_{IN1}, V_{IN2} and V_{IN3} currents on the LTC3556, tend to find their way along the ground plane in a myriad of paths ranging from directly back to a mirror path beneath the incident path on the top of the board. If there are slits or cuts in the ground plane due to other traces on that layer, the current will be forced to go around the slits. If high frequency currents are not allowed to flow back through their natural least-area path, excessive voltage will build up and radiated emissions will occur. There should be a group of vias under the grounded backside of the package leading directly down to an internal ground plane. To minimize parasitic inductance, the ground plane should be on the second layer of the PC board.

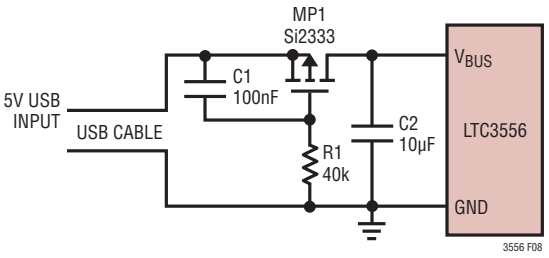

Figure 8. USB Soft Connect Circuit

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The GATE pin for the external ideal diode controller has extremely limited drive current. Care must be taken to minimize leakage to adjacent PC board traces. 100nA of leakage from this pin will introduce an offset to the 15mV ideal diode of approximately 10mV. To minimize leakage, the trace can be guarded on the PC board by surrounding it with V_{OUT} connected metal, which should generally be less that one volt higher than GATE.

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3556.

1. Are the capacitors at V_{BUS}, V_{IN1}, V_{IN2} and V_{IN3} as close as possible to the LTC3556? These capacitors provide the AC current to the internal power MOSFETs and their drivers. Minimizing inductance from these capacitors to the LTC3556 is a top priority.
2. Are C_{OUT} and L1 closely connected? The (–) plate of C_{OUT} returns current to the GND plane, and then back to C_{IN}.
3. Keep sensitive components away from the SW pins.

Battery Charger Stability Considerations

The LTC3556's battery charger contains both a constant-voltage and a constant-current control loop. The constant-voltage loop is stable without any compensation when a battery is connected with low impedance leads. Excessive lead length, however, may add enough series inductance to require a bypass capacitor of at least 1µF from BAT to GND. Furthermore, when the battery is disconnected, a 100µF OSCON B6 capacitor in series with a 0Ω jumper from BAT to GND is required to keep ripple voltage low.

High value, low ESR multilayer ceramic chip capacitors reduce the constant-voltage loop phase margin, possibly resulting in instability. Ceramic capacitors up to 22µF may be used in parallel with a battery, but larger ceramics should be decoupled with 0.2Ω to 1Ω of series resistance.

In constant-current mode, the PROG pin is in the feedback loop rather than the battery voltage. Because of the additional pole created by any PROG pin capacitance, capacitance on this pin must be kept to a minimum. With no additional capacitance on the PROG pin, the battery charger is stable with program resistor values as high as 25k. However, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz. Therefore, if the PROG pin has a parasitic capacitance, C_{PROG}, the following equation should be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq \frac{1}{2\pi \bullet 100kHz \bullet C_{PROG}}$$

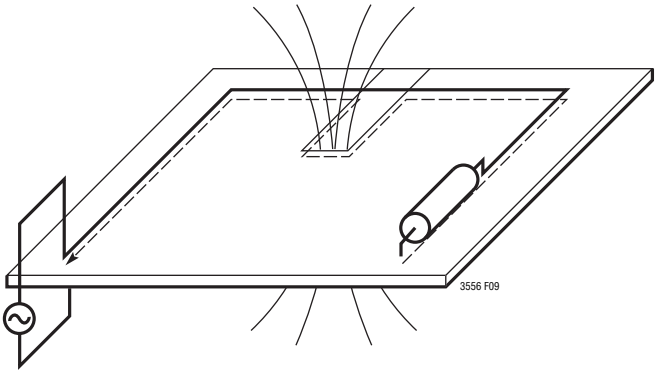
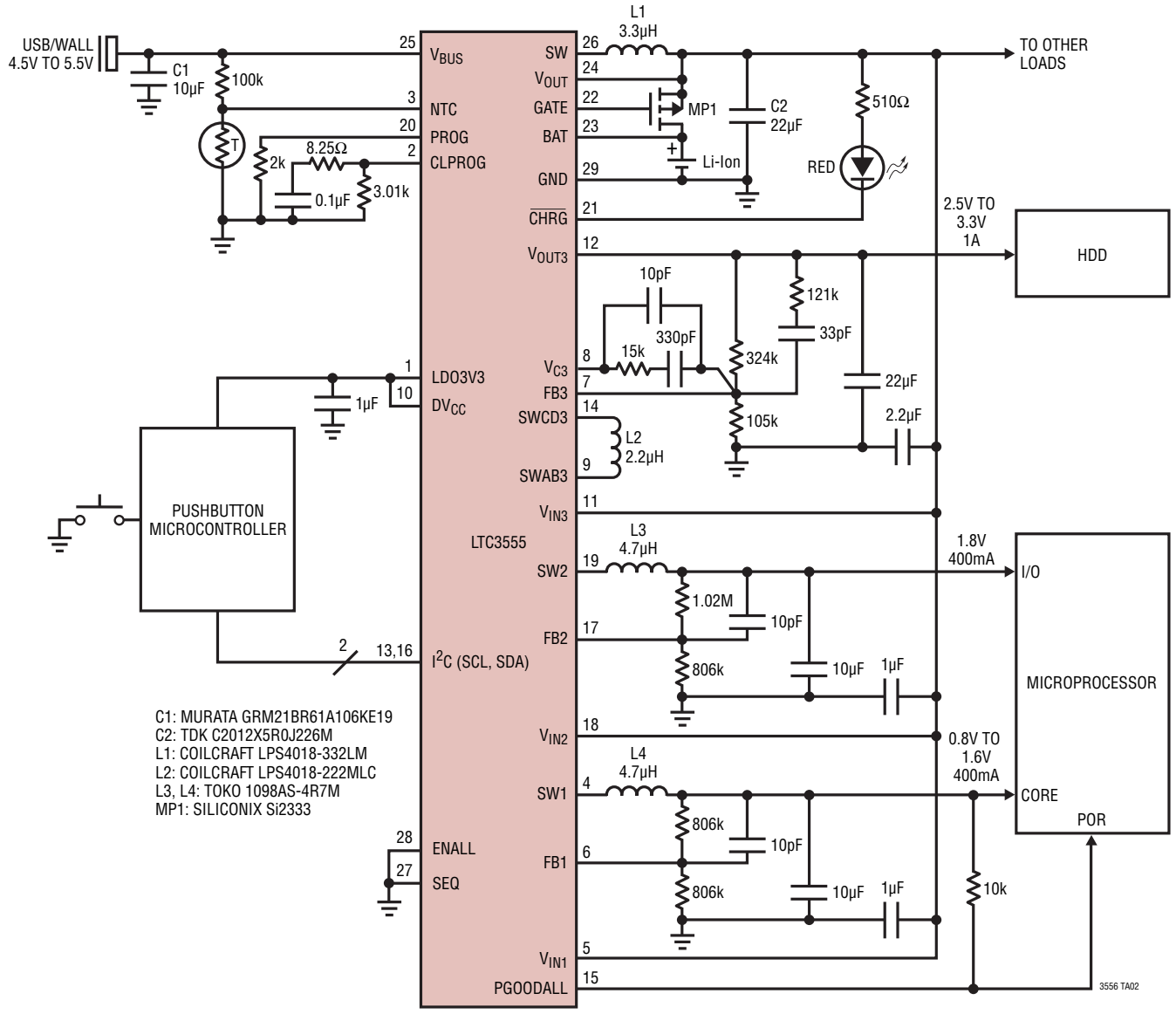


Figure 9. Higher Frequency Ground Currents Follow Their Incident Path. Slices in the Ground Plane Cause High Voltage and Increased Emissions

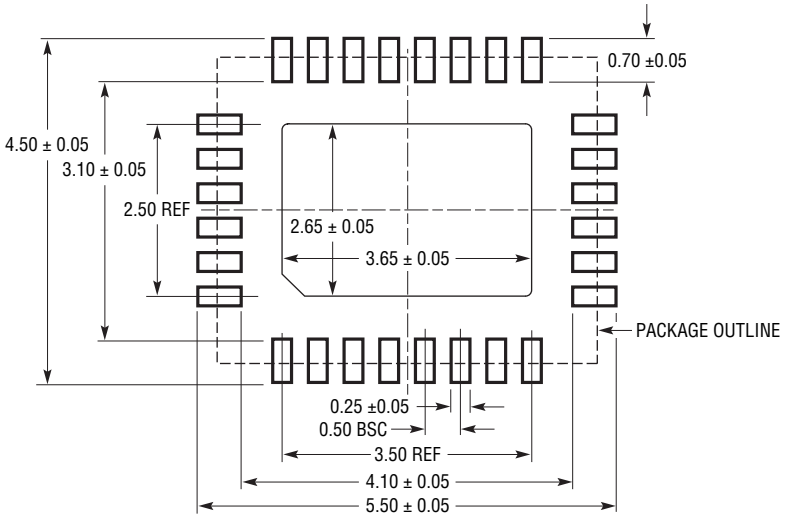
TYPICAL APPLICATION

Watchdog Microcontroller Operation

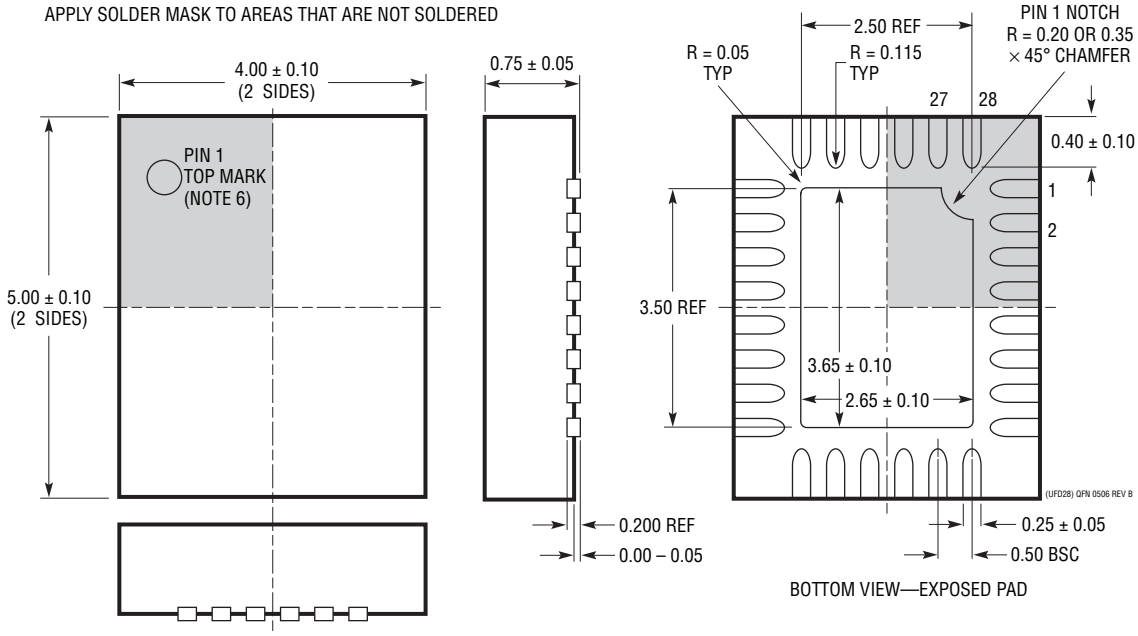


PACKAGE DESCRIPTION

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

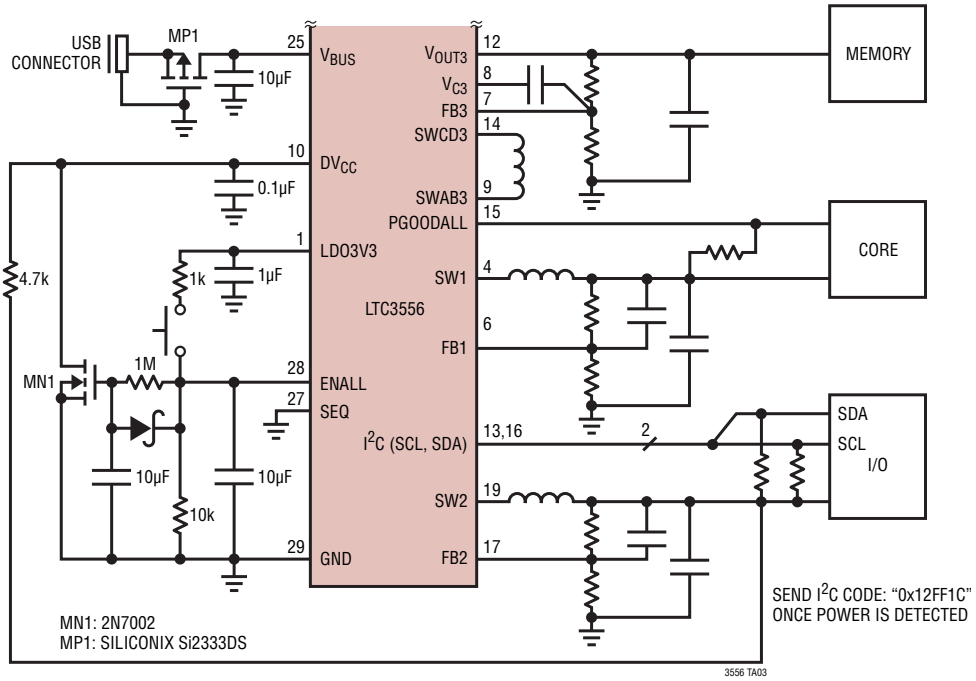


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Pushbutton Start with Automatic Sequencing, Reverse Input Voltage Protection and 10 Second Push and Hold Hard Shutdown



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3455	Dual DC/DC Converter with USB Power Manager and Li-Ion Battery Charger	Seamless Transition Between Input Power Sources: Li-Ion Battery, USB and 5V Wall Adapter. Two High Efficiency DC/DC Converters: Up to 96%. Full Featured Li-Ion Battery Charger with Accurate USB Current Limiting (500mA/100mA). Pin Selectable Burst Mode Operation. Hot Swap™ Output for SDIO and Memory Cards. 24-Lead 4mm × 4mm QFN Package
LTC3456	2-Cell, Multi-Output DC/DC Converter with USB Power Manager	Seamless Transition Between 2-Cell Battery, USB and AC Wall Adapter Input Power Sources. Main Output: Fixed 3.3V Output, Core Output: Adjustable from 0.8V to $V_{BATT(MIN)}$. Hot Swap Output for Memory Cards. Power Supply Sequencing: Main and Hot Swap Accurate USB Current Limiting. High Frequency Operation: 1MHz. High Efficiency: Up to 92%. 24-Lead 4mm × 4mm QFN Package
LTC3552	Standalone Linear Li-Ion Battery Charger with Adjustable Output Dual Synchronous Buck Converter	Synchronous Buck Converter, Efficiency: >90%, Adjustable Outputs at 800mA and 400mA, Charge Current Programmable up to 950mA, USB Compatible, 16-Lead 5mm × 3mm DFN Package
LTC3555/ LTC3555-1	High Efficiency USB Power Manager Plus Triple Step-Down DC/DC	Maximizes Available Power from USB Port, Bat-Track, "Instant On" Operation, 1.5A Max Charge Current, 180mΩ Ideal Diode with <50mΩ Option, 3.3V/25mA Always-On LDO, Three Synchronous Buck Regulators (400mA/400mA/1A), 4mm × 5mm QFN28 Package
LTC3557/ LTC3557-1	Linear USB Power Manager with Li-Ion/ Polymer Charger and Triple Synchronous Buck Converter	Complete Multifunction ASSP: Linear Power Manager and Three Buck Regulators Charge Current Programmable up to 1.5A from Wall Adapter Input, Thermal Regulation, Synchronous Buck Efficiency: >95%, ADJ Outputs: 0.8V to 3.6V at 400mA/400mA/600mA Bat-Track Adaptive Output Control, 200mΩ Ideal Diode, 4mm × 4mm QFN28 Package
LTC4085	Linear USB Power Manager with Ideal Diode Controller and Li-Ion Charger	Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 200mΩ Ideal Diode with <50mΩ option, 4mm × 3mm DFN14 Package
LTC4088/ LTC4088-1	High Efficiency USB Power Manager and Battery Charger	Maximizes Available Power from USB Port, Bat-Track, "Instant On" Operation, 1.5A Max Charge Current, 180mΩ Ideal Diode with <50mΩ Option, 3.3V/25mA Always-On LDO, 4mm × 3mm DFN14 Package

Hot Swap is a trademark of Linear Technology Corporation.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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