LTC2485

24-Bit ΔΣ ADC with Easy Drive Input Current Cancellation and I^2C Interface

FEATURES

- **Easy Drive™ Technology Enables Rail-to-Rail Inputs with Zero Differential Input Current**
- **Directly Digitizes High Impedance Sensors with Full Accuracy**
- **Integrated Temperature Sensor**
- **GND to V_{CC} Input/Reference Common Mode Range**
- **2-Wire I^2C Interface**
- Programmable 50Hz, 60Hz or Simultaneous 50Hz/60Hz Rejection Mode
- 2ppm (0.25LSB) INL, No Missing Codes
- 1ppm Offset and 15ppm Full-Scale Error
- Selectable 2x Speed Mode
- No Latency: Digital Filter Settles in a Single Cycle
- Single Supply 2.7V to 5.5V Operation
- Internal Oscillator
- Six Addresses Available and One Global Address for Synchronization
- Available in a Tiny (3mm × 3mm) 10-Lead DFN Package

APPLICATIONS

- Direct Sensor Digitizer
- Weight Scales
- Direct Temperature Measurement
- Strain Gauge Transducers
- Instrumentation
- Industrial Process Control
- DVMs and Meters

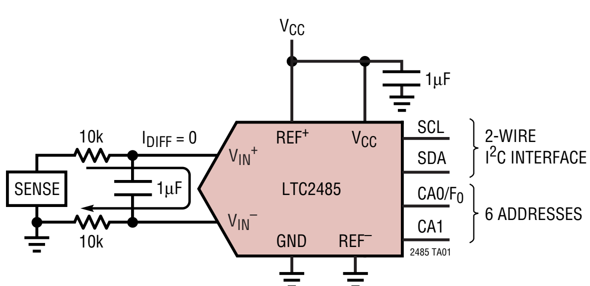
DESCRIPTION

The LTC®2485 combines a 24-bit plus sign No Latency ΔΣ™ analog-to-digital converter with patented Easy Drive technology and I^2C digital interface. The patented sampling scheme eliminates dynamic input current errors and the shortcomings of on-chip buffering through automatic cancellation of differential input current. This allows large external source impedances and input signals, with rail-to-rail input range to be directly digitized while maintaining exceptional DC accuracy.

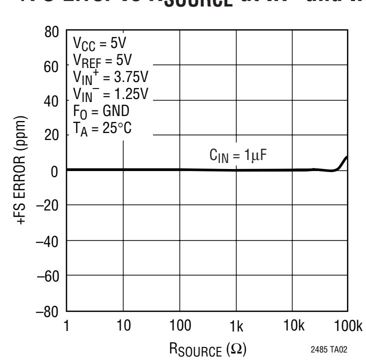
The LTC2485 includes on-chip temperature sensor and an oscillator. The LTC2485 can be configured through an I^2C interface to measure an external signal or internal temperature sensor and reject line frequencies. 50Hz, 60Hz or simultaneous 50Hz/60Hz line frequency rejection can be selected as well as a 2x speed-up mode.

The LTC2485 allows a wide common mode input range (0V to V_{CC}) independent of the reference voltage. The reference can be as low as 100mV or can be tied directly to V_{CC}. The LTC2485 includes an on-chip trimmed oscillator eliminating the need for external crystals or oscillators. Absolute accuracy and low drift are automatically maintained through continuous, transparent, offset and full-scale calibration.

TYPICAL APPLICATION



+FS Error vs R_{SOURCE} at IN^+ and IN^-



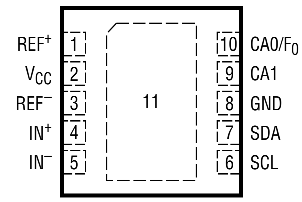
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND .... −0.3V to 6V
Analog Input Voltage to GND .... −0.3V to (V_{CC} + 0.3V)
Reference Input Voltage to GND .. −0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND .... −0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND ..... −0.3V to (V_{CC} + 0.3V)
Operating Temperature Range
LTC2485C .... 0°C to 70°C
LTC2485I .... −40°C to 85°C
Storage Temperature Range .... −65°C to 125°C

PACKAGE/ORDER INFORMATION

TOP VIEW



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS GND
MUST BE SOLDERED TO PCB

ORDER PART NUMBER	DD PART MARKING*
LTC2485CDD LTC2485IDD	LBST

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.
*The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS (NORMAL SPEED)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	$0.1 \le V_{REF} \le V_{CC}$, $-FS \le V_{IN} \le +FS$ (Note 5)	●	24			Bits
Integral Nonlinearity	$5V \le V_{CC} \le 5.5V$, V_{REF} = 5V, $V_{IN(CM)}$ = 2.5V (Note 6) $2.7V \le V_{CC} \le 5.5V$, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V (Note 6)	●		2 1	10	ppm of V_{REF} ppm of V_{REF}
Offset Error	$2.5V \le V_{REF} \le V_{CC}$, $GND \le IN^+ = IN^- \le V_{CC}$ (Note 13)	●		0.5	2.5	µV
Offset Error Drift	$2.5V \le V_{REF} \le V_{CC}$, $GND \le IN^+ = IN^- \le V_{CC}$			10		nV/°C
Positive Full-Scale Error	$2.5V \le V_{REF} \le V_{CC}$, $IN^+ = 0.75V_{REF}$, $IN^- = 0.25V_{REF}$	●			25	ppm of V_{REF}
Positive Full-Scale Error Drift	$2.5V \le V_{REF} \le V_{CC}$, $IN^+ = 0.75V_{REF}$, $IN^- = 0.25V_{REF}$			0.1		ppm of V_{REF}/°C
Negative Full-Scale Error	$2.5V \le V_{REF} \le V_{CC}$, $IN^- = 0.75V_{REF}$, $IN^+ = 0.25V_{REF}$	●			25	ppm of V_{REF}
Negative Full-Scale Error Drift	$2.5V \le V_{REF} \le V_{CC}$, $IN^- = 0.75V_{REF}$, $IN^+ = 0.25V_{REF}$			0.1		ppm of V_{REF}/°C
Total Unadjusted Error	$5V \le V_{CC} \le 5.5V$, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V (Note 6) $5V \le V_{CC} \le 5.5V$, V_{REF} = 5V, $V_{IN(CM)}$ = 2.5V (Note 6) $2.7V \le V_{CC} \le 5.5V$, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V (Note 6)			15 15 15		ppm of V_{REF} ppm of V_{REF} ppm of V_{REF}
Output Noise	$5V \le V_{CC} \le 5.5V$, V_{REF} = 5V, $GND \le IN^- = IN^+ \le V_{CC}$ (Note 12)			0.6		$µV_{RMS}$
Internal PTAT Signal	T_A = 27°C			420		mV
Internal PTAT Temperature Coefficient				1.4		mV/°C

ELECTRICAL CHARACTERISTICS (2x SPEED)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	$0.1 \le V_{REF} \le V_{CC}$, $-FS \le V_{IN} \le +FS$ (Note 5)	●	24			Bits
Integral Nonlinearity	$5V \le V_{CC} \le 5.5V$, $V_{REF} = 5V$, $V_{IN(CM)} = 2.5V$ (Note 6) $2.7V \le V_{CC} \le 5.5V$, $V_{REF} = 2.5V$, $V_{IN(CM)} = 1.25V$ (Note 6)	●		2 1	10	ppm of V_{REF}
Offset Error	$2.5V \le V_{REF} \le V_{CC}$, $GND \le IN^+ = IN^- \le V_{CC}$ (Note 13)	●		0.5	2	mV
Offset Error Drift	$2.5V \le V_{REF} \le V_{CC}$, $GND \le IN^+ = IN^- \le V_{CC}$			100		nV/°C
Positive Full-Scale Error	$2.5V \le V_{REF} \le V_{CC}$, $IN^+ = 0.75V_{REF}$, $IN^- = 0.25V_{REF}$	●			25	ppm of V_{REF}
Positive Full-Scale Error Drift	$2.5V \le V_{REF} \le V_{CC}$, $IN^+ = 0.75V_{REF}$, $IN^- = 0.25V_{REF}$			0.1		ppm of V_{REF}/°C
Negative Full-Scale Error	$2.5V \le V_{REF} \le V_{CC}$, $IN^- = 0.75V_{REF}$, $IN^+ = 0.25V_{REF}$	●			25	ppm of V_{REF}
Negative Full-Scale Error Drift	$2.5V \le V_{REF} \le V_{CC}$, $IN^- = 0.75V_{REF}$, $IN^+ = 0.25V_{REF}$			0.1		ppm of V_{REF}/°C
Output Noise	$5V \le V_{CC} \le 5.5V$, $V_{REF} = 5V$, $GND \le IN^- = IN^+ \le V_{CC}$			0.84		μV_{RMS}

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Common Mode Rejection DC	$2.5V \le V_{REF} \le V_{CC}$, $GND \le IN^- = IN^+ \le V_{CC}$ (Note 5)	●	140			dB
Input Common Mode Rejection 50Hz ±2%	$2.5V \le V_{REF} \le V_{CC}$, $GND \le IN^- = IN^+ \le V_{CC}$ (Note 5)	●	140			dB
Input Common Mode Rejection 60Hz ±2%	$2.5V \le V_{REF} \le V_{CC}$, $GND \le IN^- = IN^+ \le V_{CC}$ (Note 5)	●	140			dB
Input Normal Mode Rejection 50Hz ±2%	$2.5V \le V_{REF} \le V_{CC}$, $GND \le IN^- = IN^+ \le V_{CC}$ (Notes 5, 7)	●	110	120		dB
Input Normal Mode Rejection 60Hz ±2%	$2.5V \le V_{REF} \le V_{CC}$, $GND \le IN^- = IN^+ \le V_{CC}$ (Notes 5, 8)	●	110	120		dB
Input Normal Mode Rejection 50Hz/60Hz ±2%	$2.5V \le V_{REF} \le V_{CC}$, $GND \le IN^- = IN^+ \le V_{CC}$ (Notes 5, 9)	●	87			dB
Reference Common Mode Rejection DC	$2.5V \le V_{REF} \le V_{CC}$, $GND \le IN^- = IN^+ \le V_{CC}$ (Note 5)	●	120	140		dB
Power Supply Rejection DC	$V_{REF} = 2.5V$, $IN^- = IN^+ = GND$			120		dB
Power Supply Rejection, 50Hz ±2%	$V_{REF} = 2.5V$, $IN^- = IN^+ = GND$ (Notes 7, 9)			120		dB
Power Supply Rejection, 60Hz ±2%	$V_{REF} = 2.5V$, $IN^- = IN^+ = GND$ (Notes 8, 9)			120		dB

ANALOG INPUT AND REFERENCE

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN^+	Absolute/Common Mode IN^+ Voltage			GND – 0.3V		V_{CC} + 0.3V	V
IN^-	Absolute/Common Mode IN^- Voltage			GND – 0.3V		V_{CC} + 0.3V	V
FS	Full Scale of the Differential Input ($IN^+ - IN^-$)		●	$0.5V_{REF}$			V
LSB	Least Significant Bit of the Output Code		●	$FS/2^{24}$			
V_{IN}	Input Differential Voltage Range ($IN^+ - IN^-$)		●	–FS		+FS	V
V_{REF}	Reference Voltage Range ($REF^+ - REF^-$)		●	0.1		V_{CC}	V

ANALOG INPUT AND REFERENCE

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_S (IN^+)	IN^+ Sampling Capacitance				11		pF
C_S (IN^-)	IN^- Sampling Capacitance				11		pF
C_S (V_{REF})	V_{REF} Sampling Capacitance				11		pF
I_{DC_LEAK} (IN^+)	IN^+ DC Leakage Current	Sleep Mode, IN^+ = GND	●	–10	1	10	nA
I_{DC_LEAK} (IN^-)	IN^- DC Leakage Current	Sleep Mode, IN^- = GND	●	–10	1	10	nA
I_{DC_LEAK} (V_{REF})	REF^+, REF^- DC Leakage Current	Sleep Mode, V_{REF} = V_{CC}	●	–100	1	100	nA

I²C DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	$0.7V_{CC}$			V
V_{IL}	Low Level Input Voltage		●			$0.3V_{CC}$	V
$V_{IL(CA1)}$	Low Level Input Voltage for Address Pin		●			$0.05V_{CC}$	V
$V_{IH(CA0/F0,CA1)}$	High Level Input Voltage for Address Pins		●	$0.95V_{CC}$			V
R_{INH}	Resistance from CA0/F_0,CA1 to V_{CC} to Set Chip Address Bit to 1		●			10	kΩ
R_{INL}	Resistance from CA1 to GND to Set Chip Address Bit to 0		●			10	kΩ
R_{INF}	Resistance from CA0/F_0, CA1 to V_{CC} or GND to Set Chip Address Bit to Float		●	2			MΩ
I_I	Digital Input Current		●	–10		10	µA
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	(Note 5)		$0.05V_{CC}$			V
V_{OL}	Low Level Output Voltage SDA	I = 3mA	●			0.4	V
t_{OF}	Output Fall Time from V_{IHMIN} to V_{ILMAX}	Bus Load C_B 10pF to 400pF (Note 14)	●	$20+0.1C_B$		250	ns
t_{SP}	Input Spike Suppression		●			50	ns
I_{IN}	Input Leakage	$0.1V_{CC} \le V_{IN} \le V_{CC}$	●			1	µA
C_I	Capacitance for Each I/O Pin		●	10			pF
C_B	Capacitance Load for Each Bus Line		●			400	pF
C_{CAX}	External Capacitive Load on Chip Address Pins (CA0/F_0,CA1) for Valid Float		●			10	pF
$V_{IH(EXT,OSC)}$	High Level CA0/F_0 External Oscillator	$2.7V \le V_{CC} < 5.5V$	●	V_{CC} – 0.5V			V
$V_{IL(EXT,OSC)}$	Low Level CA0/F_0 External Oscillator	$2.7V \le V_{CC} < 5.5V$	●			0.5	V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current	Conversion Mode (Note 11) Sleep Mode (Note 11)	● ●		160 1	250 2	µA µA

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	10		4000	kHz
t_{HEO}	External Oscillator High Period		●	0.125		100	µs
t_{LEO}	External Oscillator Low Period		●	0.125		100	µs
t_{CONV_1}	Conversion Time for 1x Speed Mode	50Hz Mode	●	157.2	160.3	163.5	ms
		60Hz Mode	●	131.0	133.6	136.3	ms
		Simultaneous 50Hz/60Hz Mode	●	144.1	146.9	149.9	ms
		External Oscillator (Note 10)	●		$41036/f_{EOSC}$		ms
t_{CONV_2}	Conversion Time for 2x Speed Mode	50Hz Mode	●	78.7	80.3	81.9	ms
		60Hz Mode	●	65.6	66.9	68.2	ms
		Simultaneous 50Hz/60Hz Mode	●	72.2	73.6	75.1	ms
		External Oscillator (Note 10)	●		$20556/f_{EOSC}$		ms

I²C TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 15)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(SDA)}$	Hold Time (Repeated) START Condition		●	0.6			µs
t_{LOW}	LOW Period of the SCL Clock Pin		●	1.3			µs
t_{HIGH}	HIGH Period of the SCL Clock Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated START Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time for Both SDA and SCL Signals	(Note 14)	●	$20+0.1C_B$		300	ns
t_f	Fall Time for Both SDA and SCL Signals	(Note 14)	●	$20+0.1C_B$		300	ns
$t_{SU(STO)}$	Set-Up Time for STOP Condition		●	0.6			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7V to 5.5V unless otherwise specified.

$V_{REF} = REF^+ - REF^-$, $V_{REFCM} = (REF^+ + REF^-)/2$, $FS = 0.5V_{REF}$;
$V_{IN} = IN^+ - IN^-$, $V_{INCM} = (IN^+ + IN^-)/2$.

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: 50Hz mode (internal oscillator) or f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: 60Hz mode (internal oscillator) or f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz mode (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The external oscillator is connected to the CA0/F_0 pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 11: The converter uses the internal oscillator.

Note 12: The output noise includes the contribution of the internal calibration operations.

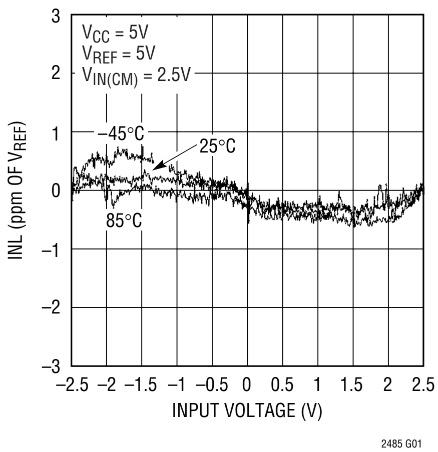
Note 13: Guaranteed by design and test correlation.

Note 14: C_B = capacitance of one bus line in pF.

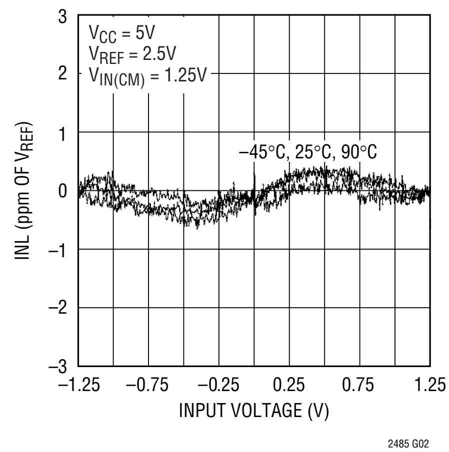
Note 15: All values refer to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

TYPICAL PERFORMANCE CHARACTERISTICS

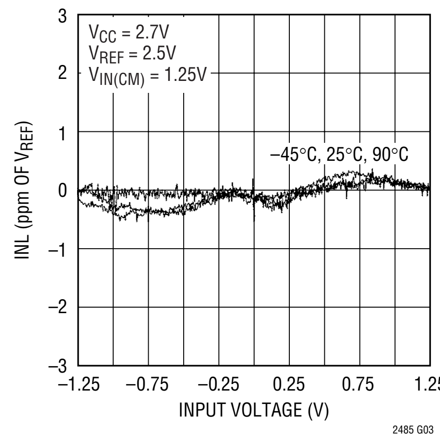
Integral Nonlinearity (V_{CC} = 5V, V_{REF} = 5V)



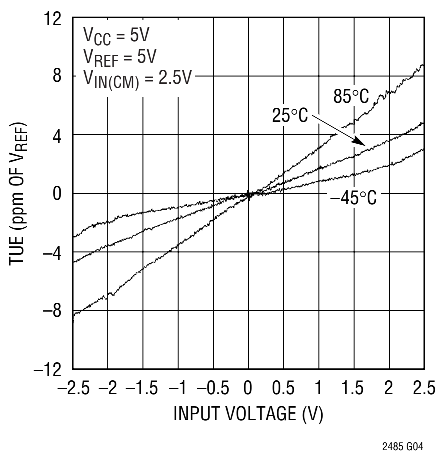
Integral Nonlinearity (V_{CC} = 5V, V_{REF} = 2.5V)



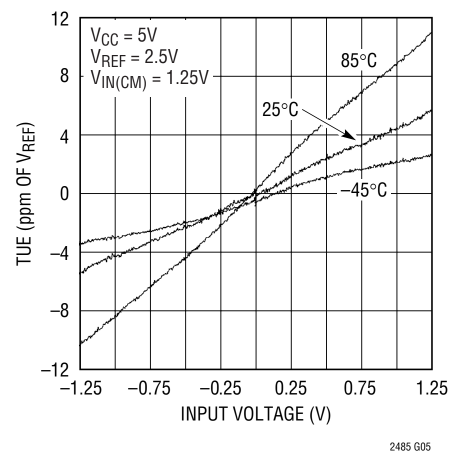
Integral Nonlinearity (V_{CC} = 2.7V, V_{REF} = 2.5V)



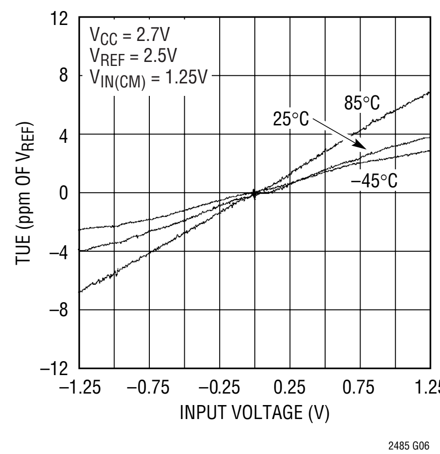
Total Unadjusted Error (V_{CC} = 5V, V_{REF} = 5V)



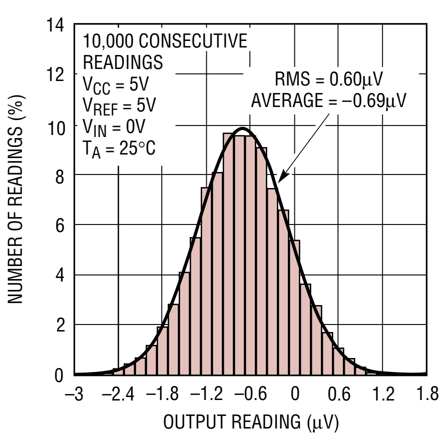
Total Unadjusted Error (V_{CC} = 5V, V_{REF} = 2.5V)



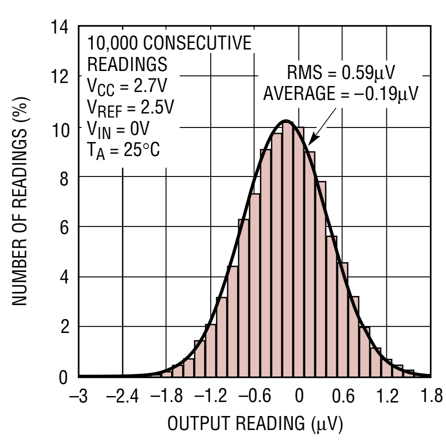
Total Unadjusted Error (V_{CC} = 2.7V, V_{REF} = 2.5V)



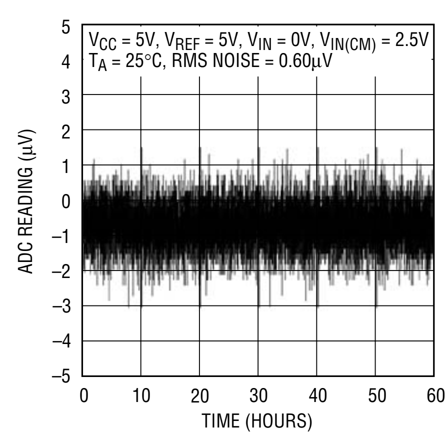
Noise Histogram (6.8sps)



Noise Histogram (7.5sps)

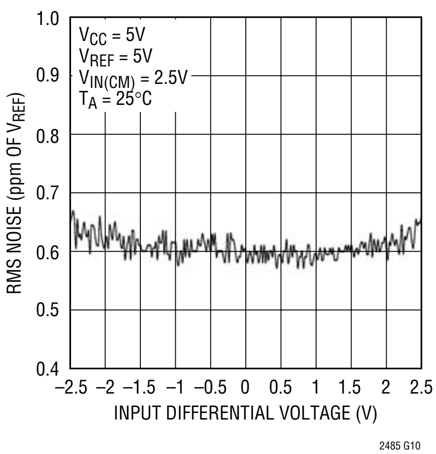


Long-Term ADC Readings

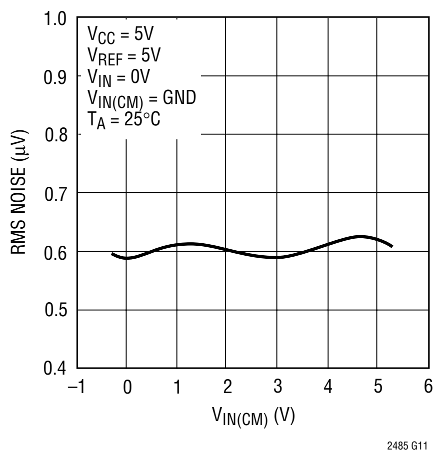


TYPICAL PERFORMANCE CHARACTERISTICS

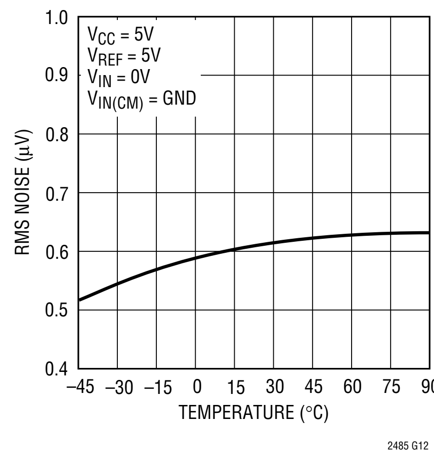
RMS Noise vs Input Differential Voltage



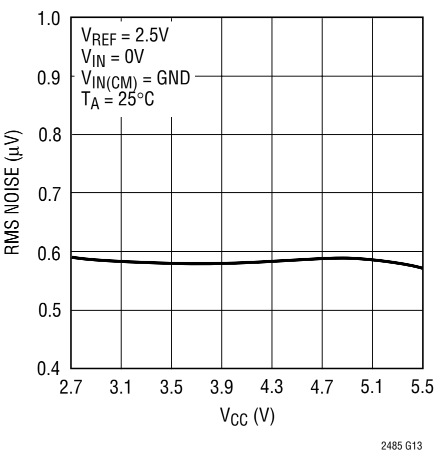
RMS Noise vs $V_{IN(CM)}$



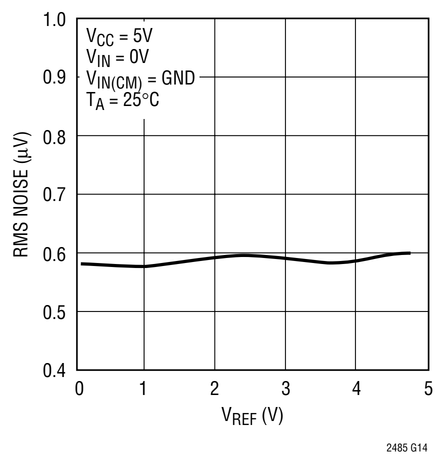
RMS Noise vs Temperature (T_A)



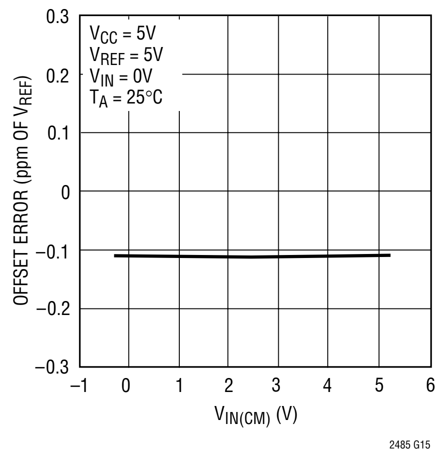
RMS Noise vs V_{CC}



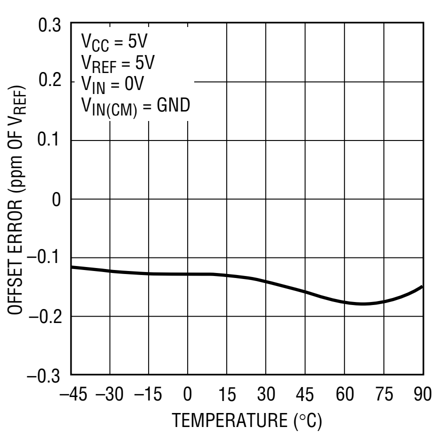
RMS Noise vs V_{REF}



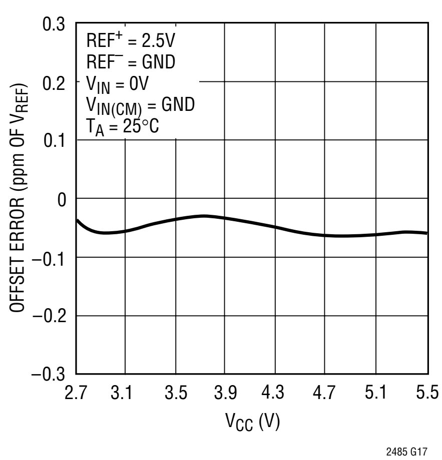
Offset Error vs $V_{IN(CM)}$



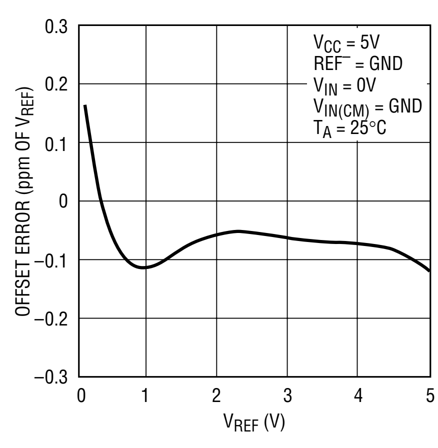
Offset Error vs Temperature



Offset Error vs V_{CC}

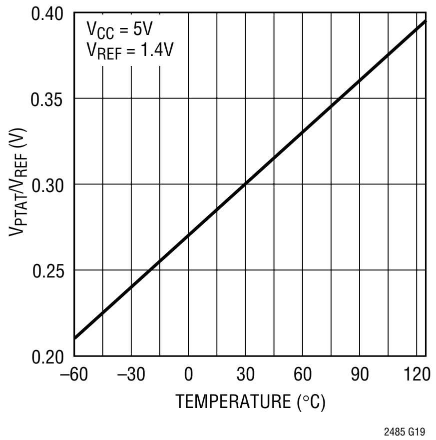


Offset Error vs V_{REF}

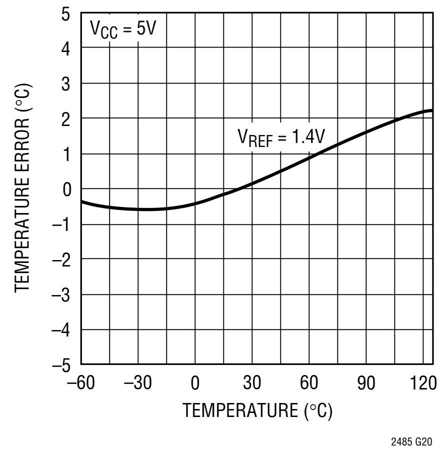


TYPICAL PERFORMANCE CHARACTERISTICS

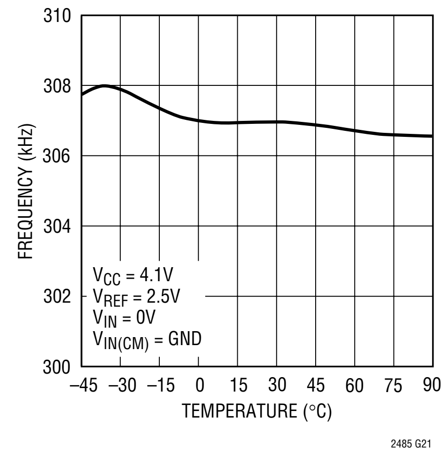
Temperature Sensor vs Temperature



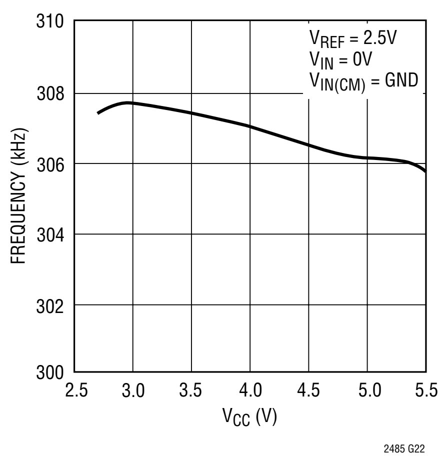
Temperature Sensor Error vs Temperature



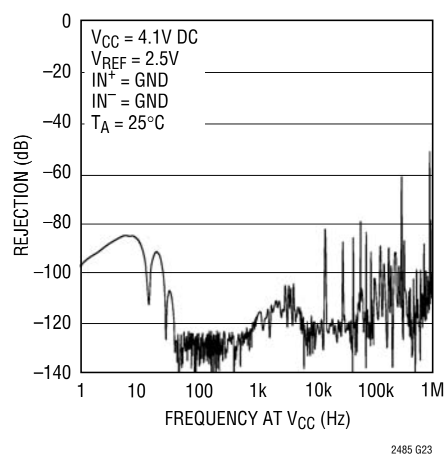
On-Chip Oscillator Frequency vs Temperature



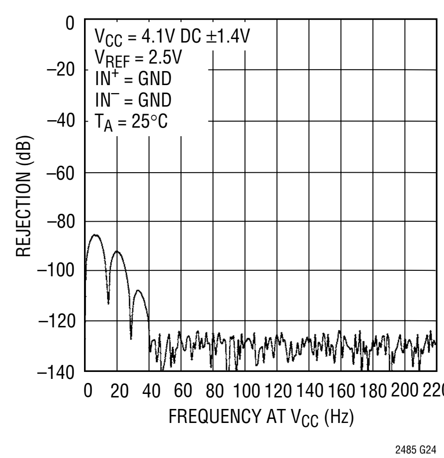
On-Chip Oscillator Frequency vs V_{CC}



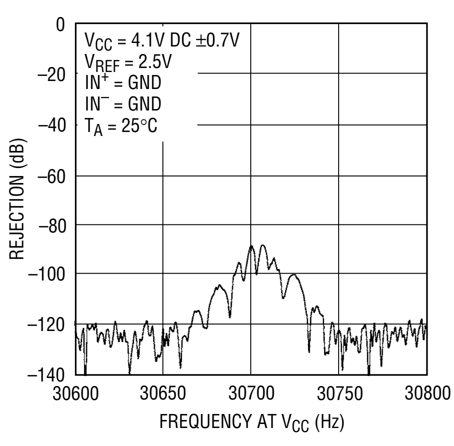
PSRR vs Frequency at V_{CC}



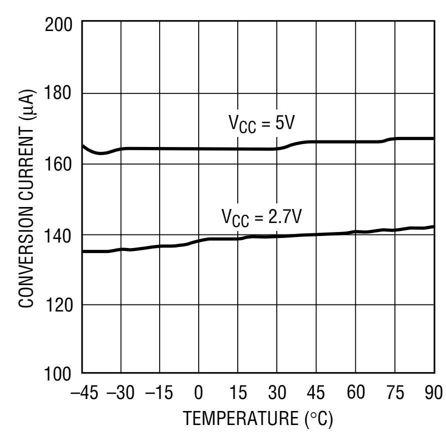
PSRR vs Frequency at V_{CC}



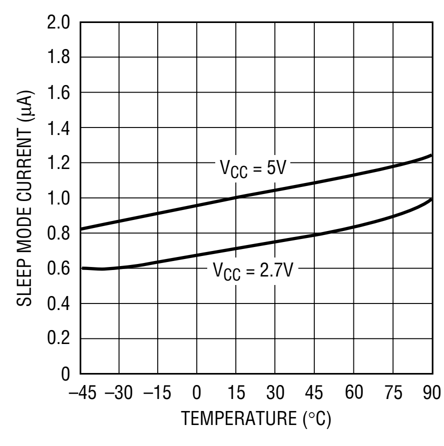
PSRR vs Frequency at V_{CC}



Conversion Current vs Temperature

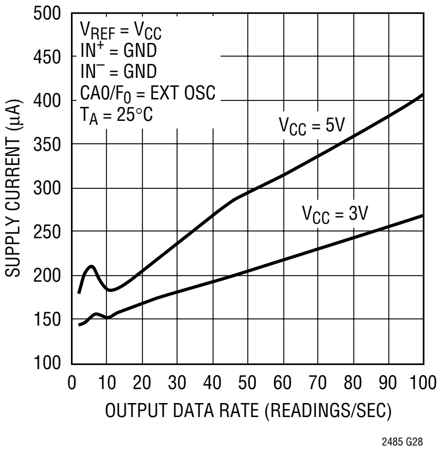


Sleep Mode Current vs Temperature

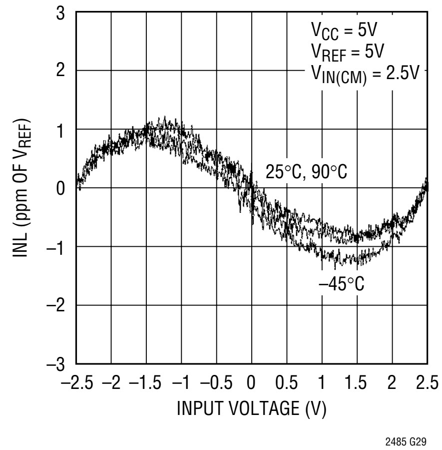


TYPICAL PERFORMANCE CHARACTERISTICS

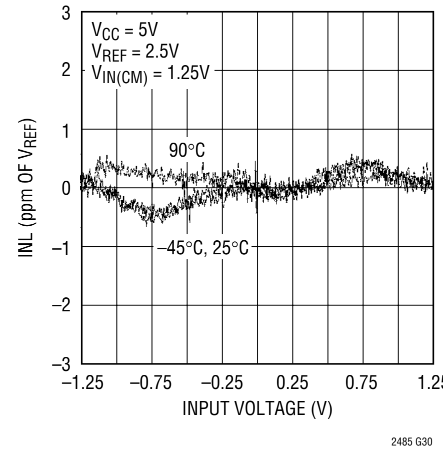
Conversion Current vs Output Data Rate



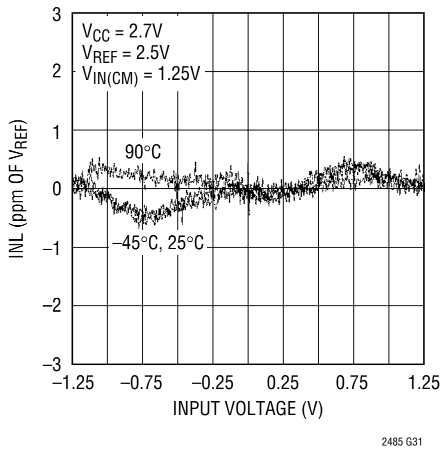
Integral Nonlinearity (2x Speed Mode; $V_{CC} = 5V$, $V_{REF} = 5V$)



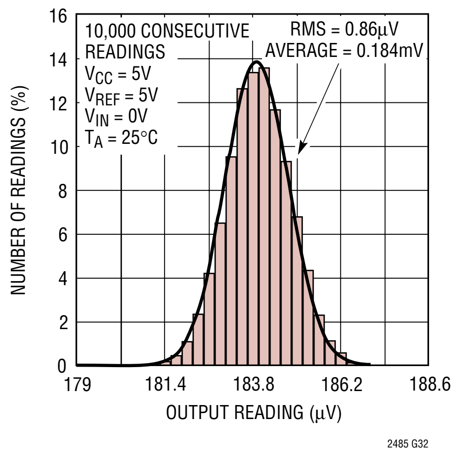
Integral Nonlinearity (2x Speed Mode; $V_{CC} = 5V$, $V_{REF} = 2.5V$)



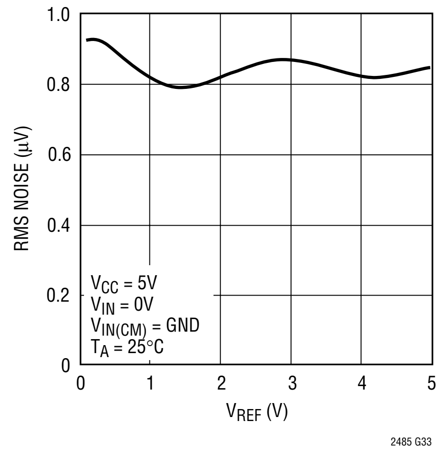
Integral Nonlinearity (2x Speed Mode; $V_{CC} = 2.7V$, $V_{REF} = 2.5V$)



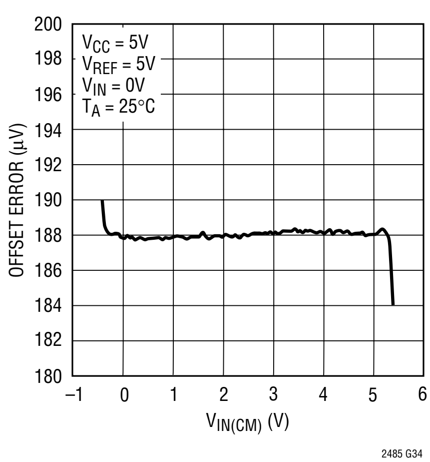
Noise Histogram (2x Speed Mode)



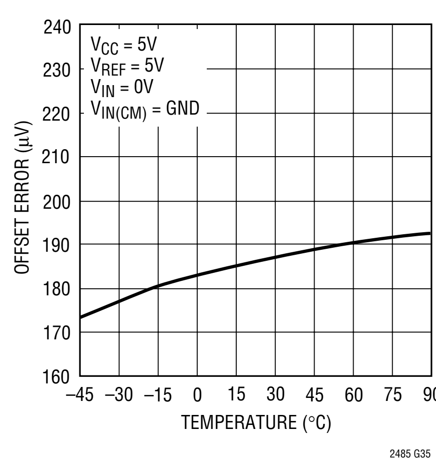
RMS Noise vs V_{REF} (2x Speed Mode)



Offset Error vs $V_{IN(CM)}$ (2x Speed Mode)

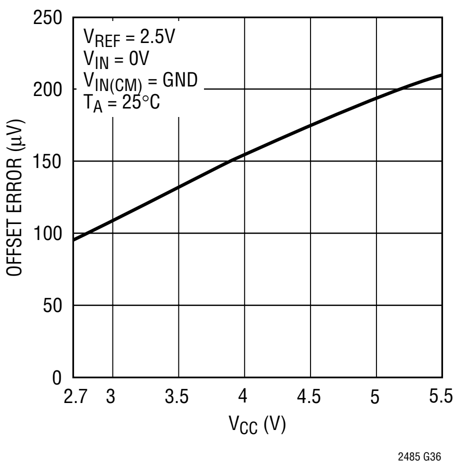


Offset Error vs Temperature (2x Speed Mode)

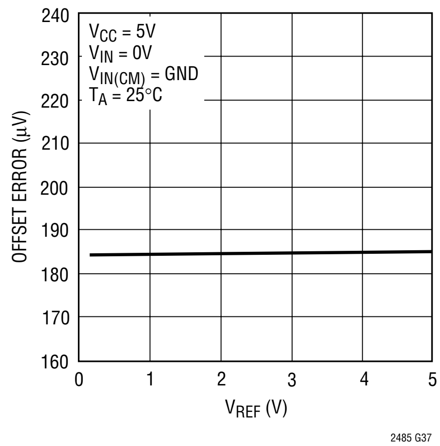


TYPICAL PERFORMANCE CHARACTERISTICS

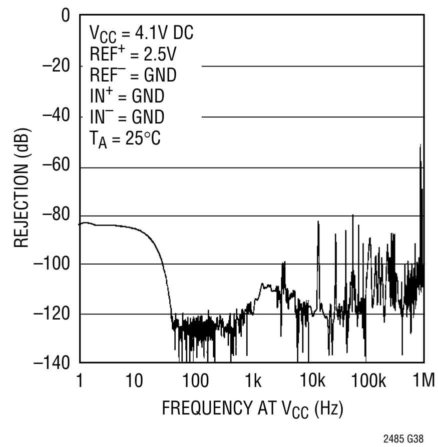
Offset Error vs V_{CC} (2x Speed Mode)



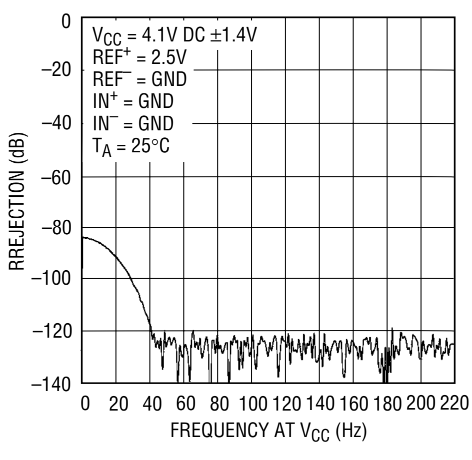
Offset Error vs V_{REF} (2x Speed Mode)



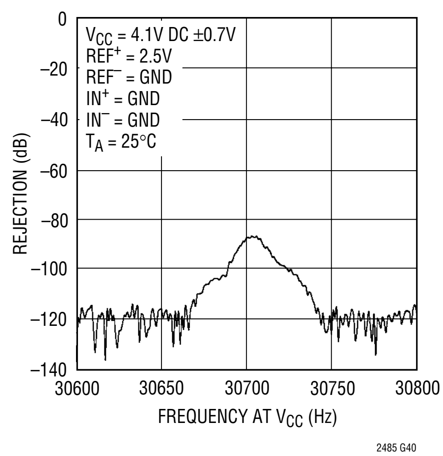
PSRR vs Frequency at V_{CC} (2x Speed Mode)



PSRR vs Frequency at V_{CC} (2x Speed Mode)



PSRR vs Frequency at V_{CC} (2x Speed Mode)



PIN FUNCTIONS

REF^+ (Pin 1), REF^- (Pin 3): Differential Reference Input. The voltage on these pins can have any value between GND and V_{CC} as long as the reference positive input, REF^+, is more positive than the reference negative input, REF^-, by at least 0.1V.

V_{CC} (Pin 2): Positive Supply Voltage. Bypass to GND (Pin 8) with a 1µF tantalum capacitor in parallel with 0.1µF ceramic capacitor as close to the part as possible.

IN^+ (Pin 4), IN^- (Pin 5): Differential Analog Input. The voltage on these pins can have any value between GND – 0.3V and V_{CC} + 0.3V. Within these limits the converter bipolar input range ($V_{IN} = IN^+ - IN^-$) extends from $-0.5 \bullet V_{REF}$ to $0.5 \bullet V_{REF}$. Outside this input range the converter produces unique overrange and underrange output codes.

SCL (Pin 6): Serial Clock Pin of the I^2C Interface. The LTC2485 can only act as a slave and the SCL pin only accepts external serial clock. Data is shifted into the SDA pin on the rising edges of the SCL clock and output through the SDA pin on the falling edges of the SCL clock.

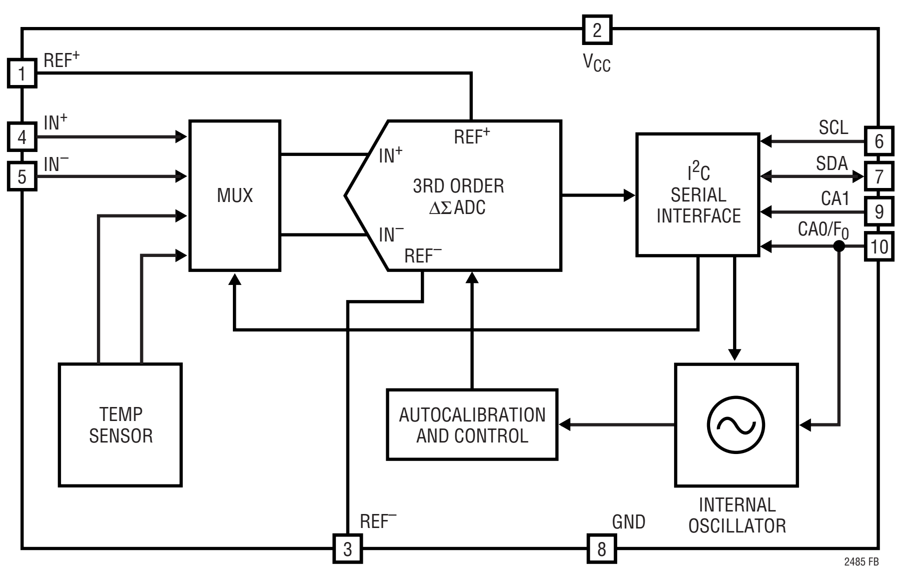
SDA (Pin 7): Bidirectional Serial Data Line of the I^2C Interface. In the transmitter mode (Read), the conversion result is output through the SDA pin, while in the receiver mode (Write), the device configuration bits are input through the SDA pin. At data input mode, the pin is high impedance; while at data output mode, it is an open-drain N-channel driver and therefore an external pull-up resistor or current source to V_{CC} is needed.

GND (Pin 8): Ground. Connect this pin to a ground plane through a low impedance connection.

CA1 (Pin 9): Chip Address Control Pin. The CA1 pin is configured as a three state (LOW, HIGH, or Floating) address control bit for the device I^2C address.

CA0/F_0 (Pin 10): Chip Address Control Pin/External Clock Input Pin. When no transition is detected on the CA0/F_0 pin, it is a two state (HIGH or Floating) address control bit for the device I^2C address. When the pin is driven by an external clock signal with a frequency f_{EOSC} of at least 10kHz, the converter uses this signal as its system clock and the fundamental digital filter rejection null is located at a frequency f_{EOSC}/5120 and sets the Chip Address CA0 internally to a HIGH.

FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS INFORMATION

CONVERTER OPERATION

Converter Operation Cycle

The LTC2485 is a low power, ΔΣ analog-to-digital converter with an I²C interface. After power on reset, its operation is made up of three states. The converter operating cycle begins with the conversion, followed by the low power sleep state and ends with the data output/input (see Figure 1).

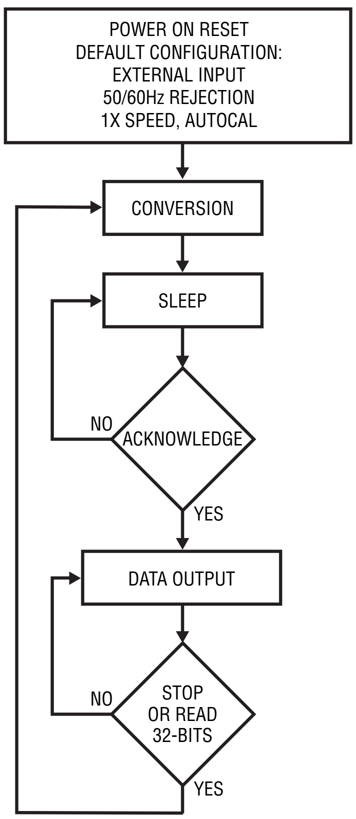


Figure 1. LTC2485 State Transition Diagram

Initially, the LTC2485 performs a conversion. Once the conversion is complete, the device enters the sleep state. While in this sleep state, power consumption is reduced by two orders of magnitude. The part remains in the sleep state as long as it is not addressed for a read/write operation. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.

The device will not acknowledge an external request during the conversion state. After a conversion is finished, the device is ready to accept a read/write request. Once the LTC2485 is addressed for a read operation, the device begins outputting the conversion result under control of the serial clock (SCL). There is no latency in the conversion result. The data output is 32 bits long and contains a 24-bit plus sign conversion result. This result is shifted out on the SDA pin under the control of the SCL. Data is updated on the falling edges of SCL allowing the user to reliably latch data on the rising edge of SCL. In write operation, the device accepts one configuration byte and the data is shifted in on the rising edges of the SCL. A new conversion is initiated by a STOP condition following a valid write operation or at the conclusion of a data read operation (read out all 32 bits).

I²C INTERFACE

The LTC2485 communicates through an I²C interface. The I²C interface is a 2-wire open-drain interface supporting multiple devices and masters on a single bus. The connected devices can only pull the bus wires LOW and they never drive the bus HIGH. The bus wires are externally connected to a positive supply voltage via a current-source or pull-up resistor. When the bus is free, both lines are HIGH. Data on the I²C-bus can be transferred at rates of up to 100kbit/s in the Standard-mode and up to 400kbit/s in the Fast-mode.

Each device on the I²C bus is recognized by a unique address stored in that device and can operate as either a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At the same time any device addressed is considered a slave.

The LTC2485 can only be addressed as a slave. Once addressed, it can receive configuration bits or transmit the last conversion result. Therefore the serial clock line SCL is an input only and the data line SDA is bidirectional. The device supports the Standard-mode and the Fast-mode for data transfer speeds up to 400kbit/s. Figure 2 shows the definition of timing for Fast/Standard-mode devices on the I²C-bus.

APPLICATIONS INFORMATION

The START and STOP Conditions

A START condition is generated by transitioning SDA from HIGH to LOW while SCL is HIGH. The bus is considered to be busy after the START condition. When the data transfer is finished, a STOP condition is generated by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus is free again a certain time after the STOP condition. START and STOP conditions are always generated by the master.

When the bus is in use, it stays busy if a repeated START (Sr) is generated instead of a STOP condition. The repeated START (Sr) conditions are functionally identical to the START (S).

Data Transferring

After the START condition, the I^2C bus is busy and data transfer is set between a master and a slave. Data is transferred over I^2C in groups of nine bits (one byte) followed by an acknowledge bit, therefore each group takes nine SCL cycles. The transmitter releases the SDA line during the acknowledge clock pulse and the receiver issues an Acknowledge (ACK) by pulling SDA LOW or leaves SDA HIGH to indicate a Not Acknowledge (NAK) condition. Change of data state can only happen while SCL is LOW.

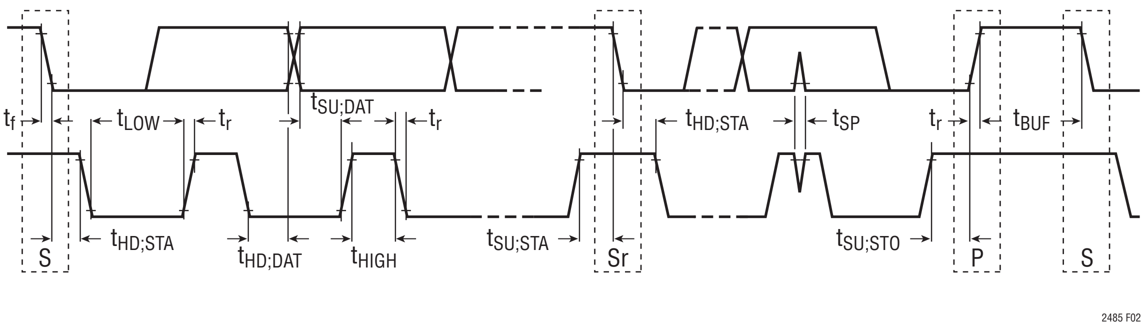


Figure 2. Definition of Timing for F/S-Mode Devices on the I^2C-Bus

APPLICATIONS INFORMATION

Accessing the Special Features of the LTC2485

The LTC2485 combines a high resolution, low noise $\Delta\Sigma$ analog-to-digital converter with an on-chip selectable temperature sensor, programmable digital filter and output rate control. These special features are selected through a single 8-bit serial input word during the data input/output cycle (see Figure 3).

The LTC2485 powers up in a default mode commonly used for most measurements. The device will remain in this mode until a valid write cycle is performed. In this default mode, the measured input is external, the digital filter simultaneously rejects 50Hz and 60Hz line frequency noise, and the speed mode is 1x (offset automatically, continuously calibrated).

The I^2C serial interface grants access to any or all special functions contained within the LTC2485. In order to change the mode of operation, a valid write address followed by 8 bits of data are shifted into the device (see Table 1). The first 4 bits are reserved and should be low. The 5th bit (IM) is used to select the internal temperature sensor as the conversion input, while the 6th and 7th bits (FA, FB) combine to determine the line frequency rejection mode. The 8th bit (SPD) is used to double the output rate by disabling the offset auto calibration.

Temperature Sensor (IM)

The LTC2485 includes an on-chip temperature sensor. The temperature sensor is selected by setting IM = 1 in the serial input data stream. Conversions are performed directly on the temperature sensor by the converter. While operating in this mode, the device behaves as a temperature to bits converter. The digital reading is proportional to the absolute temperature of the device. This feature allows the converter to linearize temperature sensors or continuously remove temperature effects from external sensors. Several applications leveraging this feature are presented in more detail in the applications section. While operating in this mode, the speed is set to normal independent of the control bit (SPD).

Table 1. Selecting Special Modes

IM	FA	FB	SPD	COMMENTS
0	0	0	0	External Input, 50Hz and 60Hz Rejection, Autocalibration
0	0	1	0	External Input, 50Hz Rejection, Autocalibration
0	1	0	0	External Input, 60Hz Rejection, Autocalibration
0	0	0	1	External Input, 50Hz and 60Hz Rejection, 2x Speed
0	0	1	1	External Input, 50Hz Rejection, 2x Speed
0	1	0	1	External Input, 60Hz Rejection, 2x Speed
1	0	0	0	Temperature Input, 50Hz and 60Hz Rejection, Autocalibration
1	0	1	X	Temperature Input, 50Hz Rejection, Autocalibration
1	1	0	X	Temperature Input, 60Hz Rejection, Autocalibration
X	1	1	X	Reserved, Do Not Use

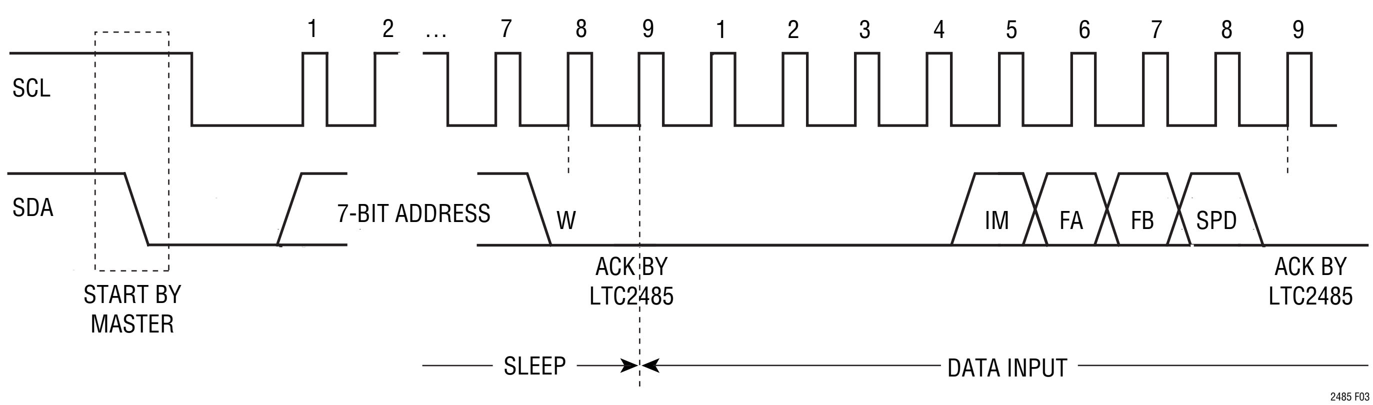


Figure 3. Timing Diagram for Writing to the LTC2485

APPLICATIONS INFORMATION

Rejection Mode (FA, FB)

The LTC2485 includes a high accuracy on-chip oscillator with no required external components. Coupled with a 4th order digital lowpass filter, the LTC2485 rejects line frequency noise. In the default mode, the LTC2485 simultaneously rejects 50Hz and 60Hz by at least 87dB. The LTC2485 can also be configured to selectively reject 50Hz or 60Hz to better than 110dB.

Speed Mode (SPD)

The LTC2485 continuously performs offset calibrations. Every conversion cycle, two conversions are automatically performed (default) and the results combined. This result is free from offset and drift. In applications where the offset is not critical, the autocalibration feature can be disabled with the benefit of twice the output rate.

Linearity, full-scale accuracy and full-scale drift are identical for both 2x and 1x speed modes. In both the 1x and 2x speed there is no latency. This enables input steps or multiplexer channel changes to settle in a single conversion cycle easing system overhead and increasing the effective conversion rate.

LTC2485 Data Format

After a START condition, the master sends a 7-bit address followed by a R/W bit. The bit R/W is 1 for a Read request and 0 for a Write request. If the 7-bit address agrees with an LTC2485's address, that device is selected. When the device is in the conversion state, it does not accept the request and issues a Not-Acknowledge (NAK) by leaving SDA HIGH. A write operation will also generate an NAK signal. If the conversion is complete, it issues an acknowledge (ACK) by pulling SDA LOW.

The LTC2485 has two registers. The output register contains the result of the last conversion and a user programmable configuration register that sets the converter operation mode.

The output register contains the last conversion result. After each conversion is completed, the device automatically enters the sleep state where the supply current is reduced to 1μA. When the LTC2485 is addressed for a Read operation, it acknowledges (by pulling SDA LOW) and acts as a transmitter. The master and receiver can read up to four bytes from the LTC2485. After a complete Read operation (4 bytes), the output register is emptied, a new conversion is initiated, and a following Read request in the same output phase will be NAKed. The LTC2485 output data stream is 32 bits long, shifted out on the falling edges of SCL. The first bit is the conversion result sign bit (SIG), (see Tables 2 and 3). This bit is HIGH if $V_{IN} \geq 0$. It is LOW if $V_{IN} < 0$. The second bit is the most significant bit (MSB)

Table 2. LTC2485 Status Bits

INPUT RANGE	BIT 31 SIG	BIT 30 MSB
$V_{IN} \geq 0.5 \bullet V_{REF}$	1	1
$0V \leq V_{IN} < 0.5 \bullet V_{REF}$	1	0
$-0.5 \bullet V_{REF} \leq V_{IN} < 0V$	0	1
$V_{IN} < -0.5 \bullet V_{REF}$	0	0

Table 3. LTC2485 Output Data Format

DIFFERENTIAL INPUT VOLTAGE V_{IN}*	BIT 31 SIG	BIT 30 MSB	BIT 29	BIT 28	BIT 27	…	BIT 0
V_{IN}* ≥ FS**	1	1	0	0	0	…	0
FS** – 1LSB	1	0	1	1	1	…	1
0.5 • FS**	1	0	1	0	0	…	0
0.5 • FS** – 1LSB	1	0	0	1	1	…	1
0	1	0	0	0	0	…	0
–1LSB	0	1	1	1	1	…	1
–0.5 • FS**	0	1	1	0	0	…	0
–0.5 • FS** – 1LSB	0	1	0	1	1	…	1
–FS**	0	1	0	0	0	…	0
V_{IN}* < –FS**	0	0	1	1	1	…	1

*The differential input voltage $V_{IN} = IN^+ - IN^-$. **The full-scale voltage $FS = 0.5 \bullet V_{REF}$.

APPLICATIONS INFORMATION

of the result. The first two bits (SIG and MSB) can be used to indicate over range conditions. If both bits are HIGH, the differential input voltage is above +FS and the following 24 bits are set to LOW to indicate an overrange condition. If both bits are LOW, the input voltage is below –FS and the following 24 bits are set to HIGH to indicate an underrange condition. The function of these two bits is summarized in Table 1. The next 24 bits contain the conversion results in binary two's complement format. The remaining six bits are Sub LSBs below the 24-bit level.

As long as the voltage on the IN^+ and IN^- pins is maintained within the –0.3V to (V_{CC} + 0.3V) absolute maximum operating range, a conversion result is generated for any differential input voltage V_{IN} from –FS = –0.5 • V_{REF} to +FS=0.5 • V_{REF}. For differential input voltages greater than +FS, the conversion result is clamped to the value corresponding to the +FS + 1LSB. For differential input voltages below –FS, the conversion result is clamped to the value corresponding to –FS – 1LSB.

Initiating a New Conversion

When the LTC2485 finishes a conversion, it automatically enters the sleep state. Once in the sleep state, the device is ready for a Read operation. After the device acknowledges a Read request, the device exits the sleep state and enters the data output state. The data output state concludes and the LTC2485 starts a new conversion once a STOP condition is issued by the master or all 32 bits of data are read out of the device.

During the data read cycle, a stop command may be issued by the master controller in order to start a new conversion and abort the data transfer. This stop command must be issued during the ninth clock cycle of a byte read when the bus is free (the ACK/NAK cycle).

LTC2485 Address

The LTC2485 has two address pins, enabling one in 6 possible addresses, as shown in Table 4.

Table 4. LTC2485 Address Assignment

CA1	CA0/F_0 *	Address
LOW	HIGH	001 01 00
LOW	Floating	001 01 01
Floating	HIGH	001 01 11
Floating	Floating	010 01 00
HIGH	HIGH	010 01 10
HIGH	Floating	010 01 11

* CA0/F_0 is treated as HIGH when driven by a valid external clock.

In addition to the configurable addresses listed in Table 5, the LTC2485 also contains a global address (1110111) which may be used for synchronizing multiple LTC2485s.

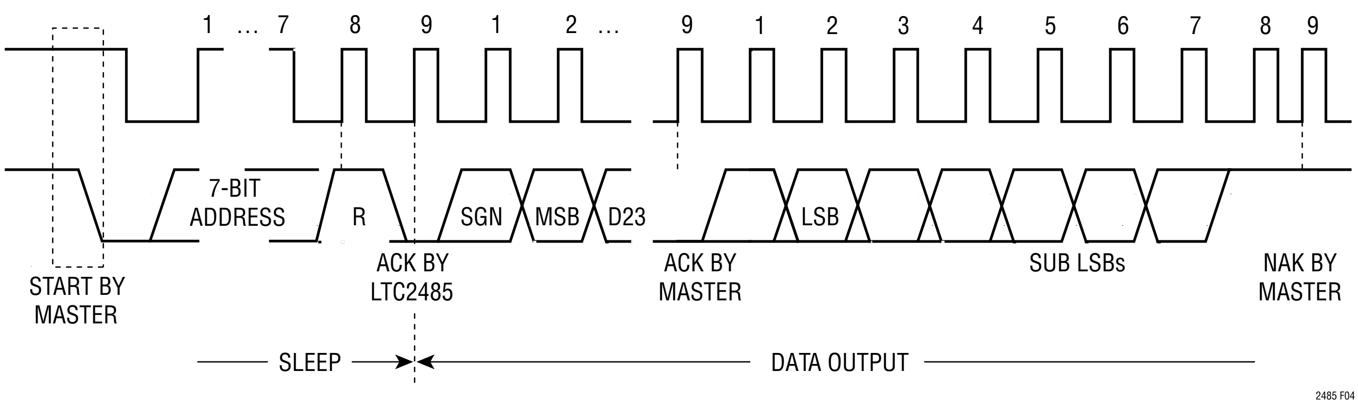


Figure 4. Timing Diagram for Reading from the LTC2485

APPLICATIONS INFORMATION

OPERATION SEQUENCE

The LTC2485 acts as a transmitter or receiver. The device may be programmed to perform several functions. These include measuring an external differential input signal or an integrated temperature sensor, selecting line frequency rejection (50Hz, 60Hz, or simultaneous 50Hz and 60Hz), and a 2x speed up mode.

Continuous Read

In applications where the configuration does not need to change for each conversion cycle, the conversion result can be continuously read. The configuration remains unchanged from the last value written into the device. If the device has not been written to since power up, the configuration is set to the default value (Input External, simultaneous 50Hz/60Hz rejection, and 1x speed mode). The operation sequence is shown in Figure 6. When the conversion is finished, the device may be addressed for a read operation. At the end of a read operation, a new conversion begins. At the conclusion of the conversion cycle, the next result may be read using the method described above. If the conversion cycle is not concluded and a valid address selects the device, the LTC2485 generates a NAK signal indicating the conversion cycle is in progress.

Continuous Read/Write

Once the conversion cycle is concluded, the LTC2485 can be written to then read from, using the repeated Start (Sr) command.

Figure 7 shows a cycle which begins with a data Write, a repeated start, followed by a read, and concluded with a stop command. The following conversion begins after all 32 bits are read out of the device or after the STOP command and uses the newly programmed configuration data.

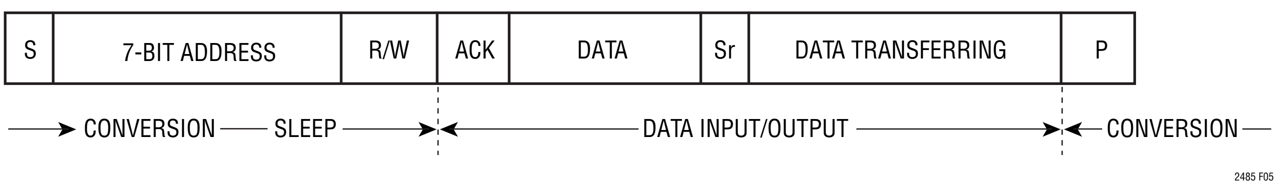


Figure 5. The LTC2485 Conversion Sequence

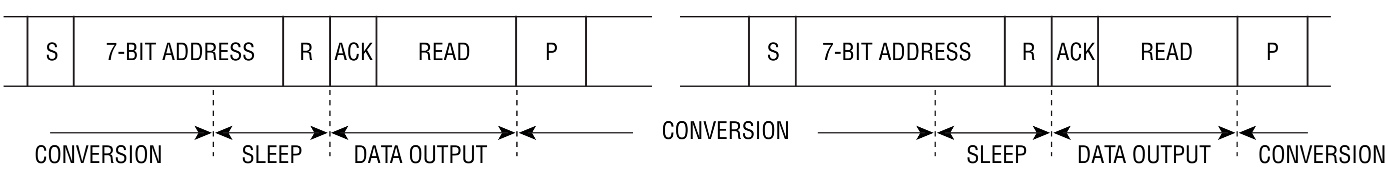


Figure 6. Consecutive Reading at the Same Configuration

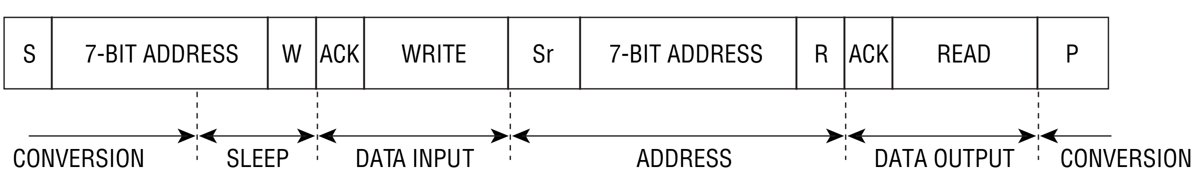


Figure 7. Write, Read, Start Conversion

APPLICATIONS INFORMATION

Discarding a Conversion Result and Initiating a New Conversion with Optional Configuration Updating

At the conclusion of a conversion cycle, a Write cycle can be initiated. Once the Write cycle is acknowledged, a stop (P) command initiates a new conversion. If a new configuration is required, this data can be written into the device and a stop command initiates a new conversion, see Figure 8.

Synchronizing Multiple LTC2485s with the Global Address Call

In applications where several LTC2485s are used on the same I^2C bus, all LTC2485s can be synchronized with the global address call. To achieve this, first all the LTC2485s must have completed the conversion cycle. The master issues a Start, followed by the LTC2485 global address 1110111 and a Write request. All LTC2485s will be selected and acknowledge the request. The master then sends the write byte (Optional) and ends the Write operation with a STOP. This will update the configuration registers (if a write byte was sent) and initiate a new conversion simultaneously on all the LTC2485s, as shown in Figure 9. In order to synchronize the start of conversion without affecting the configuration registers, the Write operation can be aborted with a STOP. This initiates a new conversion on all the LTC2485s without changing the configuration registers.

Easy Drive Input Current Cancellation

The LTC2485 combines a high precision delta-sigma ADC with an automatic differential input current cancellation front end. A proprietary front-end passive sampling network transparently removes the differential input current. This enables external RC networks and high impedance sensors to directly interface to the LTC2485 without external amplifiers. The remaining common mode input current is eliminated by either balancing the differential input impedances or setting the common mode input equal to the common mode reference (see Automatic Input Current Cancellation section). This unique architecture does not require on-chip buffers enabling input signals to swing all the way to ground and up to V_{CC}. Furthermore, the cancellation does not interfere with the transparent offset and full-scale auto-calibration and the absolute accuracy (full scale + offset + linearity) is maintained even with external RC networks.

Conversion Clock

A major advantage the delta-sigma converter offers over conventional type converters is an on-chip digital filter (commonly implemented as a SINC or Comb filter). For high resolution, low frequency applications, this filter is typically designed to reject line frequencies of 50Hz or 60Hz plus their harmonics. The filter rejection performance is directly related to the accuracy of the converter system clock. The

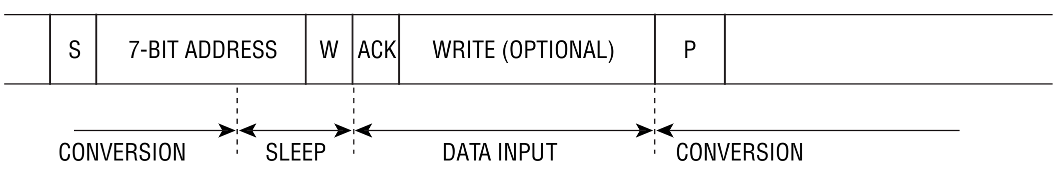


Figure 8. Start a New Conversion without Reading Old Conversion Result

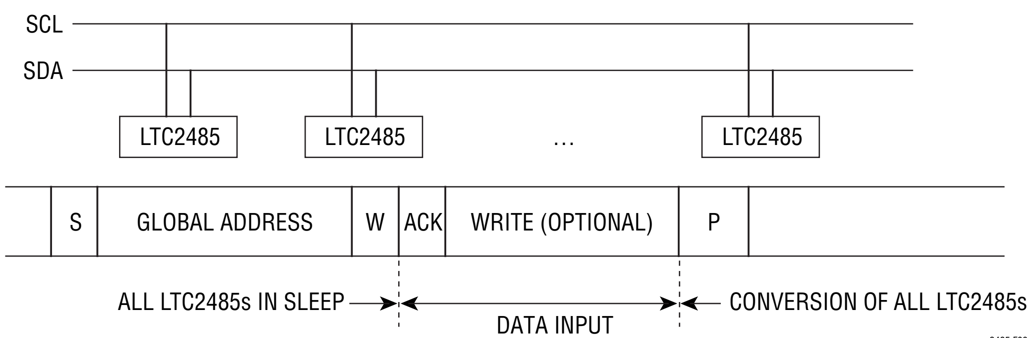


Figure 9. Synchronize the LTC2485s with the Global Address Call

APPLICATIONS INFORMATION

LTC2485 incorporates a highly accurate on-chip oscillator. This eliminates the need for external frequency setting components such as crystals or oscillators.

Frequency Rejection Selection (CA0/F_0)

The LTC2485 internal oscillator provides better than 110dB normal mode rejection at the line frequency and all its harmonics (up to the 255th) for 50Hz ±2% or 60Hz ±2%, or better than 87dB normal mode rejection from 48Hz to 62.4Hz. The rejection mode is selected by writing to the on-chip configuration register (the default mode at power up is simultaneous 50Hz/60Hz rejection).

When a fundamental rejection frequency different from 50Hz or 60Hz is required or when the converter must be synchronized with an outside source, the LTC2485 can operate with an external conversion clock. The converter automatically detects the presence of an external clock signal at the CA0/F_0 pin and turns off the internal oscillator. The chip address for CA0 is internally set HIGH. The frequency f_{EOSC} of the external signal must be at least 10kHz to be detected. The external clock signal duty cycle is not significant as long as the minimum and maximum specifications for the high and low periods t_{HEO} and t_{LEO} are observed.

While operating with an external conversion clock of a frequency f_{EOSC}, the LTC2485 provides better than 110dB normal mode rejection in a frequency range of f_{EOSC}/5120 ±4% and its harmonics. The normal mode rejection as a function of the input frequency deviation from f_{EOSC}/5120 is shown in Figure 10.

Whenever an external clock is not present at the CA0/F_0 pin, the converter automatically activates its internal oscillator and enters the Internal Conversion Clock mode. CA0/F_0 may be tied HIGH or left floating in order to set the chip address. The LTC2485 operation will not be disturbed if the change of conversion clock source occurs during the sleep state or during the data output state while the converter uses an external serial clock. If the change occurs during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected.

Table 5 summarizes the duration of the conversion state of each state and the achievable output data rate as a function of f_{EOSC}.

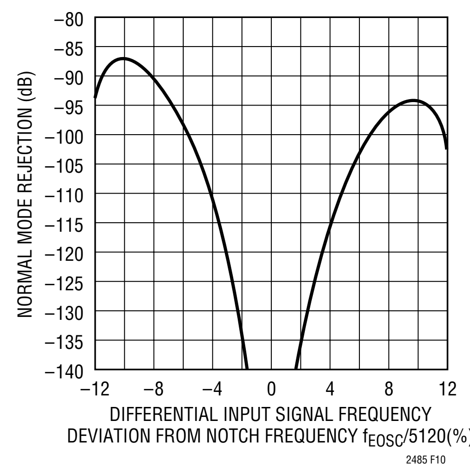


Figure 10. LTC2485 Normal Mode Rejection When Using an External Oscillator

Table 6. LTC2485 State Duration

STATE	OPERATING MODE		DURATION
CONVERSION	Internal Oscillator	60Hz Rejection	133ms, Output Data Rate ≤ 7.5 Readings/s for 1x Speed Mode 67ms, Output Data Rate ≤ 15 Readings/s for 2x Speed Mode
		50Hz Rejection	160ms, Output Data Rate ≤ 6.2 Readings/s for 1x Speed Mode 80ms, Output Data Rate ≤ 12.5 Readings/s for 2x Speed Mode
		50Hz/60Hz Rejection	147ms, Output Data Rate ≤ 6.8 Readings/s for 1x Speed Mode 73.6ms, Output Data Rate ≤ 13.6 Readings/s for 2x Speed Mode
	External Oscillator	CA0/F_0 = External Oscillator with Frequency f_{EOSC} Hz (f_{EOSC}/5120 Rejection)	41036/f_{EOSC}s, Output Data Rate ≤ f_{EOSC}/41036 Readings/s for 1x Speed Mode 20556/f_{EOSC}s, Output Data Rate ≤ f_{EOSC}/20556 Readings/s for 2x Speed Mode

APPLICATIONS INFORMATION

Ease of Use

The LTC2485 data output has no latency, filter settling delay or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog voltages is easy.

The LTC2485 performs offset and full-scale calibrations every conversion cycle. This calibration is transparent to the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

Power-Up Sequence

The LTC2485 automatically enters an internal reset state when the power supply voltage V_{CC} drops below approximately 2V. This feature guarantees the integrity of the conversion result.

When the V_{CC} voltage rises above this critical threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. Following the POR signal, the LTC2485 starts a normal conversion cycle and follows the succession of states described in Figure 1. The first conversion result following POR is accurate within the specifications of the device if the power supply voltage is restored within the operating range (2.7V to 5.5V) before the end of the POR time interval.

On-Chip Temperature Sensor

The LTC2485 contains an on-chip PTAT (proportional to absolute temperature) signal that can be used as a temperature sensor. The internal PTAT has a typical value of 420mV at 27°C and is proportional to the absolute temperature value with a temperature coefficient of 420/(27 + 273) = 1.40mV/°C (SLOPE), as shown in Figure 11. The internal PTAT signal is used in a single-ended mode referenced to device ground internally. The 1x speed mode with automatic offset calibration is automatically selected for the internal PTAT signal measurement as well.

When using the internal temperature sensor, if the output code is normalized to $R_{SDA} = V_{PTAT}/V_{REF}$, the temperature is calculated using the following formula:

$$T_K = \frac{R_{SDA} \bullet V_{REF}}{SLOPE} \text{ in Kelvin}$$

and

$$T_C = \frac{R_{SDA} \bullet V_{REF}}{SLOPE} - 273 \text{ in °C}$$

where SLOPE is nominally 1.4mV/°C.

Since the PTAT signal can have an initial value variation which results in errors in SLOPE, to achieve absolute temperature measurements, a one-time calibration is needed to adjust the SLOPE value. The converter output of the PTAT signal, $R0_{SDA}$, is measured at a known temperature T0 (in °C) and the SLOPE is calculated as:

$$SLOPE = \frac{R0_{SDA} \bullet V_{REF}}{T0 + 273}$$

This calibrated SLOPE can be used to calculate the temperature.

If the same V_{REF} source is used during calibration and temperature measurement, the actual value of the V_{REF} is not needed to measure the temperature as shown in the calculation below:

$$\begin{aligned} T_C &= \frac{R_{SDA} \bullet V_{REF}}{SLOPE} - 273 \\ &= \frac{R_{SDA}}{R0_{SDA}} \bullet \left(T0 + 273\right) - 273 \end{aligned}$$

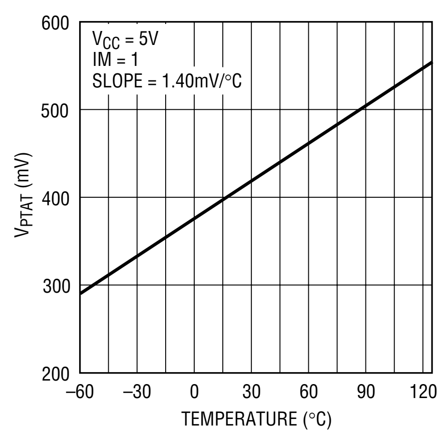


Figure 11. Internal PTAT Signal vs Temperature

APPLICATIONS INFORMATION

Reference Voltage Range

The LTC2485 external reference voltage range is 0.1V to V_{CC}. The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in nanovolts is nearly constant with reference voltage. A reduced reference voltage will improve the converter performance when operated with an external conversion clock (external F_O signal) at substantially higher output data rates (see the Output Data Rate section). V_{REF} must be ≥1.1V to use the internal temperature sensor.

The reference input is differential. The differential reference input range ($V_{REF} = REF^+ – REF^–$) is 100mV to V_{CC} and the common mode reference input range is 0V to V_{CC}.

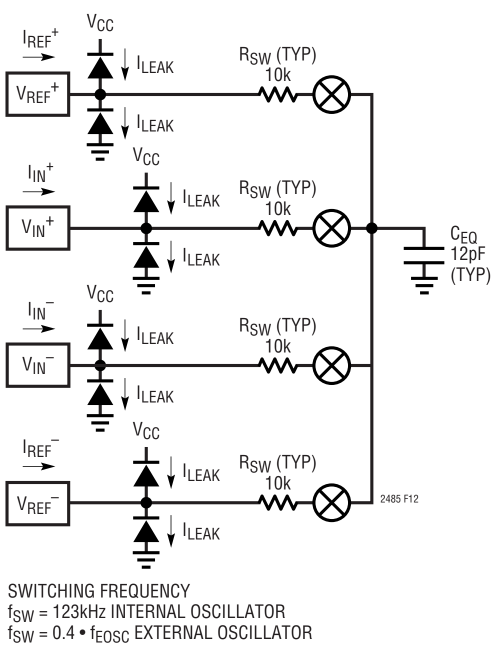
Input Voltage Range

The analog input is truly differential with an absolute/common mode range for the IN^+ and $IN^–$ input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2485 converts the bipolar differential input signal, $V_{IN} = IN^+ – IN^–$, from –FS to +FS where FS = 0.5 • V_{REF}. Beyond this range, the converter indicates the overrange or the underrange condition using distinct output codes. Since the differential input current cancellation does not rely on an on-chip buffer, current cancellation and DC performance is maintained rail-to-rail.

Input signals applied to IN^+ and $IN^–$ pins may extend by 300mV below ground and above V_{CC}. In order to limit any fault current, resistors of up to 5k may be added in series with the IN^+ and $IN^–$ pins without affecting the performance of the devices. The effect of the series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent offset error due to the input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

Driving the Input and Reference

The input and reference pins of the LTC2485 converter are directly connected to a network of sampling capacitors. Depending upon the relation between the differential input voltage and the differential reference voltage, these capacitors are switching between these four pins transferring small amounts of charge in the process. A simplified equivalent circuit is shown in Figure 12.



$$I(IN^+)_{AVG} = I(IN^-)_{AVG} = \frac{V_{IN(CM)} - V_{REF(CM)}}{0.5 \bullet R_{EQ}}$$

$$I(REF^+)_{AVG} = \frac{1.5 \bullet V_{REF} - V_{INCM} + V_{REFCM}}{0.5 \bullet R_{EQ}} - \frac{V_{IN}^2}{V_{REF} \bullet R_{EQ}} - \frac{0.5 \bullet V_{REF} \bullet D_T}{R_{EQ}} \cong \frac{1.5V_{REF} + (V_{REF(CM)} - V_{IN(CM)})}{0.5 \bullet R_{EQ}} - \frac{V_{IN}^2}{V_{REF} \bullet R_{EQ}}$$

where:

$$V_{REFCM} = \left(\frac{REF^+ + REF^-}{2}\right), V_{REF} = REF^+ - REF^-$$

$$V_{IN} = IN^+ - IN^-$$

$$V_{INCM} = \left(\frac{IN^+ + IN^-}{2}\right)$$

$R_{EQ} = 2.71M\Omega$ INTERNAL OSCILLATOR 60Hz MODE

$R_{EQ} = 2.98M\Omega$ INTERNAL OSCILLATOR 50Hz AND 60Hz MODE

$R_{EQ} = (0.833 \bullet 10^{12}) / f_{EOSC}$ EXTERNAL OSCILLATOR

D_T IS THE DENSITY OF A DIGITAL TRANSITION AT THE MODULATOR OUTPUT

WHERE $REF^–$ IS INTERNALLY TIED TO GND

Figure 12. LTC2485 Equivalent Analog Input Circuit

APPLICATIONS INFORMATION

For a simple approximation, the source impedance R_S driving an analog input pin (IN^+, IN^-, REF^+ or REF^-) can be considered to form, together with R_{SW} and C_{EQ} (see Figure 12), a first order passive network with a time constant $\tau = (R_S + R_{SW}) \bullet C_{EQ}$. The converter is able to sample the input signal with better than 1ppm accuracy if the sampling period is at least 14 times greater than the input circuit time constant τ. The sampling process on the four input analog pins is quasi-independent so each time constant should be considered by itself and, under worst-case circumstances, the errors may add.

When using the internal oscillator, the LTC2485's front-end switched-capacitor network is clocked at 123kHz corresponding to an 8.1µs sampling period. Thus, for settling errors of less than 1ppm, the driving source impedance should be chosen such that $\tau \le 8.1\mu s/14 = 580ns$. When an external oscillator of frequency f_{EOSC} is used, the sampling period is $2.5/f_{EOSC}$ and, for a settling error of less than 1ppm, $\tau \le 0.178/f_{EOSC}$.

Automatic Differential Input Current Cancellation

In applications where the sensor output impedance is low (up to 10kΩ with no external bypass capacitor or up to 500Ω with 0.001µF bypass), complete settling of the input occurs. In this case, no errors are introduced and direct digitization of the sensor is possible.

For many applications, the sensor output impedance combined with external bypass capacitors produces RC time constants much greater than the 580ns required for 1ppm accuracy. For example, a 10kΩ bridge driving a 0.1µF bypass capacitor has a time constant an order of magnitude greater than the required maximum. Historically, settling issues were solved using buffers. These buffers led to increased noise, reduced DC performance (Offset/Drift), limited input/output swing (cannot digitize signals near ground or V_{CC}), added system cost and increased power. The LTC2485 uses a proprietary switching algorithm that forces the average differential input current to zero independent of external settling errors. This allows accurate direct digitization of high impedance sensors without the need of buffers (see Figures 13 to 15). Additional errors resulting from mismatched leakage currents must also be taken into account.

The switching algorithm forces the average input current on the positive input (I_{IN}^+) to be equal to the average input current on the negative input (I_{IN}^-). Over the complete conversion cycle, the average differential input current ($I_{IN}^+ - I_{IN}^-$) is zero. While the differential input current is zero, the common mode input current ($I_{IN}^+ + I_{IN}^-$)/2 is proportional to the difference between the common mode input voltage (V_{INCM}) and the common mode reference voltage (V_{REFCM}).

In applications where the input common mode voltage is equal to the reference common mode voltage, as in the case of a balance bridge type application, both the differential and common mode input current are zero. The accuracy of the converter is unaffected by settling errors. Mismatches in source impedances between IN^+ and IN^- also do not affect the accuracy.

In applications where the input common mode voltage is constant but different from the reference common mode voltage, the differential input current remains zero while the common mode input current is proportional to the difference between V_{INCM} and V_{REFCM}. For a reference common mode of 2.5V and an input common mode of 1.5V, the common mode input current is approximately 0.74µA (in simultaneous 50Hz/60Hz rejection mode). This common mode input current has no effect on the accuracy if the external source impedances tied to IN^+ and IN^- are matched. Mismatches in these source impedances lead to a fixed offset error but do not affect the linearity or full-scale reading. A 1% mismatch in 1kΩ source resistances leads to a 15ppm shift (74µV) in offset voltage.

In applications where the common mode input voltage varies as a function of input signal level (single-ended input, RTDs, half bridges, current sensors, etc.), the common mode input current varies proportionally with input voltage. For the case of balanced input impedances, the common mode input current effects are rejected by the large CMRR of the LTC2485 leading to little degradation in accuracy. Mismatches in source impedances lead to gain errors proportional to the difference between the common mode input voltage and the common mode reference voltage. 1% mismatches in 1kΩ source resistances lead to worst-case gain errors on the order of 15ppm or 1LSB (for 1V differences in reference and input common mode

APPLICATIONS INFORMATION

voltage). Table 6 summarizes the effects of mismatched source impedance and differences in reference/input common mode voltages.

Table 6. Suggested Input Configuration for LTC2485

	BALANCED INPUT RESISTANCES	UNBALANCED INPUT RESISTANCES
Constant $V_{IN(CM)} – V_{REF(CM)}$	C_{EXT} > 1nF at Both IN^+ and $IN^–$. Can Take Large Source Resistance with Negligible Error	C_{EXT} > 1nF at Both IN^+ and $IN^–$. Can Take Large Source Resistance. Unbalanced Resistance Results in an Offset Which Can be Calibrated
Varying $V_{IN(CM)} – V_{REF(CM)}$	C_{EXT} > 1nF at Both IN^+ and $IN^–$. Can Take Large Source Resistance with Negligible Error	Minimize IN^+ and $IN^–$ Capacitors and Avoid Large Source Impedance (<5k Recommended)

The magnitude of the dynamic input current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature and power supply range is typically better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are used for the external source impedance seen by IN^+ and $IN^–$, the expected drift of the dynamic current and offset will be insignificant (about 1% of their respective values over the entire temperature and voltage range). Even for the most stringent applications, a one-time calibration operation may be sufficient.

In addition to the input sampling charge, the input ESD protection diodes have a temperature dependent leakage current. This current, nominally 1nA (±10nA max), results in a small offset shift. A 1k source resistance will create a 1µV typical and 10µV maximum offset voltage.

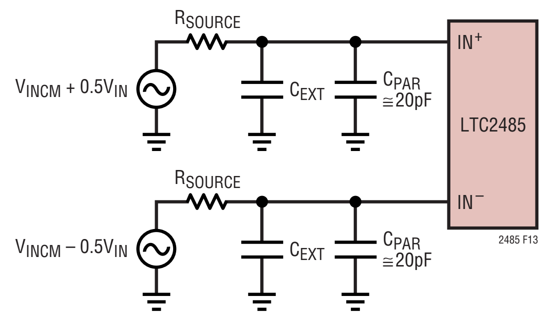


Figure 13. An RC Network at IN^+ and $IN^–$

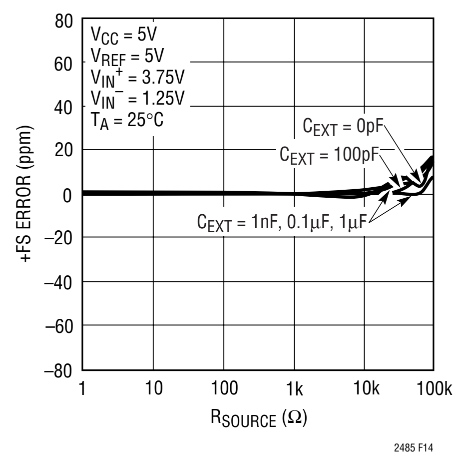


Figure 14. +FS Error vs R_{SOURCE} at IN^+ and $IN^–$

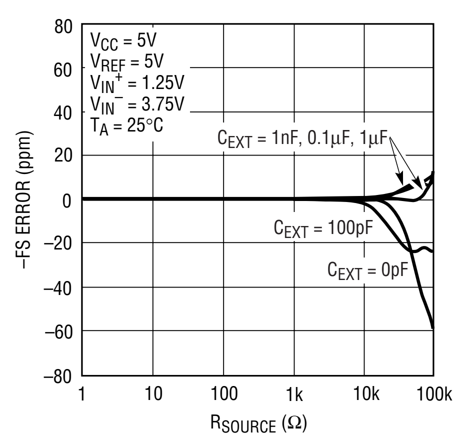


Figure 15. –FS Error vs R_{SOURCE} at IN^+ and $IN^–$

APPLICATIONS INFORMATION

Reference Current

In a similar fashion, the LTC2485 samples the differential reference pins REF^+ and REF^- transferring small amount of charge to and from the external driving circuits thus producing a dynamic reference current. This current does not change the converter offset, but it may degrade the gain and INL performance. The effect of this current can be analyzed in two distinct situations.

For relatively small values of the external reference capacitors (C_{REF} < 1nF), the voltage on the sampling capacitor settles almost completely and relatively large values for the source impedance result in only small errors. Such values for C_{REF} will deteriorate the converter offset and gain performance without significant benefits of reference filtering and the user is advised to avoid them.

Larger values of reference capacitors (C_{REF} > 1nF) may be required as reference filters in certain configurations. Such capacitors will average the reference sampling charge and the external source resistance will see a quasi constant reference differential impedance.

In the following discussion, it is assumed the input and reference common mode are the same. Using internal oscillator for 60Hz mode, the typical differential reference resistance is 1MΩ which generates a full-scale ($V_{REF}/2$) gain error of 0.51ppm for each ohm of source resistance driving the REF^+ or REF^- pins. For 50Hz/60Hz mode, the related difference resistance is 1.1MΩ and the resulting full-scale error is 0.46ppm for each ohm of source resistance driving the REF^+ and REF^- pins. For 50Hz mode, the related difference resistance is 1.2MΩ and the resulting full-scale error is 0.42ppm for each ohm of source resistance driving the REF^+ and REF^- pins. When $CA0/F_0$ is driven by an external oscillator with a frequency f_{EOSC} (external conversion clock operation), the typical differential reference resistance is $0.30 \cdot 10^{12}/f_{EOSC}$ Ω and each ohm of source resistance driving the REF^+ or REF^- pins will result in $1.67 \cdot 10^{-6} \cdot f_{EOSC}$ppm gain error. The typical +FS and –FS errors for various combinations of source resis-tance seen by the REF^+ or REF^- pins and external capacitance connected to that pin are shown in Figures 16-19.

In addition to this gain error, the converter INL performance is degraded by the reference source impedance. The INL is caused by the input dependent terms $-V_{IN}^2/(V_{REF} \cdot R_{EQ}) - (0.5 \cdot V_{REF} \cdot D_T)/R_{EQ}$ in the reference pin current as expressed in Figure 12. When using internal oscillator and 60Hz mode, every 100Ω of reference source resistance translates into about 0.67ppm additional INL error. When using internal oscillator and 50Hz/60Hz mode, every 100Ω of reference source resistance translates into about 0.61ppm additional INL error. When using internal oscillator and 50Hz mode, every 100Ω of reference source resistance translates into about 0.56ppm additional INL error. When $CA0/F_0$ is driven by an external oscillator with a frequency f_{EOSC}, every 100Ω of source resistance driving REF^+ or REF^- translates into about $2.18 \cdot 10^{-6} \cdot f_{EOSC}$ppm additional INL error. Figure 20 shows the typical INL error due to the source resistance driving the REF^+ or REF^- pins when large C_{REF} values are used. The user is advised to minimize the source impedance driving the REF^+ and REF^- pins.

In applications where the reference and input common mode voltages are different, extra errors are introduced. For every 1V of the reference and input common mode voltage difference ($V_{REFCM} - V_{INCM}$) and a 5V reference, each Ohm of reference source resistance introduces an extra $(V_{REFCM} - V_{INCM})/(V_{REF} \cdot R_{EQ})$ full-scale gain error, which is 0.074ppm when using internal oscillator and 60Hz mode. When using internal oscillator and 50Hz/60Hz mode, the extra full-scale gain error is 0.067ppm. When using internal oscillator and 50Hz mode, the extra gain error is 0.061ppm. If an external clock is used, the corresponding extra gain error is $0.24 \cdot 10^{-6} \cdot f_{EOSC}$ppm.

The magnitude of the dynamic reference current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature and power supply range is typically better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are used for the external source impedance seen by V_{REF}^+ and V_{REF}^-, the expected drift of the dynamic current gain error will be insignificant (about 1% of its value over the entire temperature and voltage range). Even for the most stringent applications a one-time calibration operation may be sufficient.

In addition to the reference sampling charge, the reference pins ESD protection diodes have a temperature dependent leakage

APPLICATIONS INFORMATION

current. This leakage current, nominally 1nA (±10nA max), results in a small gain error. A 100Ω source resistance will create a 0.05µV typical and 0.5µV maximum full-scale error.

Output Data Rate

When using its internal oscillator, the LTC2485 produces up to 7.5 samples per second (sps) with a notch frequency of 60Hz, 6.25sps with a notch frequency of 50Hz and 6.82sps with the 50Hz/60Hz rejection mode. The actual output data rate will depend upon the length of the sleep and data output phases which are controlled by the user and which can be made insignificantly short. When operated with an external conversion clock (CA0/F_0 connected to an external oscillator), the LTC2485 output data rate can be increased as desired. The duration of the conversion

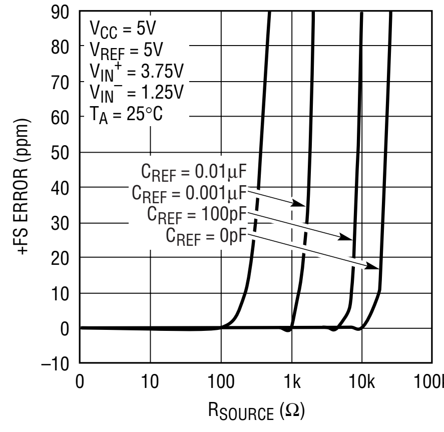


Figure 16. +FS Error vs R_{SOURCE} at REF^+ or REF^- (Small C_{REF})

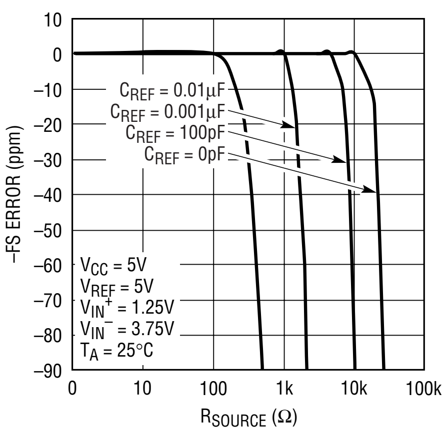


Figure 17. –FS Error vs R_{SOURCE} at REF^+ or REF^- (Small C_{REF})

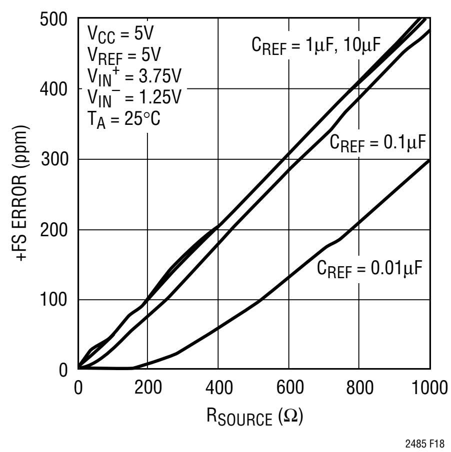


Figure 18. +FS Error vs R_{SOURCE} at REF^+ or REF^- (Large C_{REF})

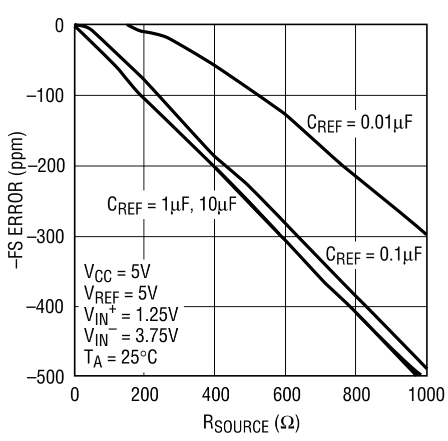


Figure 19. –FS Error vs R_{SOURCE} at REF^+ or REF^- (Large C_{REF})

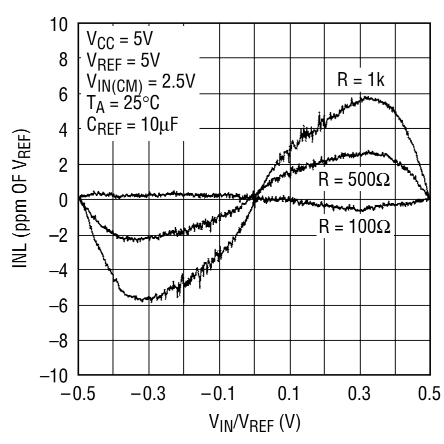


Figure 20. INL vs DIFFERENTIAL Input Voltage and Reference Source Resistance for C_{REF} > 1µF

APPLICATIONS INFORMATION

phase is $41036/f_{EOSC}$. If f_{EOSC} = 307.2kHz, the converter behaves as if the internal oscillator is used and the notch is set at 60Hz.

An increase in f_{EOSC} over the nominal 307.2kHz will translate into a proportional increase in the maximum output data rate. The increase in output rate is nevertheless accompanied by three potential effects, which must be carefully considered.

First, a change in f_{EOSC} will result in a proportional change in the internal notch position and in a reduction of the converter differential mode rejection at the power line frequency. In many applications, the subsequent performance degradation can be substantially reduced by relying upon the LTC2485's exceptional common mode rejection and by carefully eliminating common mode to differential mode conversion sources in the input circuit. The user should avoid single-ended input filters and should maintain a very high degree of matching and symmetry in the circuits driving the IN^+ and IN^- pins.

Second, the increase in clock frequency will increase proportionally the amount of sampling charge transferred through the input and the reference pins. If large external input and/or reference capacitors (C_{IN}, C_{REF}) are used, the previous section provides formulae for evaluating the effect of the source resistance upon the converter performance for any value of f_{EOSC}. If small external input and/or reference capacitors (C_{IN}, C_{REF}) are used, the effect of the external source resistance upon the LTC2485 typical performance can be inferred from Figures 14, 15, 16 and 17 in which the horizontal axis is scaled by $307200/f_{EOSC}$.

Third, an increase in the frequency of the external oscillator above 1MHz (a more than 3X increase in the output data rate) will start to decrease the effectiveness of the internal autocalibration circuits. This will result in a progressive degradation in the converter accuracy and linearity. Typical measured performance curves for output data rates up to 100 readings per second are shown in Figures 21 to 28. In order to obtain the highest possible level of accuracy from this converter at output data rates above 20 readings per second, the user is advised to maximize the power supply voltage used and to limit the maximum ambient operating temperature. In certain circumstances, a reduction of the differential reference voltage may be beneficial.

Input Bandwidth

The combined effect of the internal $SINC^4$ digital filter and of the analog and digital autocalibration circuits determines the LTC2485 input bandwidth. When the internal oscillator is used with the notch set at 60Hz, the 3dB input bandwidth is 3.63Hz. When the internal oscillator is used with the notch set at 50Hz, the 3dB input bandwidth is 3.02Hz. If an external conversion clock generator of frequency f_{EOSC} is connected to the $CA0/F_0$ pin, the 3dB input bandwidth is $11.8 \cdot 10^{-6} \cdot f_{EOSC}$.

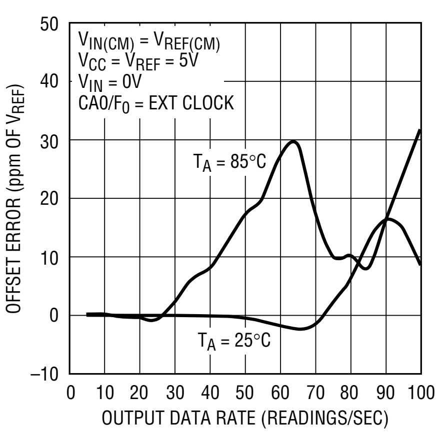


Figure 21. Offset Error vs Output Data Rate and Temperature

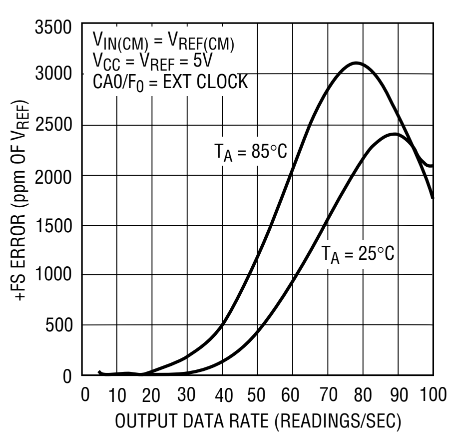


Figure 22. +FS Error vs Output Data Rate and Temperature

APPLICATIONS INFORMATION

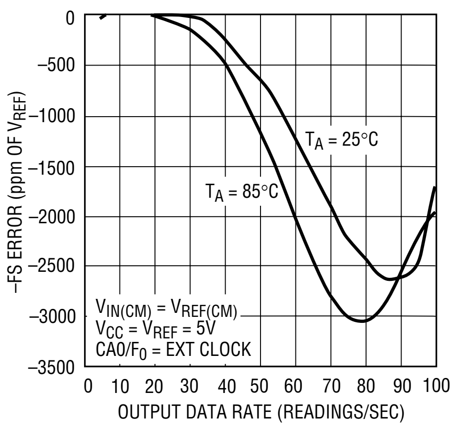


Figure 23. –FS Error vs Output Data Rate and Temperature

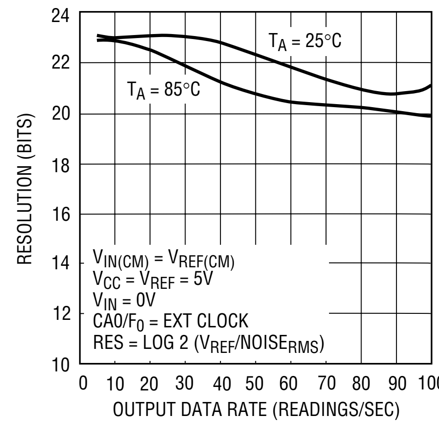


Figure 24. Resolution ($Noise_{RMS} \leq$ 1LSB) vs Output Data Rate and Temperature

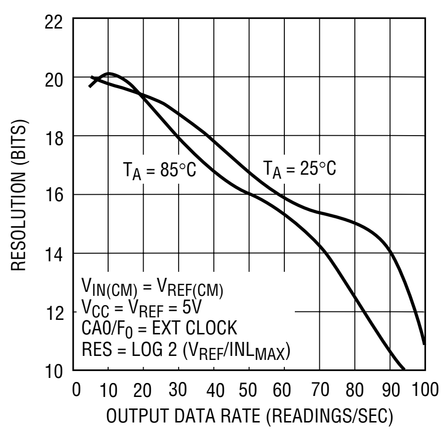


Figure 25. Resolution ($INL_{MAX} \leq$ 1LSB) vs Output Data Rate and Temperature

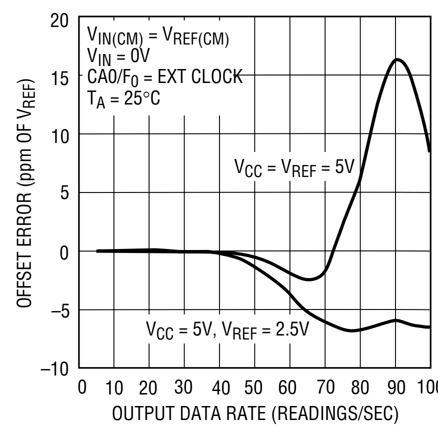


Figure 26. Offset Error vs Output Data Rate and Reference Voltage

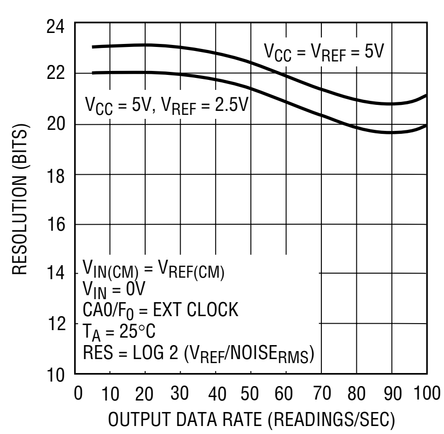


Figure 27. Resolution ($Noise_{RMS} \leq$ 1LSB) vs Output Data Rate and Reference Voltage

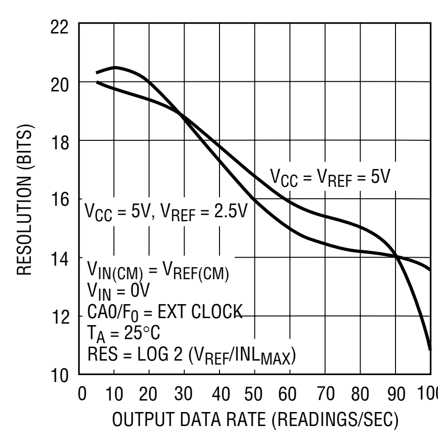


Figure 28. Resolution ($INL_{MAX} \leq$ 1LSB) vs Output Data Rate and Reference Voltage

APPLICATIONS INFORMATION

Due to the complex filtering and calibration algorithms utilized, the converter input bandwidth is not modeled very accurately by a first order filter with the pole located at the 3dB frequency. When the internal oscillator is used, the shape of the LTC2485 input bandwidth is shown in Figure 29. When an external oscillator of frequency f_{EOSC} is used, the shape of the LTC2485 input bandwidth can be derived from Figure 29, 60Hz mode curve in which the horizontal axis is scaled by $f_{EOSC}/307200$.

The conversion noise ($600nV_{RMS}$ typical for $V_{REF} = 5V$) can be modeled by a white noise source connected to a noise free converter. The noise spectral density is 47nV√Hz for an infinite bandwidth source and 64nV√Hz for a single 0.5MHz pole source. From these numbers, it is clear that particular attention must be given to the design of external amplification circuits. Such circuits face the simultaneous requirements of very low bandwidth (just a few Hz) in order to reduce the output referred noise and relatively high bandwidth (at least 500kHz) necessary to drive the input switched-capacitor network. A possible solution is a high gain, low bandwidth amplifier stage followed by a high bandwidth unity-gain buffer.

When external amplifiers are driving the LTC2485, the ADC input referred system noise calculation can be simplified by Figure 30. The noise of an amplifier driving the LTC2485 input pin can be modeled as a band limited white noise source. Its bandwidth can be approximated by the bandwidth of a single pole lowpass filter with a corner frequency f_i. The amplifier noise spectral density is n_i. From Figure 30, using f_i as the x-axis selector, we can find on the y-axis the noise equivalent bandwidth $freq_i$ of the input driving amplifier. This bandwidth includes the band limiting effects of the ADC internal calibration and filtering. The noise of the driving amplifier referred to the converter input and including all these effects can be calculated as $N = n_i \bullet \sqrt{freq_i}$. The total system noise (referred to the LTC2485 input) can now be obtained by summing as square root of sum of squares the three ADC input referred noise sources: the LTC2485 internal noise, the noise of the IN^+ driving amplifier and the noise of the IN^- driving amplifier.

If the $CA0/F_0$ pin is driven by an external oscillator of frequency f_{EOSC}, Figure 30 can still be used for noise calculation if the x-axis is scaled by $f_{EOSC}/307200$. For large values of the ratio $f_{EOSC}/307200$, the Figure 30 plot accuracy begins to decrease, but at the same time the LTC2485 noise floor rises and the noise contribution of the driving amplifiers lose significance.

Normal Mode Rejection and Antialiasing

One of the advantages delta-sigma ADCs offer over conventional ADCs is on-chip digital filtering. Combined with a large oversampling ratio, the LTC2485 significantly simplifies antialiasing filter requirements. Additionally, the input current cancellation feature of the LTC2485 allows external lowpass filtering without degrading the DC performance of the device.

The $SINC^4$ digital filter provides greater than 120dB normal mode rejection at all frequencies except DC and integer multiples of the modulator sampling frequency (f_S). The LTC2485's autocalibration circuits further simplify the antialiasing requirements by additional normal mode signal filtering both in the analog and digital domain. Independent of the operating mode, $f_S = 256 \bullet f_N = 2048 \bullet f_{OUTMAX}$ where f_N is the notch frequency and f_{OUTMAX} is the maximum output data rate. In the internal oscillator mode with a 50Hz notch setting, f_S = 12800Hz, with 50Hz/60Hz rejection, f_S = 13960Hz and with a 60Hz notch setting f_S = 15360Hz. In the external oscillator mode, $f_S = f_{EOSC}/20$. The performance of the normal mode rejection is shown in Figures 31 and 32.

In 1x speed mode, the regions of low rejection occurring at integer multiples of f_S have a very narrow bandwidth. Magnified details of the normal mode rejection curves are shown in Figure 33 (rejection near DC) and Figure 34 (rejection at $f_S = 256f_N$) where f_N represents the notch frequency. These curves have been derived for the external oscillator mode but they can be used in all operating modes by appropriately selecting the f_N value.

APPLICATIONS INFORMATION

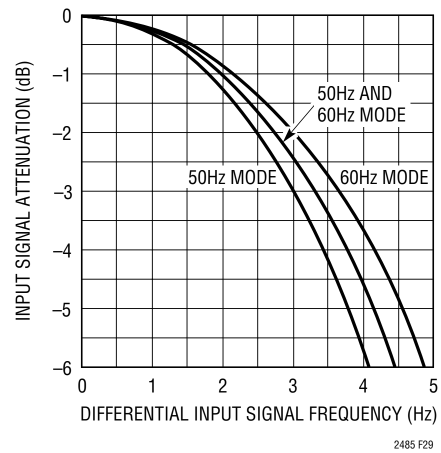


Figure 29. Input Signal Using the Internal Oscillator

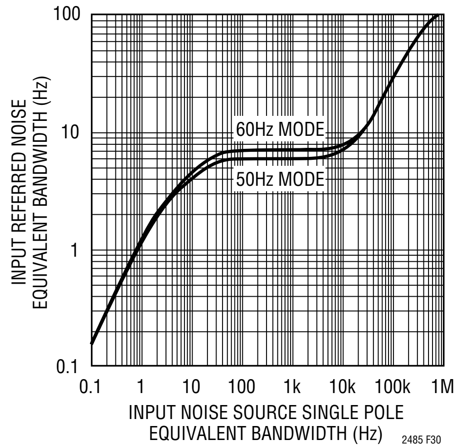


Figure 30. Input Refered Noise Equivalent Bandwidth of an Input Connected White Noise Source

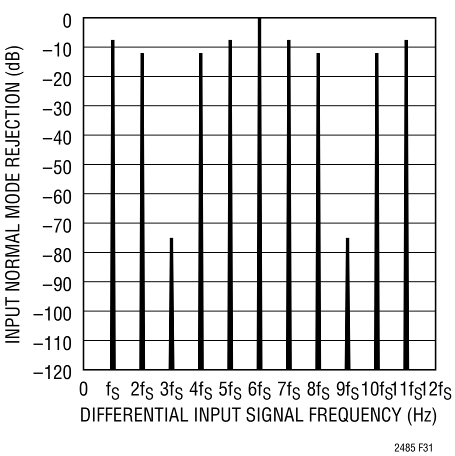


Figure 31. Input Normal Mode Rejection, Internal Oscillator and 50Hz Notch Mode

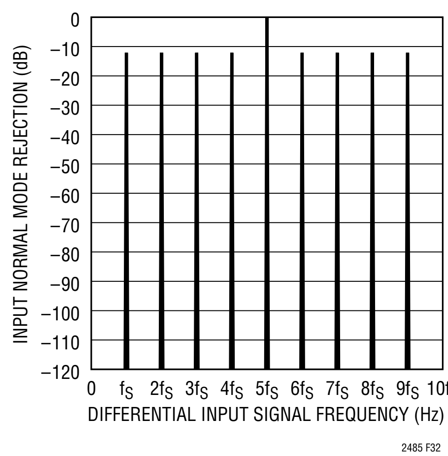


Figure 32. Input Normal Mode Rejection at DC

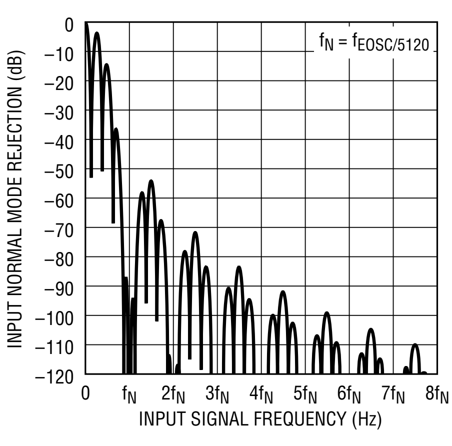


Figure 33. Input Normal Mode Rejection at DC

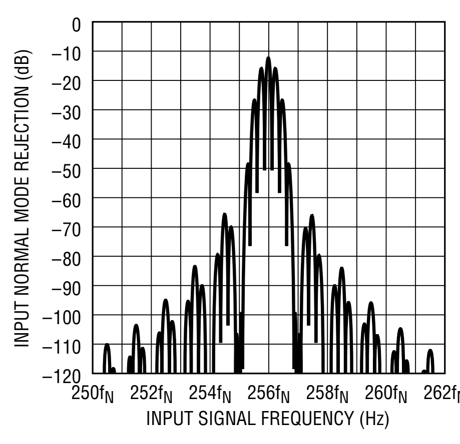


Figure 34. Input Normal Mode Rejection at $f_S = 256f_N$

APPLICATIONS INFORMATION

The user can expect to achieve this level of performance using the internal oscillator as it is demonstrated by Figures 35, 36 and 37. Typical measured values of the normal mode rejection of the LTC2485 operating with an internal oscillator and a 60Hz notch setting are shown in Figure 35 superimposed over the theoretical calculated curve. Similarly, the measured normal mode rejection of the LTC2485 for the 50Hz rejection mode and 50Hz/60Hz rejection mode are shown in Figures 36 and 37.

As a result of these remarkable normal mode specifications, minimal (if any) antialias filtering is required in front of the LTC2485. If passive RC components are placed in front of the LTC2485, the input dynamic current should be considered (see Input Current section). In this case, the differential input current cancellation feature of the LTC2485 allows external RC networks without significant degradation in DC performance.

Traditional high order delta-sigma modulators, while providing very good linearity and resolution, suffer from potential instabilities at large input signal levels. The proprietary architecture used for the LTC2485 third order modulator resolves this problem and guarantees a predictable stable behavior at input signal levels of up to 150% of full scale. In many industrial applications, it is not uncommon to have to measure microvolt level signals superimposed on volt level perturbations and the LTC2485 is eminently suited for such tasks. When the perturbation is differential, the specification of interest is the normal mode rejection for large input signal levels. With a reference voltage V_{REF} = 5V, the LTC2485 has a full-scale differential input range of 5V peak-to-peak. Figures 38 and 39 show measurement results for the LTC2485 normal mode rejection ratio with a 7.5V peak-to-peak (150% of full scale) input signal superimposed over the more traditional normal mode rejection ratio results obtained with a 5V peak-to-peak (full scale) input signal. In Figure 38, the LTC2485 uses the internal oscillator with the notch set at 60Hz and in Figure 39 it uses the internal oscillator with the notch set at 50Hz. It is clear that the LTC2485 rejection performance is maintained with no compromises in this extreme situation. When operating with large input signal levels, the user must observe that such signals do not violate the device absolute maximum ratings.

APPLICATIONS INFORMATION

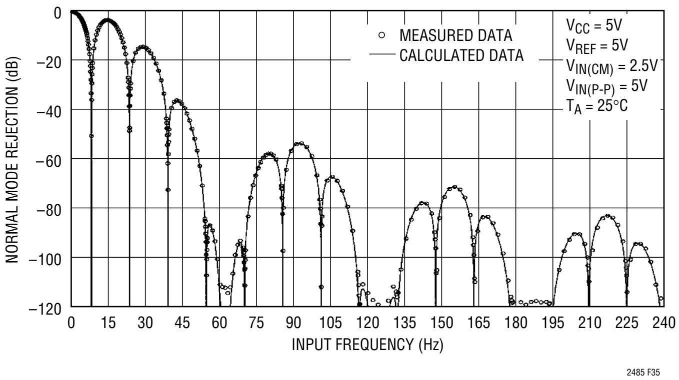


Figure 35. Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 100% Full Scale (60Hz Notch)

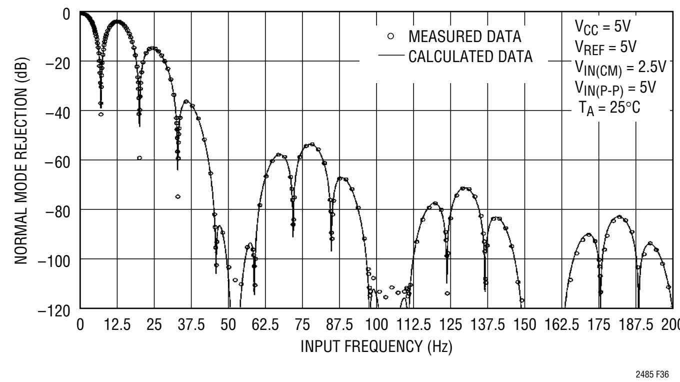


Figure 36. Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 100% Full Scale (50Hz Notch)

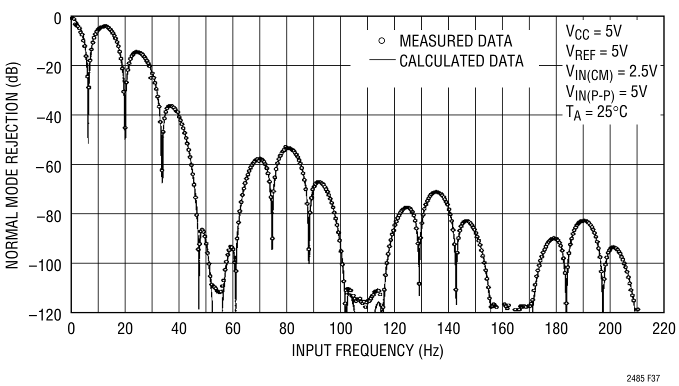


Figure 37. Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 100% Full Scale (50Hz/60Hz Mode)

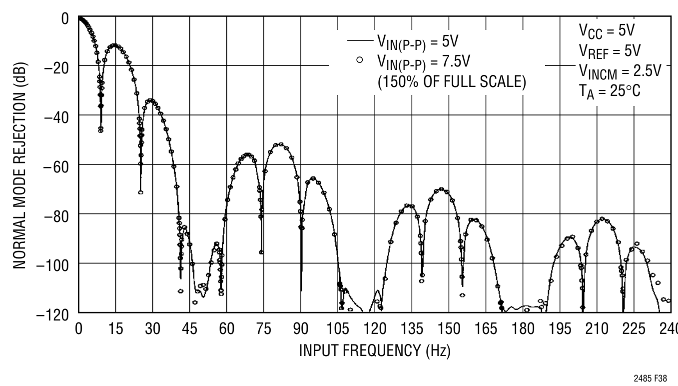


Figure 38. Measured Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 150% Full Scale (60Hz Notch)

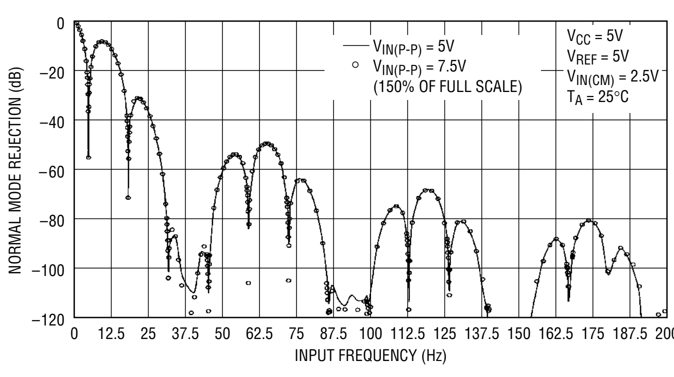


Figure 39. Measured Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 150% Full Scale (50Hz Notch)

APPLICATIONS INFORMATION

Using the 2x speed mode of the LTC2485, the device bypasses the digital offset calibration operation to double the output data rate. The superior normal mode rejection is maintained as shown in Figures 31 and 32. However, the magnified details near DC and $f_S = 256f_N$ are different, see Figures 40 and 41. In 2x speed mode, the bandwidth is 11.4Hz for the 50Hz rejection mode, 13.6Hz for the 60Hz rejection mode and 12.4Hz for the 50Hz/60Hz rejection mode. Typical measured values of the normal mode rejection of the LTC2485 operating with the internal oscillator and 2x speed mode is shown in Figure 42.

When the LTC2485 is configured in 2x speed mode, by performing a running average, a $SINC^1$ notch is combined with the $SINC^4$ digital filter, yielding the normal mode rejection identical as that for the 1x speed mode. The averaging operation still keeps the output rate with the following algorithm:

Result 1 = average (sample 0, sample 1)

Result 2 = average (sample 1, sample 2)

……

Result n = average (sample n – 1, sample n)

The main advantage of the running average is that it achieves simultaneous 50Hz/60Hz rejection at twice the effective output rate, as shown in Figure 43. The raw output data provides a better than 70dB rejection over 48Hz to 62.4Hz, which covers both 50Hz ±2% and 60Hz ±2%. With running average on, the rejection is better than 87dB for both 50Hz ±2% and 60Hz ±2%.

Complete Thermocouple Measurement System with Cold Junction Compensation

The LTC2485 is ideal for direct digitization of thermocouples and other low voltage output sensors. The input has a typical offset error of 500nV (2.5µV max) offset drift of 10nV/°C and a noise level of $600nV_{RMS}$.

Figure 45 (last page of this data sheet) is a complete type K thermocouple meter. The only signal conditioning is a simple surge protection network. In any thermocouple meter, the cold junction temperature sensor must be at the same temperature as the junction between the thermocouple materials and the copper printed circuit board traces. The tiny LTC2485 can be tucked neatly underneath an Omega MPJ-K-F thermocouple socket ensuring close thermal coupling.

The LTC2485's 1.4mV/°C PTAT circuit measures the cold junction temperature. Once the thermocouple voltage and cold junction temperature are known, there are many ways of calculating the thermocouple temperature including a straight-line approximation, lookup tables or a polynomial curve fit. Calibration is performed by applying an accurate 500mV to the ADC input derived from an LT®1236 reference and measuring the local temperature with an accurate thermometer as shown in Figure 44. In calibration mode, the up and down buttons are used to adjust the local temperature reading until it matches an accurate thermometer. Both the voltage and temperature calibration are easily automated.

The complete microcontroller code for this application is available on the LTC2485 product webpage at:

http://www.linear.com

It can be used as a template for may different instruments and it illustrates how to generate calibration coefficients for the onboard temperature sensor. Extensive comments detail the operation of the program. The read_LTC2485() function controls the operation of the LTC2485 and is listed below for reference.

APPLICATIONS INFORMATION

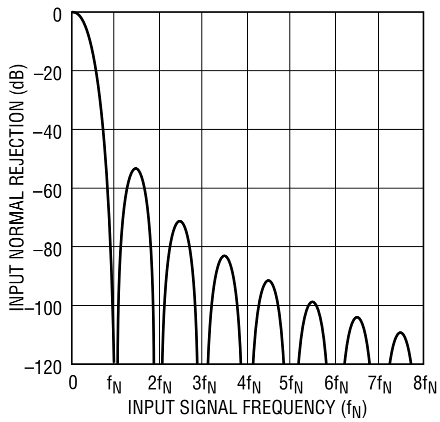


Figure 40. Input Normal Mode Rejection 2x Speed Mode

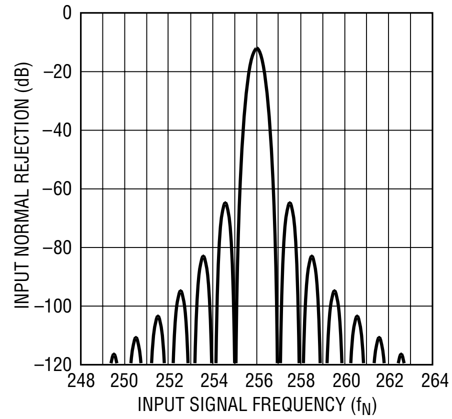


Figure 41. Input Normal Mode Rejection 2x Speed Mode

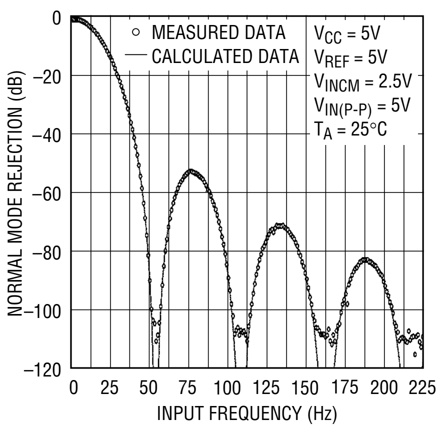


Figure 42. Input Normal Mode Rejection vs Input Frequency, 2x Speed Mode and 50Hz/60Hz Mode

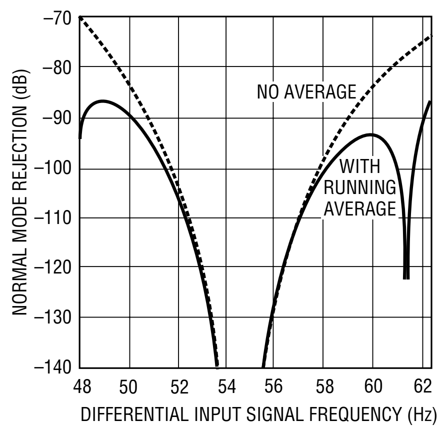


Figure 43. Input Normal Mode Rejection 2x Speed Mode

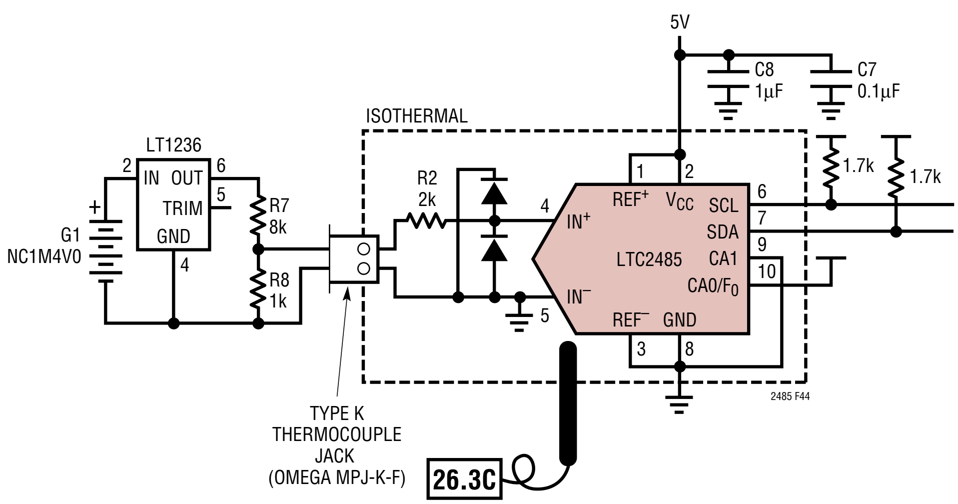


Figure 44. Calibration Setup

APPLICATIONS INFORMATION

```
/*
LTC248X.h
Processor setup and
Lots of useful defines for configuring the LTC2481, LTC2483, and LTC2485.
*/

#include <16F73.h>                              // Device
#use delay(clock=6000000)                       // 6MHz clock
//#fuses NOWDT,HS, PUT, NOPROTECT, NOBROWNOUT   // Configuration fuses
#rom 0x2007={0x3F3A} // Equivalent and more reliable fuse config.

#use I2C(master, sda=PIN_C5, scl=PIN_C3, SLOW)// Set up i2c port
#include “PCM73A.h”                          // Various defines
#include “lcd.c”                             // LCD driver functions

#define READ      0x01           // bitwise OR with address for read or write
#define WRITE     0x00
#define LTC248XADDR 0b01001000   // The one and only LTC248X in this circuit,
                                 // with both address lines floating.

// Useful defines for the LTC2481 and LTC2485 - OR them together to make the
// 8 bit config word.
// These do NOT apply to the LTC2483.

// Select gain - 1 to 256 (also depends on speed setting)
// Does NOT apply to LTC2485.
#define GAIN1  0b00000000   // G = 1   (SPD = 0), G = 1   (SPD = 1)
#define GAIN2  0b00100000   // G = 4   (SPD = 0), G = 2   (SPD = 1)
#define GAIN3  0b01000000   // G = 8   (SPD = 0), G = 4   (SPD = 1)
#define GAIN4  0b01100000   // G = 16  (SPD = 0), G = 8   (SPD = 1)
#define GAIN5  0b10000000   // G = 32  (SPD = 0), G = 16  (SPD = 1)
#define GAIN6  0b10100000   // G = 64  (SPD = 0), G = 32  (SPD = 1)
#define GAIN7  0b11000000   // G = 128 (SPD = 0), G = 64  (SPD = 1)
#define GAIN8  0b11100000   // G = 256 (SPD = 0), G = 128 (SPD = 1)

// Select ADC source - differential input or PTAT circuit
#define VIN    0b00000000
#define PTAT   0b00001000

// Select rejection frequency - 50, 55, or 60Hz
#define R50    0b00000010
#define R55    0b00000000
#define R60    0b00000100

// Select speed mode
#define SLOW   0b00000000 // slow output rate with autozero
#define FAST   0b00000001 // fast output rate with no autozero
```

APPLICATIONS INFORMATION

```
/*
LTC2485.c
Basic voltmeter test program for LTC2485

Reads LTC2485, converts result to volts,
and prints voltage to a 2 line by 16 character LCD display.

Mark Thoren
Linear Technonlgy Corporation
June 23, 2005

Written for CCS PCM compiler, Version 3.182
*/

#include "LTC248X.h"

/*** read_LTC2485() ************************************************************
This is the funciton that actually does all the work of talking to the LTC2485.

Arguments:  addr - device address
            config - configuration bits for next conversion

Returns:    zero if conversion is in progress,
            32 bit signed integer LTC2485 output word.

the i2c_xxxx() functions do the following:

void i2c_start(void): generate an i2c start or repeat start condition
void i2c_stop(void): generate an i2c stop condition
char i2c_read(boolean): return 8 bit i2c data while generating an ack or nack
boolean i2c_write(): send 8 bit i2c data and return ack or nack from slave device

These functions are very compiler specific, and can use either a hardware i2c
port or software emulation of an i2c port. This example uses software emulation.

A good starting point when porting to other processors is to write your own
i2c functions. Note that each processor has its own way of configuring
the i2c port, and different compilers may or may not have built-in functions
for the i2c port.

When in doubt, you can always write a "bit bang" function for troubleshooting
purposes.

The "fourbytes" structure allows byte access to the 32 bit return value:

struct fourbytes  // Define structure of four consecutive bytes
   {              // To allow byte access to a 32 bit int or float.
   int8 te0;      //
   int8 te1;      // The make32() function in this compiler will
   int8 te2;      // also work, but a union of 4 bytes and a 32 bit int
   int8 te3;      // is probably more portable.
   };
```

APPLICATIONS INFORMATION

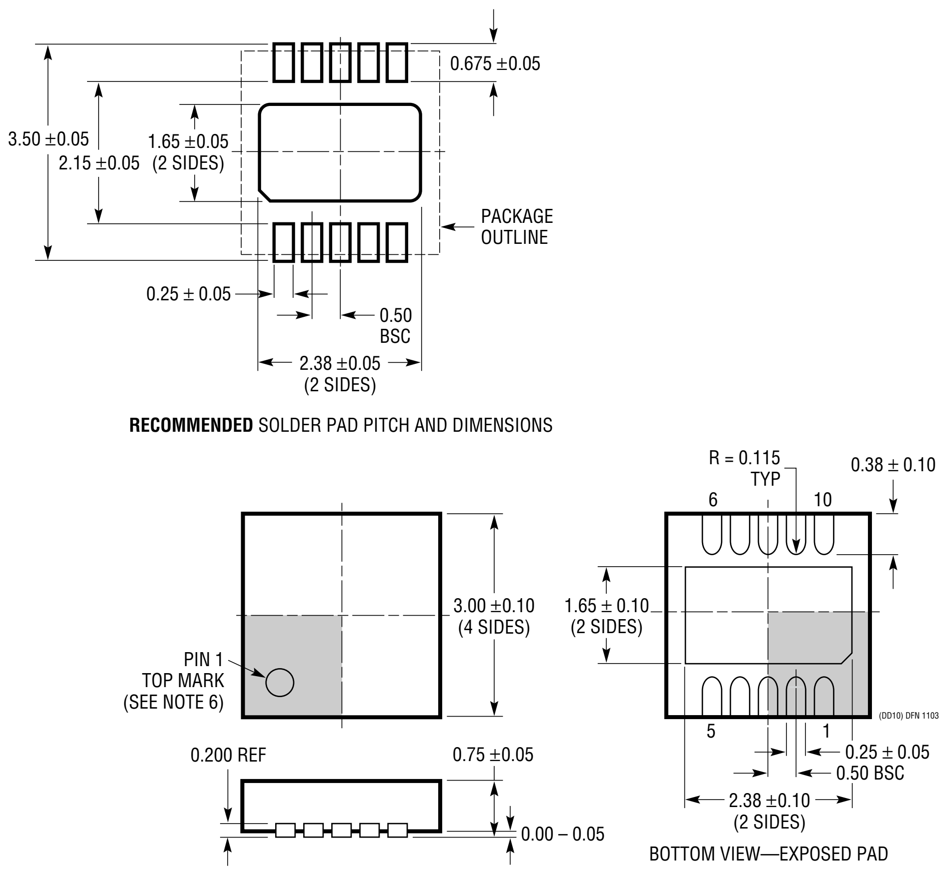
```
******************************************************************************/
signed int32 read_LTC2485(char addr, char config)
   {
   struct fourbytes  // Define structure of four consecutive bytes
      {              // To allow byte access to a 32 bit int or float.
      int8 te0;      //
      int8 te1;      // The make32() function in this compiler will
      int8 te2;      // also work, but a union of 4 bytes and a 32 bit int
      int8 te3;      // is probably more portable.
      };

   union                        // adc_code.bits32    all 32 bits
      {                         // adc_code.by.te0    byte 0
      signed int32 bits32;      // adc_code.by.te1    byte 1
      struct fourbytes by;      // adc_code.by.te2    byte 2
      } adc_code;               // adc_code.by.te3    byte 3

// Start communication with LTC2485:
      i2c_start();
      if(i2c_write(addr | WRITE))// If no acknowledge, return zero
         {
         i2c_stop();
         return 0;
         }
      i2c_write(config);
      i2c_start();
      i2c_write(addr | READ);
      adc_code.by.te3 = i2c_read();
      adc_code.by.te2 = i2c_read();
      adc_code.by.te1 = i2c_read();
      adc_code.by.te0 = i2c_read();
      i2c_stop();
   return adc_code.bits32;
   } // End of read_LTC2485()

/*** initialize() **************************************************************

Basic hardware initialization of controller and LCD, send Hello message to LCD

******************************************************************************/
void initialize(void)
   {
   // General initialization stuff.
   setup_adc_ports(NO_ANALOGS);
   setup_adc(ADC_OFF);
   setup_counters(RTCC_INTERNAL,RTCC_DIV_1);
   setup_timer_1(T1_DISABLED);
   setup_timer_2(T2_DISABLED,0,1);

   lcd_init();                  // Initialize LCD
   delay_ms(6);
   printf(lcd_putc, "Hello!");  // Obligatory hello message
   delay_ms(500);               // for half a second
   } // End of initialize()
```

APPLICATIONS INFORMATION

```
/*** main() ********************************************************************

Main program initializes microcontroller registers, then reads the LTC2481
repeatedly

*******************************************************************************/

void main()
   {
   signed int32 x, y;   // Integer result from LTC2481
   float voltage;    // Variable for floating point math
   int16 timeout;

   initialize();     // Hardware initialization

   while(1)
      {
      delay_ms(1);      // Pace the main loop to something more than 1 ms

// This is a basic error detection scheme. The LTC2485 will never take more than
// 163.5ms, 149.9ms, or 136.5ms to complete a conversion in the 50Hz, 55Hz, and 60Hz
// rejection modes, respectively.
// If read_LTC2485() does not return non-zero within this time period, something
// is wrong, such as an incorrect i2c address or bus conflict.

      if((x = read_LTC2485(LTC248XADDR, VIN | R50 | SLOW)) != 0)
         {
         // No timeout, everything is okay
         timeout = 0;                 // reset timer
         x ^= 0x80000000;             // Invert MSB, result is 2's complement
         voltage = (float) x;                   // convert to float
         voltage = voltage * 5.0 / 2147483648.0;// Multiply by Vref, divide by 2^31
         lcd_putc('\f');                        // Clear screen
         lcd_gotoxy(1,1);                       // Goto home position
         printf(lcd_putc, "%01.6f", voltage); // Display voltage
         }
      else
         {
         ++timeout;
         }

      if(timeout > 200)
         {
         timeout = 200;     // Prevent rollover
         lcd_gotoxy(1,1);
         printf(lcd_putc, "ERROR - TIMEOUT");
         delay_ms(500);
         }
      } // End of main loop
   } // End of main()
```

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

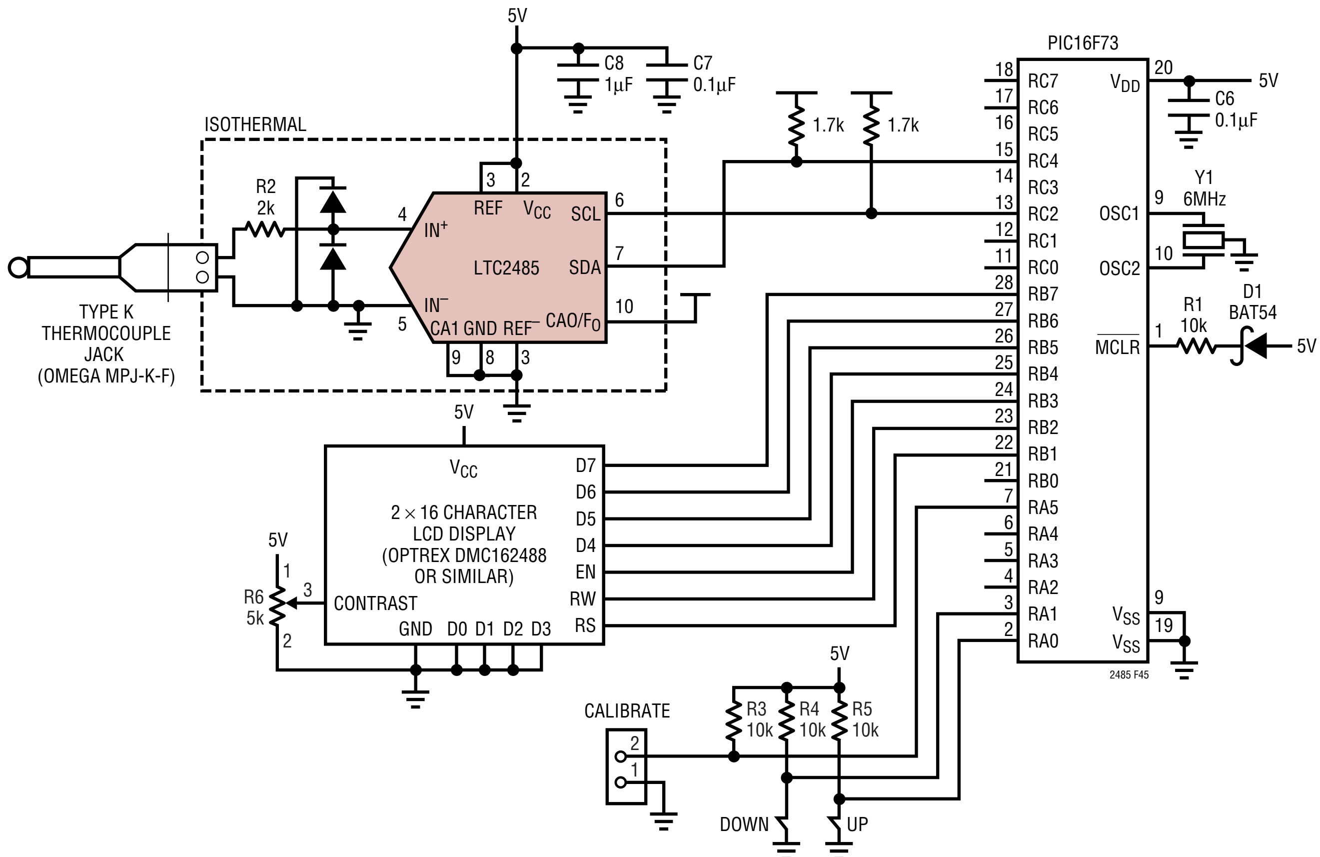


Figure 45. Complete Type K Thermocouple Meter

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1236A-5	Precision Bandgap Reference, 5V	0.05% Max Initial Accuracy, 5ppm/°C Drift
LT1460	Micropower Series Reference	0.075% Max Initial Accuracy, 10ppm/°C Max Drift
LT1790	Micropower SOT-23 Low Dropout Reference Family	0.05% Max Initial Accuracy, 10ppm/°C Max Drift
LTC2400	24-Bit, No Latency $\Delta\Sigma$ ADC in SO-8	0.3ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200µA
LTC2410	24-Bit, No Latency $\Delta\Sigma$ ADC with Differential Inputs	0.8µV_{RMS} Noise, 2ppm INL
LTC2411/LTC2411-1	24-Bit, No Latency $\Delta\Sigma$ ADCs with Differential Inputs in MSOP	1.45µV_{RMS} Noise, 4ppm INL, Simultaneous 50Hz/60Hz Rejection (LTC2411-1)
LTC2413	24-Bit, No Latency $\Delta\Sigma$ ADC with Differential Inputs	Simultaneous 50Hz/60Hz Rejection, 800nV_{RMS} Noise
LTC2415/ LTC2415-1	24-Bit, No Latency $\Delta\Sigma$ ADCs with 15Hz Output Rate	Pin Compatible with the LTC2410
LTC2414/LTC2418	8-/16-Channel 24-Bit, No Latency $\Delta\Sigma$ ADCs	0.2ppm Noise, 2ppm INL, 3ppm Total Unadjusted Errors 200µA
LTC2440	High Speed, Low Noise 24-Bit $\Delta\Sigma$ ADC	3.5kHz Output Rate, 200nV Noise, 24.6 ENOBs
LTC2480	16-Bit $\Delta\Sigma$ ADC with Easy Drive Inputs, 600nV Noise, Programmable Gain, and Temperature Sensor	Pin Compatible with LTC2482/LTC2484
LTC2481	16-Bit $\Delta\Sigma$ ADC with Easy Drive Inputs, 600nV Noise, I^2C Interface, Programmable Gain, and Temperature Sensor	Pin Compatible with LTC2483/LTC2485
LTC2482	16-Bit $\Delta\Sigma$ ADC with Easy Drive Inputs	Pin Compatible with LTC2480/LTC2484
LTC2483	16-Bit $\Delta\Sigma$ ADC with Easy Drive Inputs, and I^2C Interface	Pin Compatible with LTC2481/LTC2485
LTC2484	24-Bit $\Delta\Sigma$ ADC with Easy Drive Inputs	Pin Compatible with LTC2480/LTC2482

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT 0506 REV A • PRINTED IN USA