HEF4027B

Dual JK flip-flop

Rev. 05 — 10 November 2008 **Product data sheet**

1. General description

The HEF4027B is a edge-triggered dual JK flip-flop which features independent set-direct (SD), clear-direct (CD), clock (CP) inputs and outputs (Q, $\overline{Q}$). Data is accepted when CP is LOW, and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct (CD) and set-direct (SD) inputs are independent and override the J, K, and CP inputs. The outputs are buffered for best system performance. Schmitt trigger action makes the clock input highly tolerant of slower rise and fall times.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input. It is also suitable for use over the full industrial (–40 °C to +85 °C) temperature range.

2. Features

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Operates across the full industrial temperature range –40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

3. Applications

- Registers
- Counters
- Control circuits

4. Ordering information

Table 1. Ordering information

T_{amb} from –40 °C to +85 °C.

Type number	Package		
	Name	Description	Version
HEF4027BP	DIP16	plastic dual in-line package; 16-leads (300 mil)	SOT38-4
HEF4027BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Functional diagram

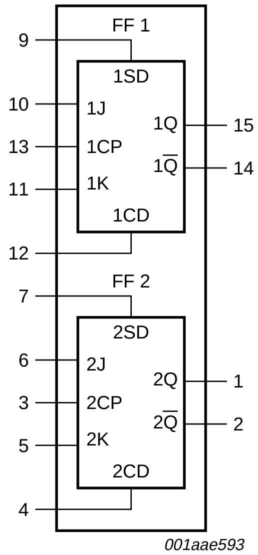


Fig 1. Functional diagram

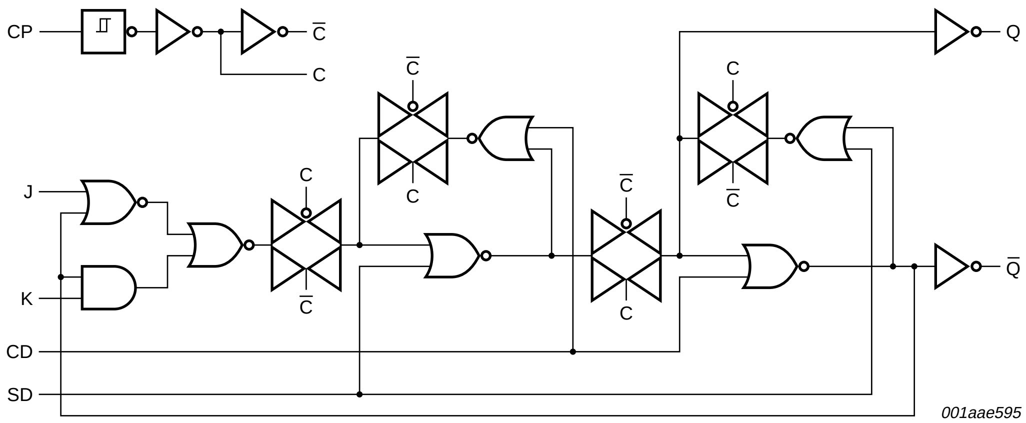


Fig 2. Logic diagram of one flip-flop

6. Pinning information

6.1 Pinning

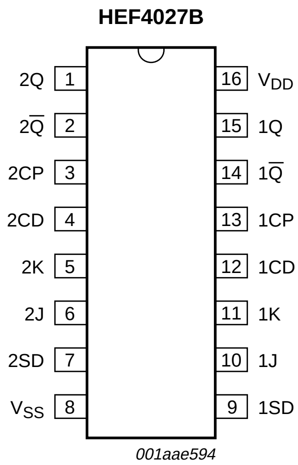


Fig 3. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{SS}	8	ground supply voltage
1SD, 2SD	9, 7	asynchronous set-direct input (active HIGH)
1J, 2J	10, 6	synchronous input
1K, 2K	11, 5	synchronous input
1CD, 2CD	12, 4	asynchronous clear-direct input (active HIGH)
1CP, 2CP	13, 3	clock input (LOW-to-HIGH edge-triggered)
$1\overline{Q}$, $2\overline{Q}$	14, 2	complement output
1Q, 2Q	15, 1	true output
V_{DD}	16	supply voltage

7. Functional description

Table 3. Function table[1]

Inputs					Outputs	
nSD	**nCD**	**nCP**	**nJ**	**nK**	**nQ**	**n$\overline{Q}$**
H	L	X	X	X	H	L
L	H	X	X	X	L	H
H	H	X	X	X	H	H

Table 3. Function table[1] *…continued*

Inputs					Outputs	
nSD	nCD	nCP	nJ	nK	nQ	$n\overline{Q}$
L	L	↑	L	L	no change	no change
L	L	↑	H	L	H	L
L	L	↑	L	H	L	H
L	L	↑	H	H	$n\overline{Q}$	nQ

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.; ↑ = positive-going transition.

8. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+18	V
I_{IK}	input clamping current	V_I < 0.5 V or V_I > V_{DD} + 0.5 V		-	±10	mA
V_I	input voltage			–0.5	V_{DD} + 0.5	V
I_{OK}	output clamping current	V_O < 0.5 V or V_O > V_{DD} + 0.5 V		-	±10	mA
$I_{I/O}$	input/output current			-	±10	mA
I_{DD}	supply current			-	50	mA
T_{stg}	storage temperature			–65	+150	°C
T_{amb}	ambient temperature	in free air		–40	+85	°C
P_{tot}	total power dissipation	T_{amb} –40 °C to +125 °C				
		DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW
P	power dissipation	per output		-	100	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		3	15	V
V_I	input voltage		0	V_{DD}	V
T_{amb}	ambient temperature	in free air	–40	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	3.75	ns/V
		V_{DD} = 10 V	-	0.5	ns/V
		V_{DD} = 15 V	-	0.08	ns/V

10. Static characteristics

Table 6. Static characteristics
V_{SS} = 0 V; V_I = V_{SS} or V_{DD}; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = –40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\| < 1$ µA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\| < 1$ µA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\| < 1$ µA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\| < 1$ µA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	–1.7	-	–1.4	-	–1.1	-	mA
		V_O = 4.6 V	5 V	–0.52	-	–0.44	-	–0.36	-	mA
		V_O = 9.5 V	10 V	–1.3	-	–1.1	-	–0.9	-	mA
		V_O = 13.5 V	15 V	–3.6	-	–3.0	-	–2.4	-	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V_O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	µA
I_{DD}	supply current	I_O = 0 A	5 V	-	4.0	-	4.0	-	30	µA
			10 V	-	8.0	-	8.0	-	60	µA
			15 V	-	16.0	-	16.0	-	120	µA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C; for test circuit see Figure 7; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}		Extrapolation formula[1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	CP → Q, $\overline{Q}$; see Figure 4	5 V		78 ns + (0.55 ns/pF)C_L	-	105	210	ns
			10 V		29 ns + (0.23 ns/pF)C_L	-	40	80	ns
			15 V		22 ns + (0.16 ns/pF)C_L	-	30	60	ns
		CD → Q; see Figure 4	5 V		93 ns + (0.55 ns/pF)C_L	-	120	240	ns
			10 V		33 ns + (0.23 ns/pF)C_L	-	45	90	ns
			15 V		27 ns + (0.16 ns/pF)C_L	-	35	70	ns
		SD → $\overline{Q}$; see Figure 4	5 V		113 ns + (0.55 ns/pF)C_L	-	140	280	ns
			10 V		44 ns + (0.23 ns/pF)C_L	-	55	110	ns
			15 V		32 ns + (0.16 ns/pF)C_L	-	40	80	ns
t_{PLH}	LOW to HIGH propagation delay	CP → Q, $\overline{Q}$; see Figure 4	5 V		58 ns + (0.55 ns/pF)C_L	-	85	170	ns
			10 V		27 ns + (0.23 ns/pF)C_L	-	35	70	ns
			15 V		22 ns + (0.16 ns/pF)C_L	-	30	60	ns
		CD → $\overline{Q}$; see Figure 4	5 V		48 ns + (0.55 ns/pF)C_L	-	75	150	ns
			10 V		24 ns + (0.23 ns/pF)C_L	-	35	70	ns
			15 V		17 ns + (0.16 ns/pF)C_L	-	25	50	ns
		SD → Q; see Figure 4	5 V		43 ns + (0.55 ns/pF)C_L	-	70	140	ns
			10 V		19 ns + (0.23 ns/pF)C_L	-	30	60	ns
			15 V		17 ns + (0.16 ns/pF)C_L	-	25	50	ns
t_t	transition time	see Figure 4	5 V	[2]	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V		9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V		6 ns + (0.28 ns/pF)C_L	-	20	40	ns
t_{su}	set-up time	J, K → CP; see Figure 5	5 V			50	25	-	ns
			10 V			30	10	-	ns
			15 V			20	5	-	ns
t_h	hold time	J, K → CP; see Figure 5	5 V			25	0	-	ns
			10 V			20	0	-	ns
			15 V			15	5	-	ns
t_W	pulse width	CP LOW; minimum width see Figure 5	5 V			80	40	-	ns
			10 V			30	15	-	ns
			15 V			24	12	-	ns
		SD, CD HIGH; minimum width see Figure 6	5 V			90	45	-	ns
			10 V			40	20	-	ns
			15 V			30	15	-	ns
t_{rec}	recovery time	SD, CD inputs; see Figure 6	5 V			+20	–15	-	ns
			10 V			+15	–10	-	ns
			15 V			+10	–5	-	ns

Table 7. Dynamic characteristics *…continued*

V_{SS} = 0 V; T_{amb} = 25 °C; for test circuit see Figure 7; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Typ	Max	Unit
f_{max}	maximum frequency	CP input; J = K = HIGH; see Figure 5	5 V		4	8	-	MHz
			10 V		12	25	-	MHz
			15 V		15	30	-	MHz

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

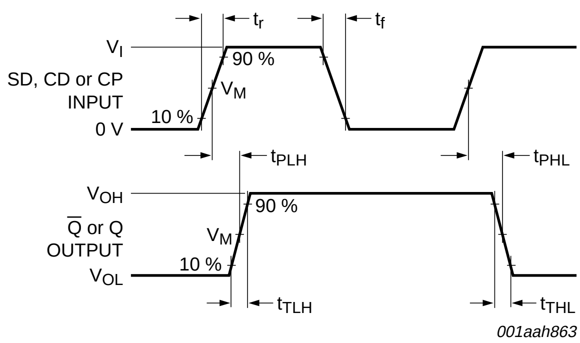
[2] t_t is the same as t_{TLH} and t_{THL}.

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. V_{SS} = 0 V; $t_r = t_f \leq$ 20 ns; T_{amb} = 25 °C.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	Where:
P_D	dynamic power dissipation	5 V	$P_D = 900 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz;
		10 V	$P_D = 4500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz;
		15 V	$P_D = 13200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF;
				V_{DD} = supply voltage in V;
				$\Sigma(C_L \times f_o)$ = sum of the outputs.

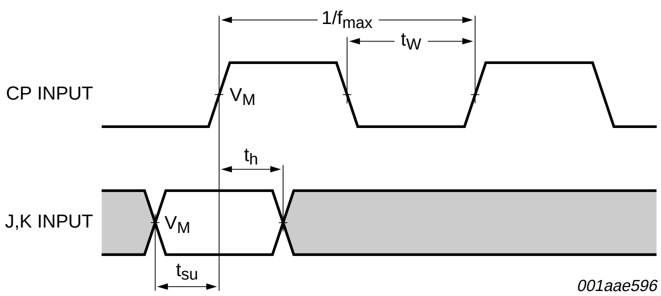
12. Waveforms



V_{OH} and V_{OL} are typical output voltages levels that occur with the output load.

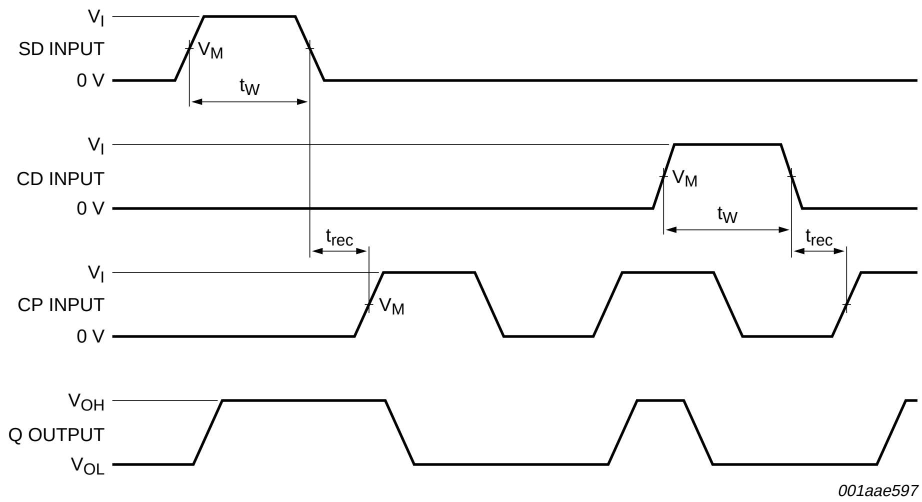
Measurement points are given in Table 9.

Fig 4. Waveforms showing rise, fall and transition times and propagation delays



Measurement points are given in Table 9.

Fig 5. Waveforms showing set-up and hold times and minimum clock pulse width



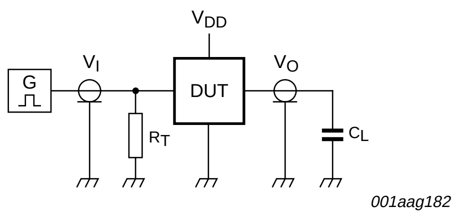
V_{OH} and V_{OL} are typical output voltages levels that occur with the output load.

Measurement points are given in Table 9.

Fig 6. Waveforms showing pulse widths and recovery times

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in Table 10.

Definitions for test circuit:

DUT = Device Under Test.

C_L = load capacitance including jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

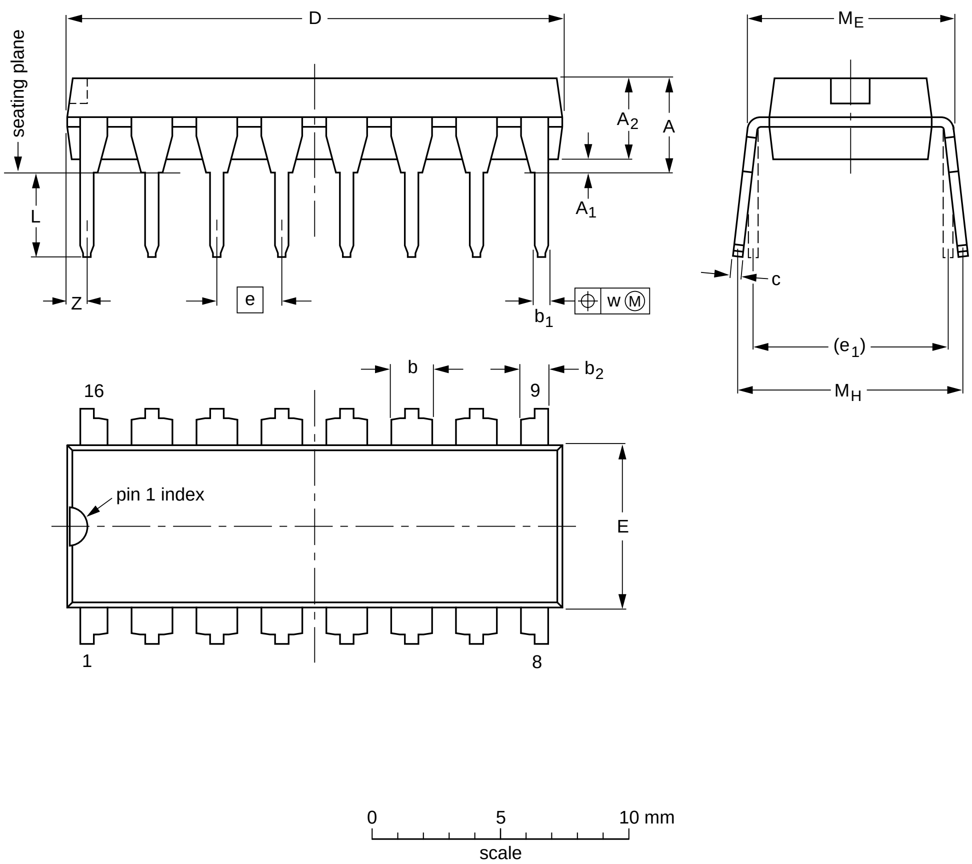
Fig 7. Test circuit

Table 10. Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

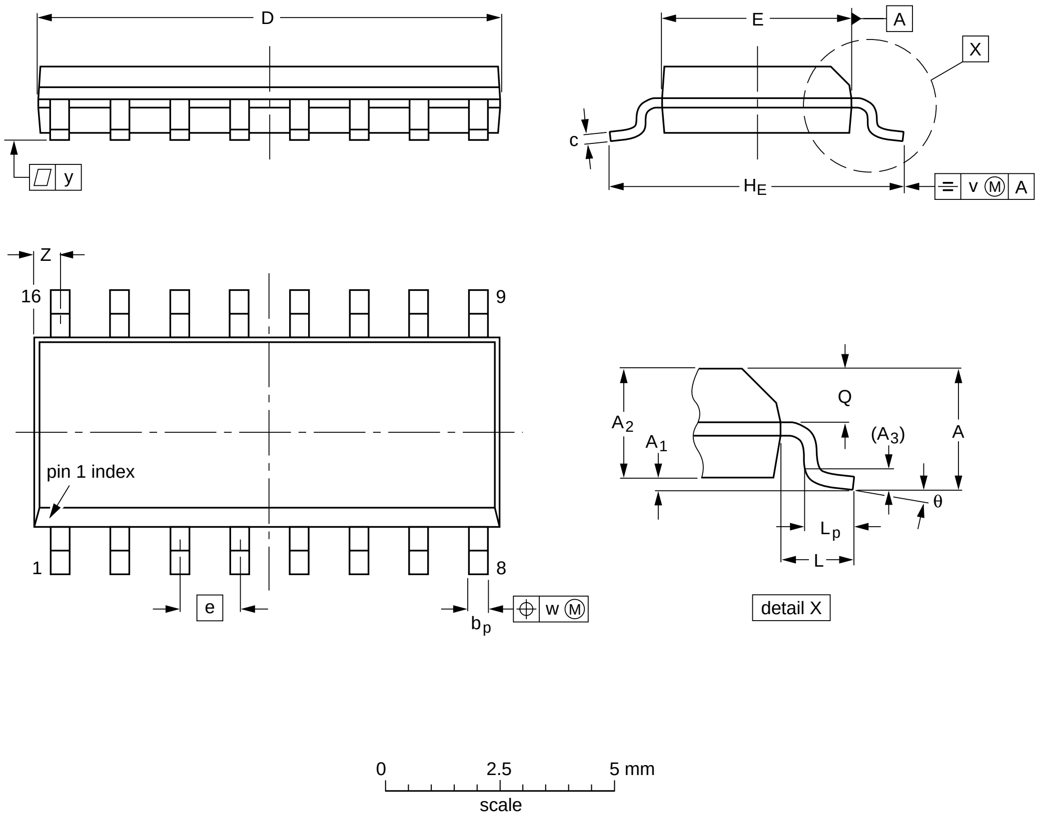
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 8. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^{o} 0^{o}
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT109-1 (SO16)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4027B_5	20081110	Product data sheet	-	HEF4027B_4
Modifications:	• Maximum T_{amb} changed to 85 °C and T_{amb} = 125 °C parameter data removed throughout. • Section 1 "General description" temperature range statement modified. • Section 10 "Static characteristics" I_{DD}, I_{OL}, I_{OH} and I_I values revised.			
HEF4027B_4	20080703	Product specification	-	HEF4027B_CNV_3
HEF4027B_CNV_3	19950101	Product specification	-	HEF4027B_CNV_2
HEF4027B_CNV_2	19950101	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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