CYWB0124AB

West Bridge™ : Antioch™ USB/Mass Storage Peripheral Controller

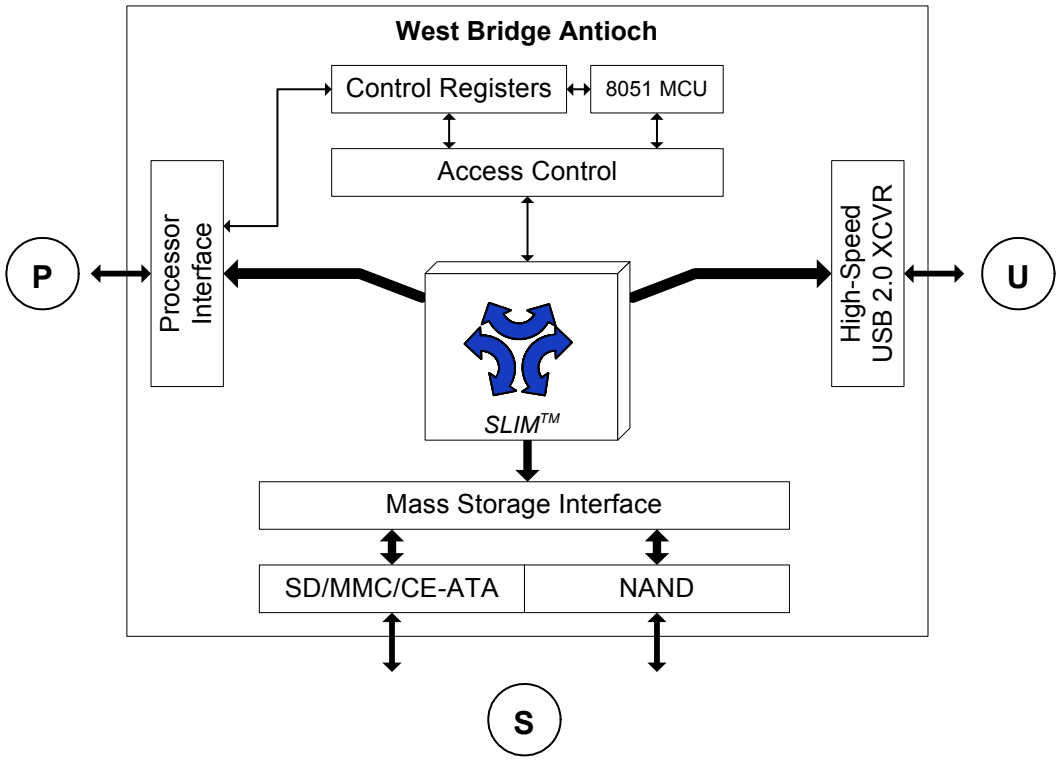
1.0 Features

- *SLIM*™ Architecture, allowing simultaneous and independent data paths between Processor & USB and between USB & Mass Storage
- High-Speed USB at 480 Mbps
  - — USB 2.0 compliant
  - — Integrated USB 2.0 transceiver, smart Serial Interface Engine
  - — 16 programmable endpoints
- Mass Storage device support
  - — MMC/MMC+/SD
  - — NAND flash: x8 or x16, SLC
  - — Full NAND management (ECC, wear-leveling)
- Memory-mapped interface to main processor
- DMA slave support
- Ultra low-power, 1.8V core operation
- Low Power Modes
- Small footprint, 6x6mm VFBGA
- Selectable Clock Input Frequencies
  - — 19.2 MHz, 24 MHz, 26 MHz, 48 MHz

2.0 Applications

- Cellular Phones
- Portable Media Players
- Personal Digital Assistants
- Digital Cameras
- Portable Video Recorder

Figure 1-1. West Bridge Antioch Block Diagram



3.0 Functional Overview

3.1The *SLIM*™ architecture

The Simultaneous Link to Independent Multimedia (SLIM) architecture allows three different interfaces (the P-port, the S-port and the U-port) to connect to one-another independently.

With this architecture, connecting a device using Antioch to a PC through USB does not disturb any of the functions of the device, which can still access Mass storage at the same time the PC is synchronizing with the main processor.

The SLIM architecture enables new usage models, in which a PC can access a Mass storage device independent of the main processor, or enumerate access to both the mass storage and the main processor at the same time.

In a handset, this typically enables the user to use the phone as a thumb drive, or download media files to the phone while still having full functionality available on the phone, or even use the same phone as a modem to connect the PC to the web.

3.2 8051 Microprocessor

The 8051 microprocessor embedded in Antioch does basic transaction management for all the transactions between the P-Port, the S-Port, and the U-Port. The 8051 does not reside in the data path; it manages the path. The data path is optimized for performance. The 8051 executes firmware that supports NAND, SD, and MMC devices at the S-Port. For the NAND device, the 8051 firmware follows the Smart Media algorithm to support:

- Physical to Logical Management
- ECC Correction support
- Wear Leveling
- NAND Flash bad blocks handling

3.2 Configuration and Status Registers

The West Bridge Antioch device includes configuration and status registers that are accessible as memory-mapped registers through the processor interface. The configuration registers allow the system to specify certain behavior of Antioch. For example, it can mask certain status registers from raising an interrupt. The status registers convey various status of Antioch, such as the addresses of buffers for read operations.

3.3 Processor Interface (P-Port)

Communication with the external processor is realized through a dedicated processor interface. This interface supports both synchronous and asynchronous SRAM-mapped memory accesses. This ensures straightforward electrical communications with the processor, which also may have other devices connected on a shared memory bus. Asynchronous accesses can reach a bandwidth of up to 66.7 MBps. Synchronous accesses can be performed at 33 MHz across 16 bits for up to 66.7 MBps bandwidth.

The memory address is decoded to access any of the multiple endpoint buffers inside Antioch. These endpoints serve as buffers for data between each pair of ports, for example, between the processor port and the USB port. The processor writes and reads into these buffers via the memory interface.

Access to these buffers is controlled by either using a DMA protocol or using an interrupt to the main processor. These two modes are configurable by the external processor.

As a DMA slave, Antioch generates a DMA request signal to signify to the main processor that a specific buffer is ready to be read from or written to. The external processor monitors this signal and polls Antioch for the specific buffers ready for read or write. It then performs the appropriate read or write operations on the buffer through the processor interface. This way, the external processor only deals with the buffers to access a multitude of storage devices connected to Antioch.

In the Interrupt mode, Antioch communicates important buffer status changes to the external processor using an interrupt signal. The external processor then polls Antioch for the specific buffers ready for read or write, and it performs the appropriate read or write operations via the processor interface.

3.4 USB Interface (U-Port)

In accordance with the USB 2.0 specification, Antioch can operate in Full-Speed USB mode in addition to High-Speed USB. The USB interface consists of the USB transceiver. The USB interface can access and be accessed by both the P-Port and the S-Port.

The Antioch USB interface supports programmable CONTROL/BULK/INTERRUPT/ISOCHRONOUS endpoints.

3.5 Mass Storage Support (S-Port)

The S-Port can be configured in two different modes, either simultaneously supporting an SD/MMC+ port and a x8 NAND port, or supporting a unique x16 NAND access port. The NANDCFG pin is used to set the configuration of the S-Port to be either 16-bit NAND or 8-bit NAND and SD/MMC. The 16-bit interface can only be used when there is no other mass storage device connected to the S-Port.

Antioch also includes two chip enables, NAND_CE# and NAND_CE2#, which allow two different NANDs to be alternately accessed.

3.5.1NAND Port (S-Port)

Antioch, as part of its mass storage management functions, can fully manage a NAND device. The embedded 8051 manages the actual reading and writing of the NAND, along with its required protocols. It performs standard NAND management functions such as ECC and wear leveling.

SLC NAND devices are supported on all devices in the Antioch family. Write performance for connecting to a single SLC NAND is up to 9 MB/s, while read performance is up to 13 MB/s.

3.5.2SD/MMC Port (S-Port)

When Antioch is configured via NANDCFG to support MMC/SD, this interface supports:

- The Multimedia Card-System Specification, MMCA Technical Committee, Version 4.1
- SD Memory Card Specification - Part 1, Physical Layer Specification, SD Group, Version 1.10, October 15, 2004.

West Bridge Antioch provides support for 1-bit and 4-bit SD cards, as well as 1-bit, 4-bit and 8-bit MMC, and MMC+. For the SD, MMC/MMC Plus, this block supports one card for one physical bus interface.

Antioch supports SD commands including the multi-sector program command that will be handled by the API.