

## Features

- High Performance, Low Power AVR<sup>®</sup> 8-bit Microcontroller
- Advanced RISC Architecture
  - 124 Powerful Instructions - Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 4 MIPS Throughput at 4 MHz
- Nonvolatile Program and Data Memories
  - 4K/8K Bytes of In-System Self-Programmable Flash (ATmega4HVD/8HVD)
  - 256 Bytes EEPROM
  - 512 Bytes Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/ 100,000 EEPROM
  - Data Retention: 20 years at 85°C /100 years at 25°C<sup>(1)</sup>
  - Programming Lock for Software Security
- Battery Management Features
  - One Cell Batteries
  - Short-circuit Protection (Discharge)
  - Over-current Protection (Charge and Discharge)
  - External Protection Input
  - High Voltage Outputs to Drive N-Channel Charge/Discharge FETs
  - Operation with 1 FET or 2 FETs supported
    - Charge FET is optional
  - Battery authentication features (Available only under NDA)
- Peripheral Features
  - Two 8/16-bit Timer/Counters with Separate Prescaler and two output compare units
  - 10-bit ADC with One External Input
  - Two High-voltage open-drain I/O pins
  - Programmable Watchdog Timer
- Special Microcontroller Features
  - debugWIRE On-chip Debug System
  - In-System Programmable
  - Power-on Reset
  - On-chip Voltage Reference with built-in Temperature Sensor
  - On-chip Voltage Regulator
  - External and Internal Interrupt Sources
  - Sleep Modes:
    - Idle, ADC Noise Reduction, Power-save, and Power-off
- Package
  - 18-pad DRDFN/ MLF
- Operating Voltage (VFET): 2.1 - 6.0V
- Operating Voltage (V<sub>CC</sub>): 2.0 - 2.4V
- Maximum Withstand Voltage (VFET): 12V
- Maximum Withstand Voltage (High-voltage pins): 5V
- Temperature Range: -20°C to 85°C
- Speed Grade: 1 - 4 MHz



## 8-bit AVR<sup>®</sup> Microcontroller with 4K/8K Bytes In-System Programmable Flash

ATmega4HVD  
ATmega8HVD

Preliminary

Summary

8052BS-AVR-09/08



## 1. Pin Configurations

Figure 1-1. Dual Row DFN/ MLF-pinout ATmega4HVD/8HVD.

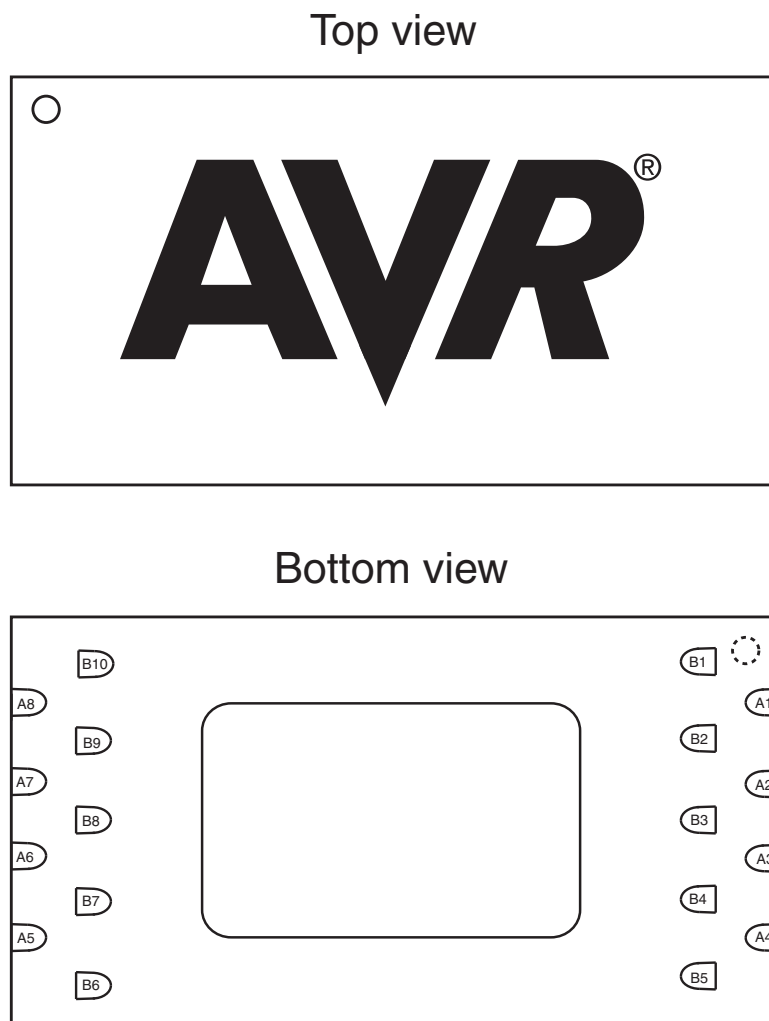


Table 1-1. Dual Row DFN/ MLF-pinout ATmega4HVD/8HVD.

	1	2	3	4	5	6	7	8	9	10
<b>A</b>	DNC	BATT	GND	PV1	PB1 (SCK/ SGND/T0)	DNC	VCC	PC1 (MOSI/INT1/ EXT_PROT)	-	-
<b>B</b>	OD	OC	VFET	VREG	NI	PB0 (ADC0)	PB2 (MISO/CKOUT/T1)	GND	PC0 (INT0/ICP0/XTAL)	RESET

## 1.1 Pin Descriptions

### 1.1.1 VFET

Input to the internal voltage regulator.

### 1.1.2 VCC

Pin for connection of external decoupling capacitor. VCC is internally connected to the voltage regulator output VREG.

### 1.1.3 VREG

Output from the internal voltage regulator. Internally connected to VCC.

### 1.1.4 GND

Ground

### 1.1.5 Port B (PB2:PB0)

Port B is a low-voltage 3-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega4HVD/8HVD.

### 1.1.6 Port C (PC1:PC0)

Port C is a High-voltage open-drain 2 bit bi-directional I/O port. Port C also serves the functions of various special features of the ATmega4HVD/8HVD.

### 1.1.7 OC

High voltage output to drive Charge FET (optional).

### 1.1.8 OD

High voltage output to drive Discharge FET.

### 1.1.9 NI

Negative input from the battery protection resistor.

### 1.1.10 PV1

Input from battery cell to ADC.

### 1.1.11 BATT

Input for detecting when a charger is connected.

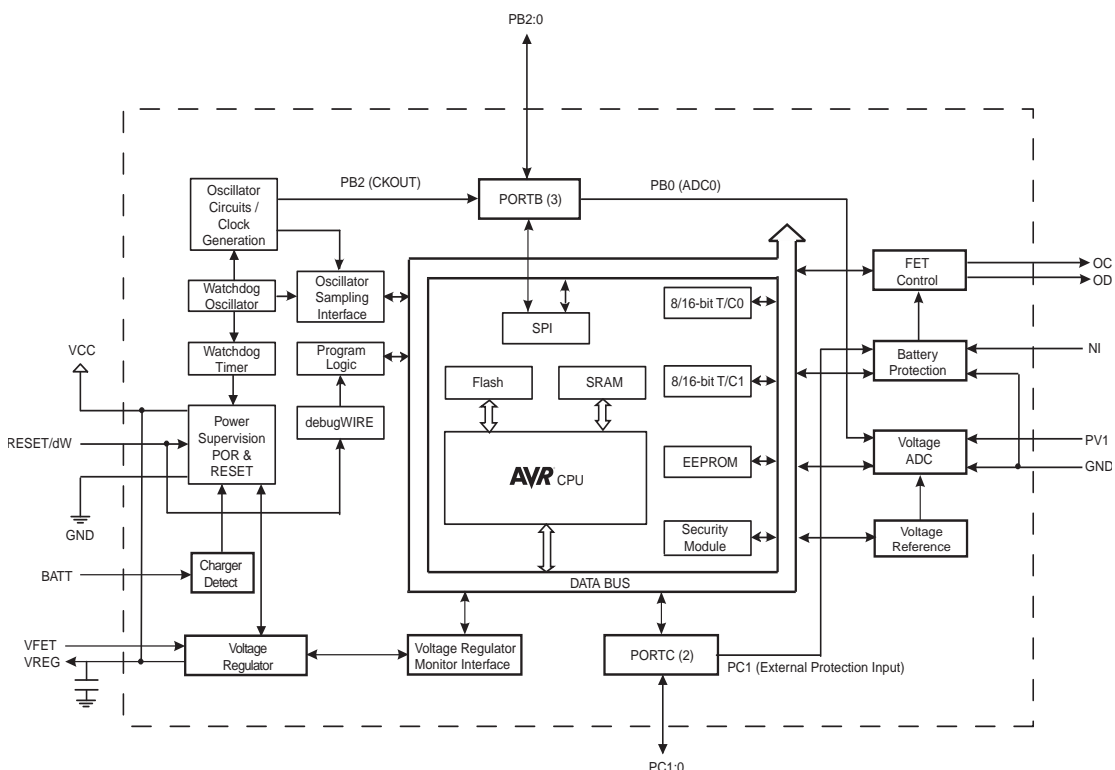
### 1.1.12 $\overline{\text{RESET}}/\text{dw}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset. This pin is also used as debugWIRE communication pin.

## 2. Overview

The ATmega4HVD/8HVD is a monitoring and protection circuit for 1-cell Li-ion applications with focus on high security/authentication, low cost and high utilization of the cell energy. The device contains secure authentication features as well as autonomous battery protection during charging and discharging. The External Protection Input can be used to implement other battery protection mechanisms using external components, e.g. protection against chargers with too high charge voltage can be easily implemented with a few low cost passive components. The feature set makes the ATmega4HVD/8HVD a key component in any system focusing on high security, battery protection, high system utilization and low cost.

**Figure 2-1.** Block Diagram



An integrated, low-dropout linear regulator that can handle input voltages as low as 2.1V, ensures that the stored energy can be fully exploited. The regulator capabilities, combined with an extremely low power consumption in the power saving modes, greatly enhances the cell energy utilization compared to existing solutions.

The chip utilizes Atmel's Deep Under-voltage Recovery (DUVR) mode that supports pre-charging of deeply discharged battery cells without using a separate Pre-charge FET. An enhanced start-up scheme allows the chip to operate correctly even with only Discharge FET connected. This makes it possible to further reduce system cost for applications that do not require Charge Over-current protection.

The ATmega4HVD/8HVD contains a 10-bit ADC for cell voltage measurements. The ADC is also used to monitor the on-chip temperature. Temperature is measured by the integrated Voltage Reference, which contains a built-in temperature sensor. ATmega4HVD/8HVD con-

tains a high-voltage tolerant, open-drain IO pin that supports serial communication. Programming can be done in-system using the 4 General Purpose IO ports that support SPI programming

The MCU includes 4K/8K bytes of In-System Programmable Flash with Self-programming capabilities, 256 bytes EEPROM, 512 bytes SRAM, 32 general purpose working registers, 4 general purpose I/O lines, debugWIRE for On-chip debugging and SPI for In-system Programming, two flexible Timer/Counters with Input Capture, internal and external interrupts, a 10-bit ADC for measuring the cell voltage and on-chip temperature, a programmable Watchdog Timer with wake-up capabilities, and software selectable power saving modes.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The device is manufactured using Atmel's high voltage high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System, by a conventional non-volatile memory programmer or by an On-chip Boot program running on the AVR core.

The ATmega4HVD/8HVD AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, and On-chip Debugger.

The ATmega4HVD/8HVD is a low-power CMOS 8-bit microcontroller based on the AVR architecture. It is part of the AVR Smart Battery family that provides secure authentication, highly accurate monitoring and autonomous protection for Lithium-ion battery cells.

### 3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on <http://www.atmel.com/avr>.

### 4. Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

## 5. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page	
(0xFF)	Reserved	–	–	–	–	–	–	–	–		
(0xFE)	BPPLR	–	–	–	–	–	–	BPPL	BPPL		
(0xFD)	BPCR	–	–	EPID	SCD	DOCD	COCD	–	–		
(0xFC)	Reserved	–	–	–	–	–	–	–	–		
(0xFB)	BPOCTR	–	–	OCTR[5:0]							
(0xFA)	BPSCTR	–	SCTR[6:0]								
(0xF9)	Reserved	–	–	–	–	–	–	–	–		
(0xF8)	Reserved	–	–	–	–	–	–	–	–		
(0xF7)	BPCOCD	COCDL[7:0]									
(0xF6)	BPDOCD	DOCDL[7:0]									
(0xF5)	BPSCD	SCDL[7:0]									
(0xF4)	Reserved	–	–	–	–	–	–	–	–		
(0xF3)	BPIFR	–	–	–	SCIF	DOCIF	COCIF	–	–		
(0xF2)	BPIMSK	–	–	–	SCIE	DOCIE	COCIE	–	–		
(0xF1)	Reserved	–	–	–	–	–	–	–	–		
(0xF0)	FCSR	–	–	–	–	DUVRD	CPS	DFE	CFE		
(0xEF)	Reserved	–	–	–	–	–	–	–	–		
(0xEE)	Reserved	–	–	–	–	–	–	–	–		
(0xED)	Reserved	–	–	–	–	–	–	–	–		
(0xEC)	Reserved	–	–	–	–	–	–	–	–		
(0xEB)	Reserved	–	–	–	–	–	–	–	–		
(0xEA)	Reserved	–	–	–	–	–	–	–	–		
(0xE9)	Reserved	–	–	–	–	–	–	–	–		
(0xE8)	Reserved	–	–	–	–	–	–	–	–		
(0xE7)	Reserved	–	–	–	–	–	–	–	–		
(0xE6)	Reserved	–	–	–	–	–	–	–	–		
(0xE5)	Reserved	–	–	–	–	–	–	–	–		
(0xE4)	Reserved	–	–	–	–	–	–	–	–		
(0xE3)	Reserved	–	–	–	–	–	–	–	–		
(0xE2)	Reserved	–	–	–	–	–	–	–	–		
(0xE1)	Reserved	–	–	–	–	–	–	–	–		
(0xE0)	Reserved	–	–	–	–	–	–	–	–		
(0xDF)	Reserved	–	–	–	–	–	–	–	–		
(0xDE)	Reserved	–	–	–	–	–	–	–	–		
(0xDD)	Reserved	–	–	–	–	–	–	–	–		
(0xDC)	Reserved	–	–	–	–	–	–	–	–		
(0xDB)	Reserved	–	–	–	–	–	–	–	–		
(0xDA)	Reserved	–	–	–	–	–	–	–	–		
(0xD9)	Reserved	–	–	–	–	–	–	–	–		
(0xD8)	Reserved	–	–	–	–	–	–	–	–		
(0xD7)	Reserved	–	–	–	–	–	–	–	–		
(0xD6)	Reserved	–	–	–	–	–	–	–	–		
(0xD5)	Reserved	–	–	–	–	–	–	–	–		
(0xD4)	Reserved	–	–	–	–	–	–	–	–		
(0xD3)	Reserved	–	–	–	–	–	–	–	–		
(0xD2)	Reserved	–	–	–	–	–	–	–	–		
(0xD1)	Reserved	–	–	–	–	–	–	–	–		
(0xD0)	Reserved	–	–	–	–	–	–	–	–		
(0xCF)	Reserved	–	–	–	–	–	–	–	–		
(0xCE)	Reserved	–	–	–	–	–	–	–	–		
(0xCD)	Reserved	–	–	–	–	–	–	–	–		
(0xCC)	Reserved	–	–	–	–	–	–	–	–		
(0xCB)	Reserved	–	–	–	–	–	–	–	–		
(0xCA)	Reserved	–	–	–	–	–	–	–	–		
(0xC9)	Reserved	–	–	–	–	–	–	–	–		
(0xC8)	ROCR	ROCS	–	–	–	–	RSCDEN	RSCWIF	RSCWIE		
(0xC7)	Reserved	–	–	–	–	–	–	–	–		
(0xC6)	Reserved	–	–	–	–	–	–	–	–		
(0xC5)	Reserved	–	–	–	–	–	–	–	–		
(0xC4)	Reserved	–	–	–	–	–	–	–	–		
(0xC3)	Reserved	–	–	–	–	–	–	–	–		
(0xC2)	Reserved	–	–	–	–	–	–	–	–		
(0xC1)	Reserved	–	–	–	–	–	–	–	–		
(0xC0)	Reserved	–	–	–	–	–	–	–	–		



Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page	
(0xBF)	Reserved	-	-	-	-	-	-	-	-		
(0xBE)	Reserved	-	-	-	-	-	-	-	-		
(0xBD)	Reserved	-	-	-	-	-	-	-	-		
(0xBC)	Reserved	-	-	-	-	-	-	-	-		
(0xBB)	Reserved	-	-	-	-	-	-	-	-		
(0xBA)	Reserved	-	-	-	-	-	-	-	-		
(0xB9)	Reserved	-	-	-	-	-	-	-	-		
(0xB8)	Reserved	-	-	-	-	-	-	-	-		
(0xB7)	Reserved	-	-	-	-	-	-	-	-		
(0xB6)	Reserved	-	-	-	-	-	-	-	-		
(0xB5)	Reserved	-	-	-	-	-	-	-	-		
(0xB4)	Reserved	-	-	-	-	-	-	-	-		
(0xB3)	Reserved	-	-	-	-	-	-	-	-		
(0xB2)	Reserved	-	-	-	-	-	-	-	-		
(0xB1)	Reserved	-	-	-	-	-	-	-	-		
(0xB0)	Reserved	-	-	-	-	-	-	-	-		
(0xAF)	Reserved	-	-	-	-	-	-	-	-		
(0xAE)	Reserved	-	-	-	-	-	-	-	-		
(0xAD)	Reserved	-	-	-	-	-	-	-	-		
(0xAC)	Reserved	-	-	-	-	-	-	-	-		
(0xAB)	Reserved	-	-	-	-	-	-	-	-		
(0xAA)	Reserved	-	-	-	-	-	-	-	-		
(0xA9)	Reserved	-	-	-	-	-	-	-	-		
(0xA8)	Reserved	-	-	-	-	-	-	-	-		
(0xA7)	Reserved	-	-	-	-	-	-	-	-		
(0xA6)	Reserved	-	-	-	-	-	-	-	-		
(0xA5)	Reserved	-	-	-	-	-	-	-	-		
(0xA4)	Reserved	-	-	-	-	-	-	-	-		
(0xA3)	Reserved	-	-	-	-	-	-	-	-		
(0xA2)	Reserved	-	-	-	-	-	-	-	-		
(0xA1)	Reserved	-	-	-	-	-	-	-	-		
(0xA0)	Reserved	-	-	-	-	-	-	-	-		
(0x9F)	Reserved	-	-	-	-	-	-	-	-		
(0x9E)	Reserved	-	-	-	-	-	-	-	-		
(0x9D)	Reserved	-	-	-	-	-	-	-	-		
(0x9C)	Reserved	-	-	-	-	-	-	-	-		
(0x9B)	Reserved	-	-	-	-	-	-	-	-		
(0x9A)	Reserved	-	-	-	-	-	-	-	-		
(0x99)	Reserved	-	-	-	-	-	-	-	-		
(0x98)	Reserved	-	-	-	-	-	-	-	-		
(0x97)	Reserved	-	-	-	-	-	-	-	-		
(0x96)	Reserved	-	-	-	-	-	-	-	-		
(0x95)	Reserved	-	-	-	-	-	-	-	-		
(0x94)	Reserved	-	-	-	-	-	-	-	-		
(0x93)	Reserved	-	-	-	-	-	-	-	-		
(0x92)	Reserved	-	-	-	-	-	-	-	-		
(0x91)	Reserved	-	-	-	-	-	-	-	-		
(0x90)	Reserved	-	-	-	-	-	-	-	-		
(0x8F)	Reserved	-	-	-	-	-	-	-	-		
(0x8E)	Reserved	-	-	-	-	-	-	-	-		
(0x8D)	Reserved	-	-	-	-	-	-	-	-		
(0x8C)	Reserved	-	-	-	-	-	-	-	-		
(0x8B)	Reserved	-	-	-	-	-	-	-	-		
(0x8A)	Reserved	-	-	-	-	-	-	-	-		
(0x89)	OCR1B	Timer/Counter1 - Output Compare Register B									
(0x88)	OCR1A	Timer/Counter1 - Output Compare Register A									
(0x87)	Reserved	-	-	-	-	-	-	-	-		
(0x86)	Reserved	-	-	-	-	-	-	-	-		
(0x85)	TCNT1H	Timer/Counter1 - Counter Register High Byte									
(0x84)	TCNT1L	Timer/Counter1 - Counter Register Low Byte									
(0x83)	Reserved	-	-	-	-	-	-	-	-		
(0x82)	Reserved	-	-	-	-	-	-	-	-		
(0x81)	TCCR1B	-	-	-	-	-	CS12	CS11	CS10		
(0x80)	TCCR1A	TCW1	ICEN1	ICNC1	ICES1	ICS1	-	-	WGM10		
(0x7F)	Reserved	-	-	-	-	-	-	-	-		
(0x7E)	DIDR0	-	-	-	-	-	-	-	PB0DID		

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x7D)	Reserved	–	–	–	–	–	–	–	–	
(0x7C)	Reserved	–	–	–	–	–	–	–	–	
(0x7B)	Reserved	–	–	–	–	–	–	–	–	
(0x7A)	ADCSRA	ADEN	ADSC	–	ADIF	ADIE	–	ADMUX1	ADMUX0	
(0x79)	ADCH	–	–	–	–	–	–	ADC9	ADC8	
(0x78)	ADCL	ADC[7:0]								
(0x77)	Reserved	–	–	–	–	–	–	–	–	
(0x76)	Reserved	–	–	–	–	–	–	–	–	
(0x75)	Reserved	–	–	–	–	–	–	–	–	
(0x74)	Reserved	–	–	–	–	–	–	–	–	
(0x73)	Reserved	–	–	–	–	–	–	–	–	
(0x72)	Reserved	–	–	–	–	–	–	–	–	
(0x71)	Reserved	–	–	–	–	–	–	–	–	
(0x70)	Reserved	–	–	–	–	–	–	–	–	
(0x6F)	TIMSK1	–	–	–	–	ICIE1	OCIE1B	OCIE1A	TOIE1	
(0x6E)	TIMSK0	–	–	–	–	ICIE0	OCIE0B	OCIE0A	TOIE0	
(0x6D)	Reserved	–	–	–	–	–	–	–	–	
(0x6C)	Reserved	–	–	–	–	–	–	–	–	
(0x6B)	Reserved	–	–	–	–	–	–	–	–	
(0x6A)	Reserved	–	–	–	–	–	–	–	–	
(0x69)	EICRA	–	–	–	–	ISC11	ISC10	ISC01	ISC00	
(0x68)	Reserved	–	–	–	–	–	–	–	–	
(0x67)	Reserved	–	–	–	–	–	–	–	–	
(0x66)	FOSCCAL	Fast Oscillator Calibration Register								
(0x65)	Reserved	–	–	–	–	–	–	–	–	
(0x64)	PRR0	–	–	PRVRM	–	PRSPI	PRTIM1	PRTIM0	PRADC	
(0x63)	Reserved	–	–	–	–	–	–	–	–	
(0x62)	Reserved	–	–	–	–	–	–	–	–	
(0x61)	CLKPR	CLKPCE	–	–	–	–	–	CLKPS1	CLKPS0	
(0x60)	WDTCR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	
0x3E (0x5E)	SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
0x3C (0x5C)	Reserved	–	–	–	–	–	–	–	–	
0x3B (0x5B)	Reserved	–	–	–	–	–	–	–	–	
0x3A (0x5A)	Reserved	–	–	–	–	–	–	–	–	
0x39 (0x59)	Reserved	–	–	–	–	–	–	–	–	
0x38 (0x58)	Reserved	–	–	–	–	–	–	–	–	
0x37 (0x57)	SPMCSR	–	–	SIGRD	CTPB	RFLB	PGWRT	PGERS	SPMEN	
0x36 (0x56)	Reserved	–	–	–	–	–	–	–	–	
0x35 (0x55)	MCUCR	–	–	CKOE	PUD	–	–	–	–	
0x34 (0x54)	MCUSR	–	–	–	OCDRF	WDRF	–	EXTRF	PORF	
0x33 (0x53)	SMCR	–	–	–	–	SM2	SM1	SM0	SE	
0x32 (0x52)	Reserved	–	–	–	–	–	–	–	–	
0x31 (0x51)	DWDR	debugWIRE Data Register								
0x30 (0x50)	Reserved	–	–	–	–	–	–	–	–	
0x2F (0x4F)	Reserved	–	–	–	–	–	–	–	–	
0x2E (0x4E)	Reserved	–	–	–	–	–	–	–	–	
0x2D (0x4D)	Reserved	–	–	–	–	–	–	–	–	
0x2C (0x4C)	Reserved	–	–	–	–	–	–	–	–	
0x2B (0x4B)	GPIOR2	General Purpose I/O Register 2								
0x2A (0x4A)	GPIOR1	General Purpose I/O Register 1								
0x29 (0x49)	OCR0B	Timer/Counter0 - Output Compare Register A								
0x28 (0x48)	OCR0A	Timer/Counter0 - Output Compare Register B								
0x27 (0x47)	TCNT0H	Timer/Counter0 - Counter Register High Byte								
0x26 (0x46)	TCNT0L	Timer/Counter0 - Counter Register Low Byte								
0x25 (0x45)	TCCR0B	–	–	–	–	–	CS02	CS01	CS00	
0x24 (0x44)	TCCR0A	TCW0	ICEN0	ICNC0	ICES0	ICS0	–	–	WGM00	
0x23 (0x43)	GTCCR	TSM	–	–	–	–	–	–	PSR	
0x22 (0x42)	Reserved	–	–	–	–	–	–	–	–	
0x21 (0x41)	EEARL	EEPROM Address Register								
0x20 (0x40)	EEDR	EEPROM Data Register								
0x1F (0x3F)	EECR	–	–	EEDM1	EEDM0	EERIE	EEMPE	EEPE	EERE	
0x1E (0x3E)	GPIOR0	General Purpose I/O Register 0								
0x1D (0x3D)	EIMSK	–	–	–	–	–	–	INT1	INT0	
0x1C (0x3C)	EIFR	–	–	–	–	–	–	INTF1	INTF0	



Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x1B (0x3B)	Reserved	–	–	–	–	–	–	–	–	
0x1A (0x3A)	Reserved	–	–	–	–	–	–	–	–	
0x19 (0x39)	Reserved	–	–	–	–	–	–	–	–	
0x18 (0x38)	Reserved	–	–	–	–	–	–	–	–	
0x17 (0x37)	OSICSR	–	–	–	OSISELO	–	–	OSIST	OSIEN	
0x16 (0x36)	TIFR1	–	–	–	–	ICF1	OCF1B	OCF1A	TOV1	
0x15 (0x35)	TIFR0	–	–	–	–	ICF0	OCF0B	OCF0A	TOV0	
0x14 (0x34)	Reserved	–	–	–	–	–	–	–	–	
0x13 (0x33)	Reserved	–	–	–	–	–	–	–	–	
0x12 (0x32)	Reserved	–	–	–	–	–	–	–	–	
0x11 (0x31)	Reserved	–	–	–	–	–	–	–	–	
0x10 (0x30)	Reserved	–	–	–	–	–	–	–	–	
0x0F (0x2F)	Reserved	–	–	–	–	–	–	–	–	
0x0E (0x2E)	Reserved	–	–	–	–	–	–	–	–	
0x0D (0x2D)	Reserved	–	–	–	–	–	–	–	–	
0x0C (0x2C)	Reserved	–	–	–	–	–	–	–	–	
0x0B (0x2B)	Reserved	–	–	–	–	–	–	–	–	
0x0A (0x2A)	Reserved	–	–	–	–	–	–	–	–	
0x09 (0x29)	Reserved	–	–	–	–	–	–	–	–	
0x08 (0x28)	PORTC	–	–	–	–	–	–	PORTC1	PORTC0	
0x07 (0x27)	Reserved	–	–	–	–	–	–	–	–	
0x06 (0x26)	PINC	–	–	–	–	–	–	PINC1	PINC0	
0x05 (0x25)	PORTB	–	–	–	–	–	PORTB2	PORTB1	PORTB0	
0x04 (0x24)	DDRB	–	–	–	–	–	DDB2	DDB1	DDB0	
0x03 (0x23)	PINB	–	–	–	–	–	PINB2	PINB1	PINB0	
0x02 (0x22)	Reserved	–	–	–	–	–	–	–	–	
0x01 (0x21)	Reserved	–	–	–	–	–	–	–	–	
0x00 (0x20)	Reserved	–	–	–	–	–	–	–	–	

- Notes:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
  2. I/O registers within the address range \$00 - \$1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
  3. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
  4. When using the I/O specific commands IN and OUT, the I/O addresses \$00 - \$3F must be used. When addressing I/O registers as data space using LD and ST instructions, \$20 must be added to these addresses. The ATmega4HVD/8HVD is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from \$60 - \$FF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

## 6. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
<b>ARITHMETIC AND LOGIC INSTRUCTIONS</b>					
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	RdI,K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	RdI,K	Subtract Immediate from Word	$Rdh:Rdl \leftarrow Rdh:Rdl - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow 0x00 - Rd$	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (0xFF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow 0xFF$	None	1
MUL	Rd, Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULS	Rd, Rr	Multiply Signed	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	$R1:R0 \leftarrow (Rd \times Rr) \lll 1$	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	$R1:R0 \leftarrow (Rd \times Rr) \lll 1$	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	$R1:R0 \leftarrow (Rd \times Rr) \lll 1$	Z,C	2
<b>BRANCH INSTRUCTIONS</b>					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
JMP	k	Direct Jump	$PC \leftarrow k$	None	3
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	3
CALL	k	Direct Subroutine Call	$PC \leftarrow k$	None	4
RET		Subroutine Return	$PC \leftarrow STACK$	None	4
RETI		Interrupt Return	$PC \leftarrow STACK$	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) $PC \leftarrow PC + 2$ or 3	None	1/2/3
CP	Rd,Rr	Compare	$Rd - Rr$	Z, N, V, C, H	1
CPC	Rd,Rr	Compare with Carry	$Rd - Rr - C$	Z, N, V, C, H	1
CPI	Rd,K	Compare Register with Immediate	$Rd - K$	Z, N, V, C, H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) $PC \leftarrow PC + 2$ or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N $\oplus$ V = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N $\oplus$ V = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then $PC \leftarrow PC + k + 1$	None	1/2

Mnemonics	Operands	Description	Operation	Flags	#Clocks
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1/2
<b>BIT AND BIT-TEST INSTRUCTIONS</b>					
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0) ← C, Rd(n+1) ← Rd(n), C ← Rd(7)	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	Rd(7) ← C, Rd(n) ← Rd(n+1), C ← Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0) ← Rd(7..4), Rd(7..4) ← Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
<b>DATA TRANSFER INSTRUCTIONS</b>					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, -X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, -Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd, Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	-X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	-Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q, Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q, Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	Rd ← (Z), Z ← Z+1	None	3
SPM		Store Program Memory	(Z) ← R1:R0	None	-
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1

Mnemonics	Operands	Description	Operation	Flags	#Clocks
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
<b>MCU CONTROL INSTRUCTIONS</b>					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

## 7. Ordering Information

### 7.1 ATmega4HVD

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
1 - 4 MHz	2.0 - 2.4V	ATmega4HVD-4MX	18M1	-20 - 85°C

Note: This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

Package Type	
<b>18M1</b>	18-pad (Staggered Dual-row) 6.5 x 3.5 x 0.80 mm Body. 3.20 x 2.00 mm Exposed Pad, (MLF)

## 7.2 ATmega8HVD

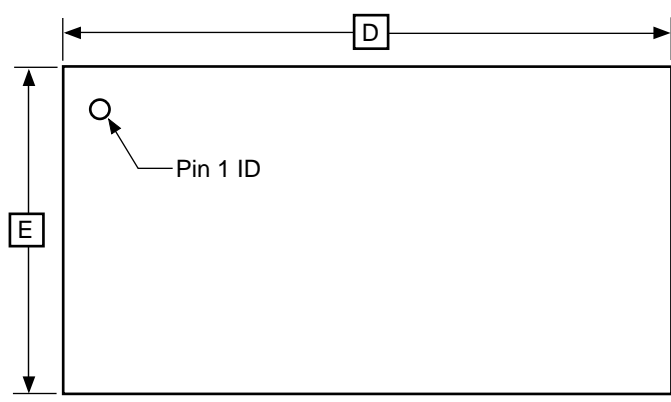
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
1 - 4 MHz	2.0 - 2.4V	ATmega8HVD-4MX	18M1	-20 - 85°C

Note: This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

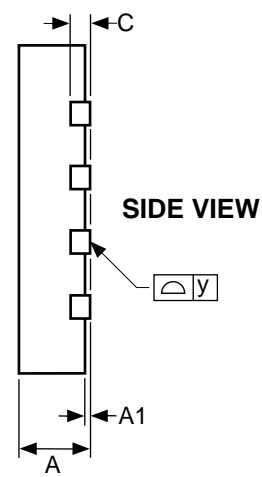
Package Type	
<b>18M1</b>	18-pad (Staggered Dual-row) 6.5 x 3.5 x 0.80 mm Body. 3.20 x 2.00 mm Exposed Pad, (MLF)

## 8. Packaging Information

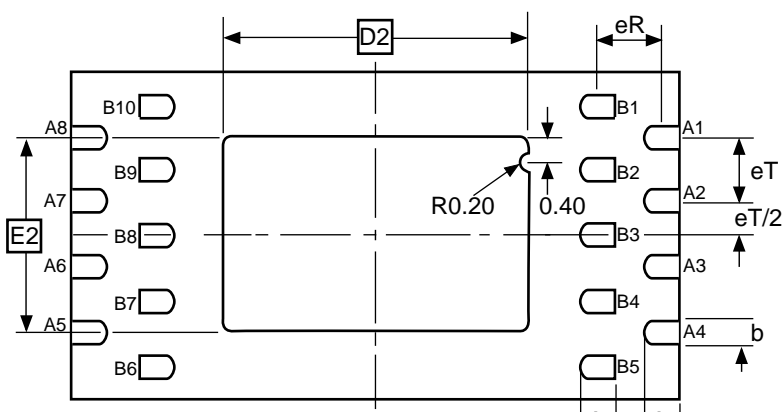
### 8.1 18M1



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.70	0.75	0.80	
A1	0.00	0.02	0.05	
b	0.23	0.28	0.33	
C	0.20 REF			
D	6.40	6.50	6.60	
D2	3.15	3.20	3.25	
E	3.40	3.50	3.60	
E2	1.95	2.00	2.05	
eT	-	0.70	-	
eR	-	0.70	-	
L	0.35	0.40	0.45	
y	0.00	-	0.075	

Note: 1. The terminal #1 ID is a Laser-marked Feature.

3/21/07

**ATMEL** 2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**  
**18M1**, 18-pad (Staggered Dual-row), 6.5 x 3.5 x 0.80 mm Body,  
3.20 x 2.00 mm Exposed Pad, MicroLeadFrame® Package (MLF)

**DRAWING NO.**  
18M1

**REV.**  
B

## 9. Errata

### 9.1 ATmega4HVD

#### 9.1.1 All revisions

No known errata.

### 9.2 ATmega8HVD

#### 9.2.1 All revisions

No known errata.



## 10. Datasheet Revision History

### 10.1 Rev. B - 09/08

1. Updated [Table 20-2 on page 110](#) and [Table 20-3 on page 111](#) in the Register summary of section of "Battery Protection" on [page 104](#).

### 10.2 Rev.A - 09/08

1. Initial revision.



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