



# N-Channel 20-V (D-S), 175 °C MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ)
20	0.0033 at V <sub>GS</sub> = 10 V	40	30 nC
	0.0044 at V <sub>GS</sub> = 4.5 V	40	

### FEATURES

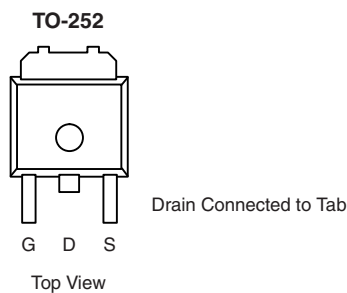
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> Tested



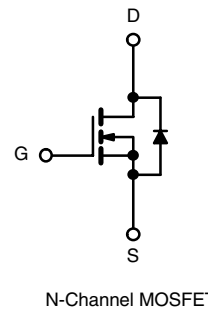
RoHS COMPLIANT

### APPLICATIONS

- Server



Order Number:  
SUD40N02-3m3P-E3 (Lead (Pb)-free)



ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	40 <sup>a</sup>
		T <sub>C</sub> = 100 °C	40 <sup>a</sup>
		T <sub>A</sub> = 25 °C	24.4 <sup>b</sup>
		T <sub>A</sub> = 100 °C	17.2 <sup>b</sup>
Pulsed Drain Current	I <sub>DM</sub>	100	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	
		T <sub>A</sub> = 25 °C	2.8 <sup>b</sup>
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	79
		T <sub>C</sub> = 100 °C	39.5
		T <sub>A</sub> = 25 °C	3.3 <sup>b</sup>
		T <sub>A</sub> = 100 °C	1.6 <sup>b</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b</sup>	Steady State	R <sub>thJA</sub>	37	45	°C/W
Maximum Junction-to-Case	Steady State	R <sub>thJC</sub>	1.5	1.9	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		21		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 6.9		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1		3	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 100\text{ }^\circ\text{C}$			20	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.0027	0.0033	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		0.0036	0.0044	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		100		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		6520		pF
Output Capacitance	$C_{oss}$			1430		
Reverse Transfer Capacitance	$C_{rss}$			770		
Total Gate Charge	$Q_g$	$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		105	160	nC
				50	75	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 50\text{ A}$		17		nC
Gate-Drain Charge	$Q_{gd}$			14		
Gate Resistance	$R_g$		$f = 1\text{ MHz}$		1.2	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 0.2\text{ }\Omega$ $I_D \cong 50\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		40	60	ns
Rise Time	$t_r$			30	45	
Turn-Off Delay Time	$t_{d(off)}$			67	101	
Fall Time	$t_f$			33	50	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 0.2\text{ }\Omega$ $I_D \cong 50\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		13	20	ns
Rise Time	$t_r$			7	11	
Turn-Off Delay Time	$t_{d(off)}$			40	60	
Fall Time	$t_f$			9	14	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			40	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				100	
Body Diode Voltage	$V_{SD}$	$I_S = 20\text{ A}$		0.81	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		38	57	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			34	51	nC
Reverse Recovery Fall Time	$t_a$			18		ns
Reverse Recovery Rise Time	$t_b$			20		

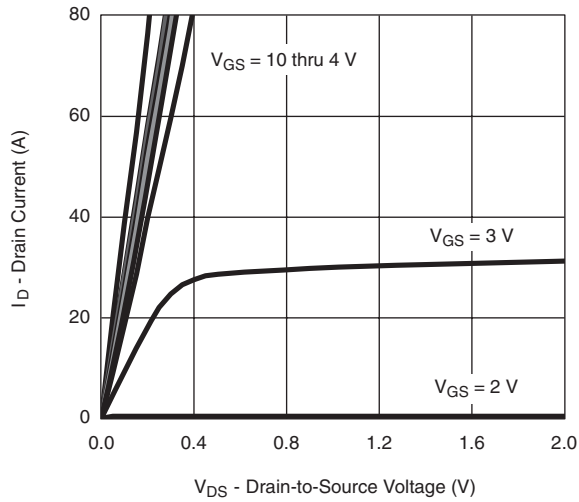
Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

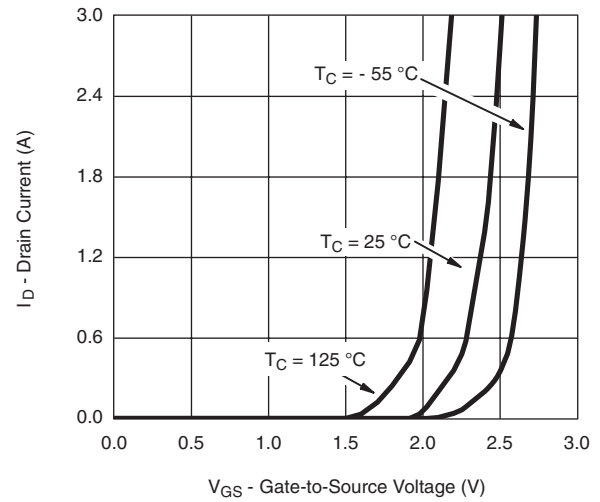
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



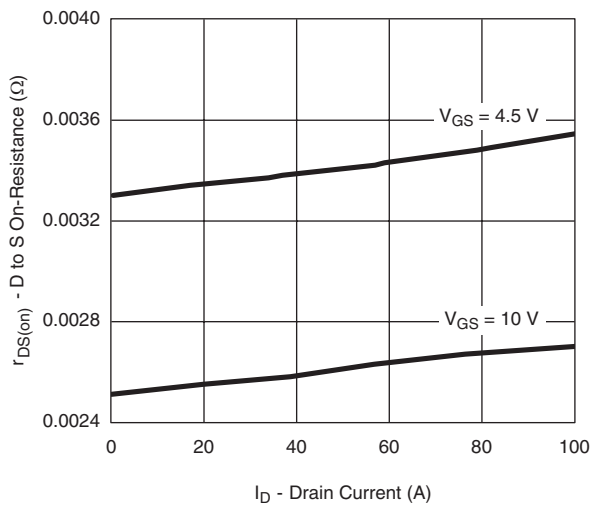
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



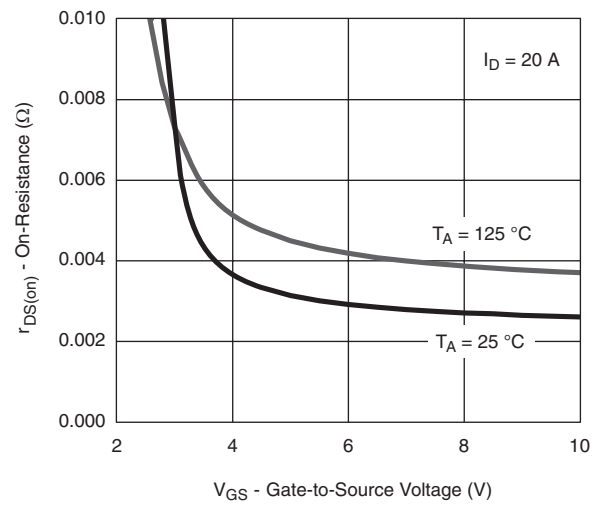
**Output Characteristics**



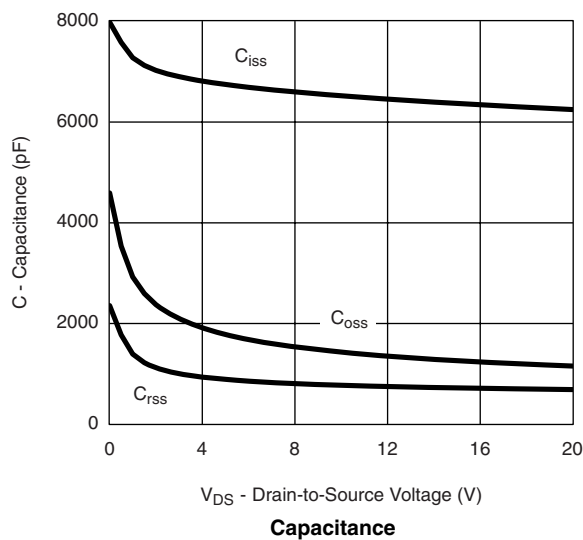
**Transfer Characteristics**



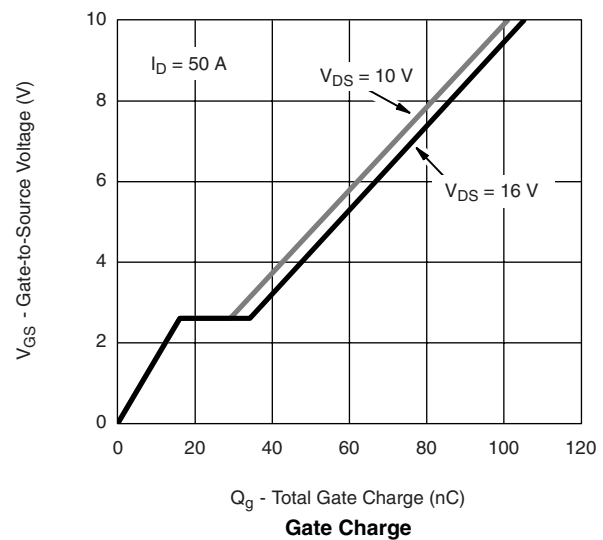
**On-Resistance vs. Drain Current**



**On-Resistance vs.  $V_{GS}$  vs. Temperature**



**Capacitance**



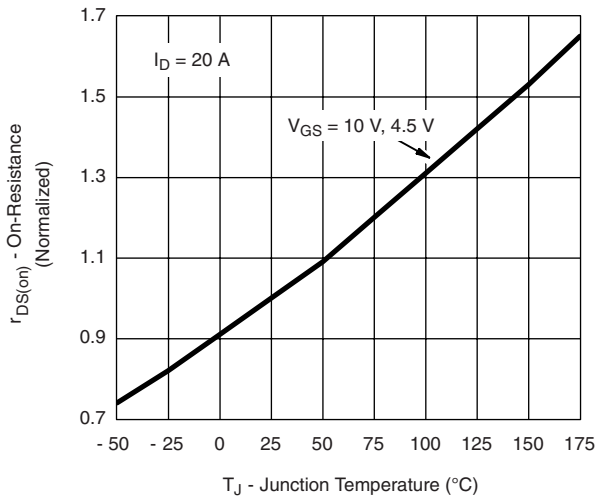
**Gate Charge**

# SUD40N02-3m3P

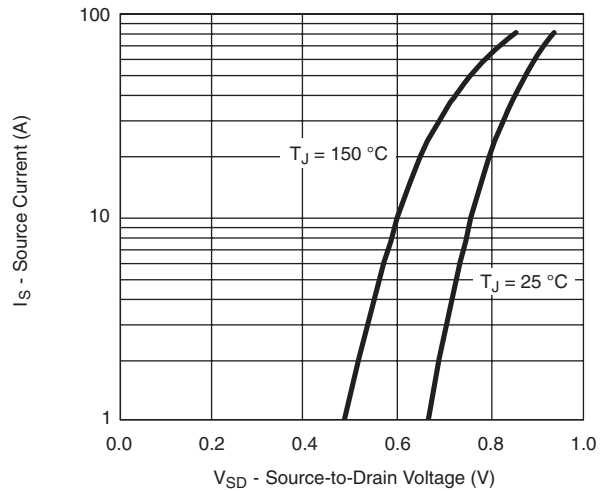


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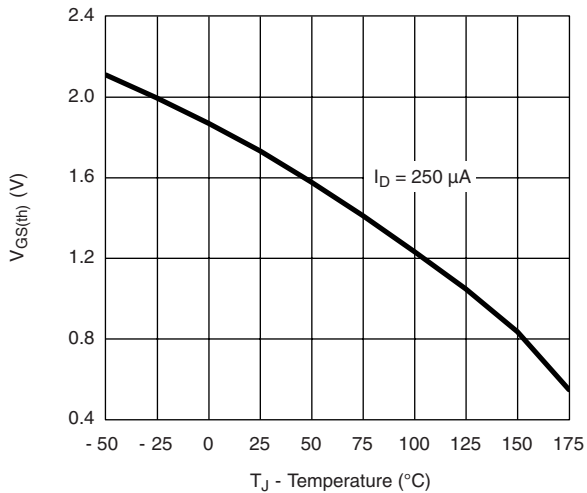
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



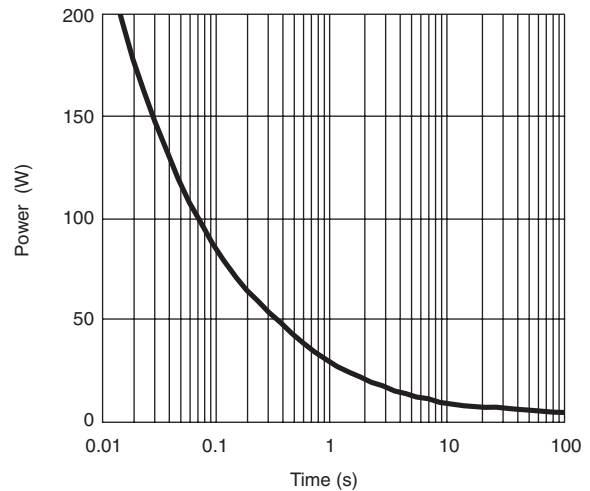
**On-Resistance vs. Junction Temperature**



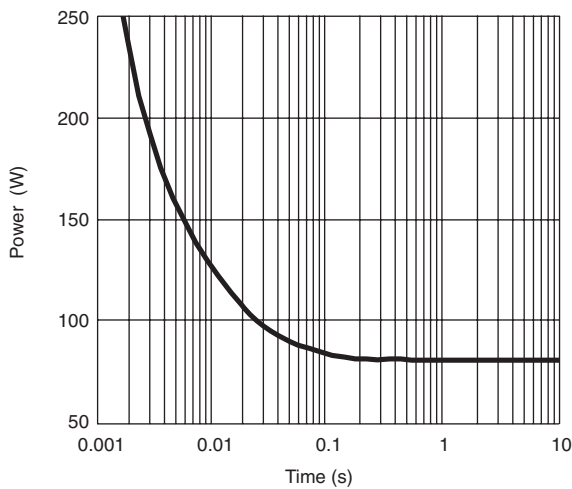
**Forward Diode Voltage vs. Temperature**



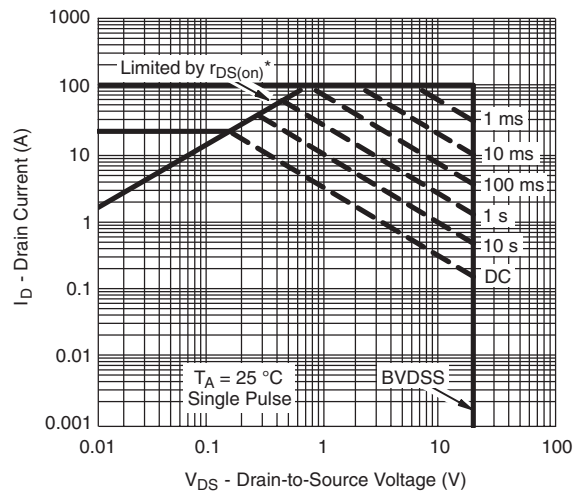
**Threshold Voltage**



**Single Pulse Power, Junction-to-Ambient**



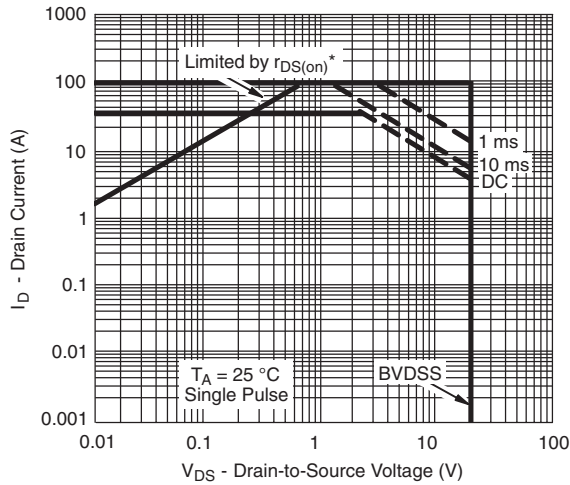
**Single Pulse Power, Junction-to-Case**



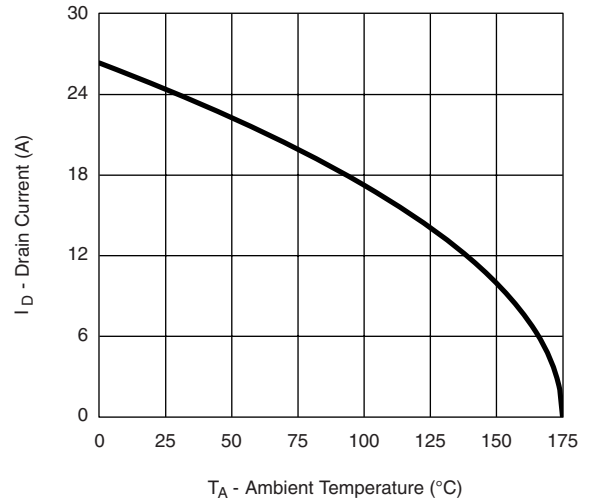
**Safe Operating Area, Junction-to-Ambient**



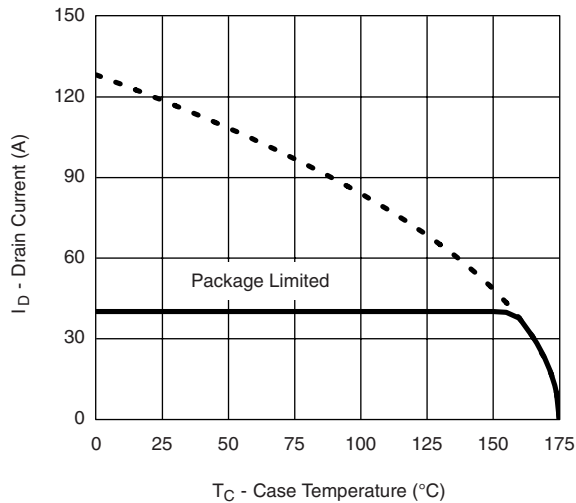
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



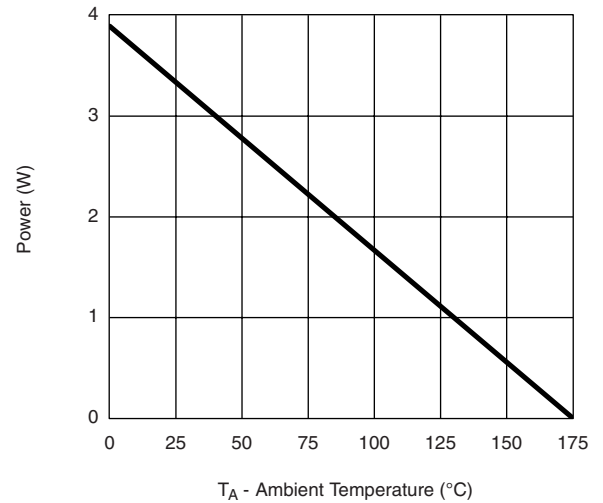
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $r_{DS(on)}$  is specified  
**Safe Operating Area, Junction-to-Case**



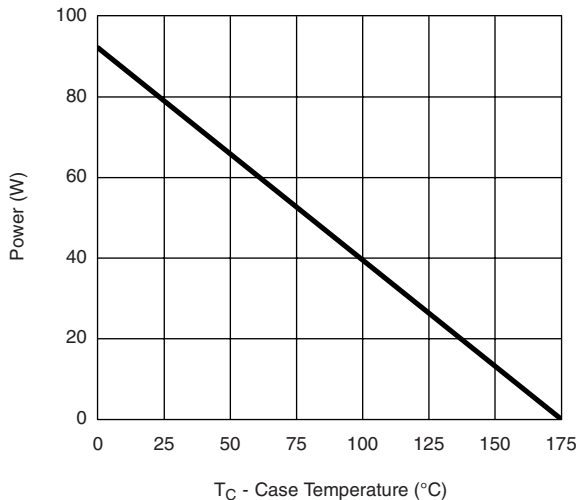
**Current Derating\*\*, Junction-to-Ambient**



**Current Derating\*\*, Junction-to-Case**



**Power Derating\*\*, Junction-to-Ambient**



**Power Derating\*\*, Junction-to-Case**

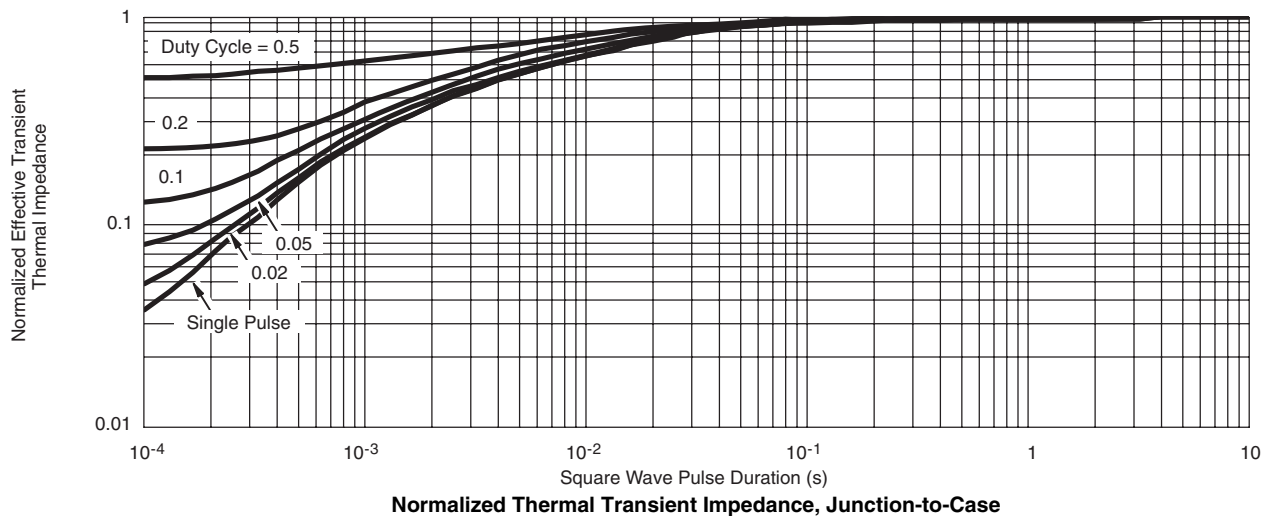
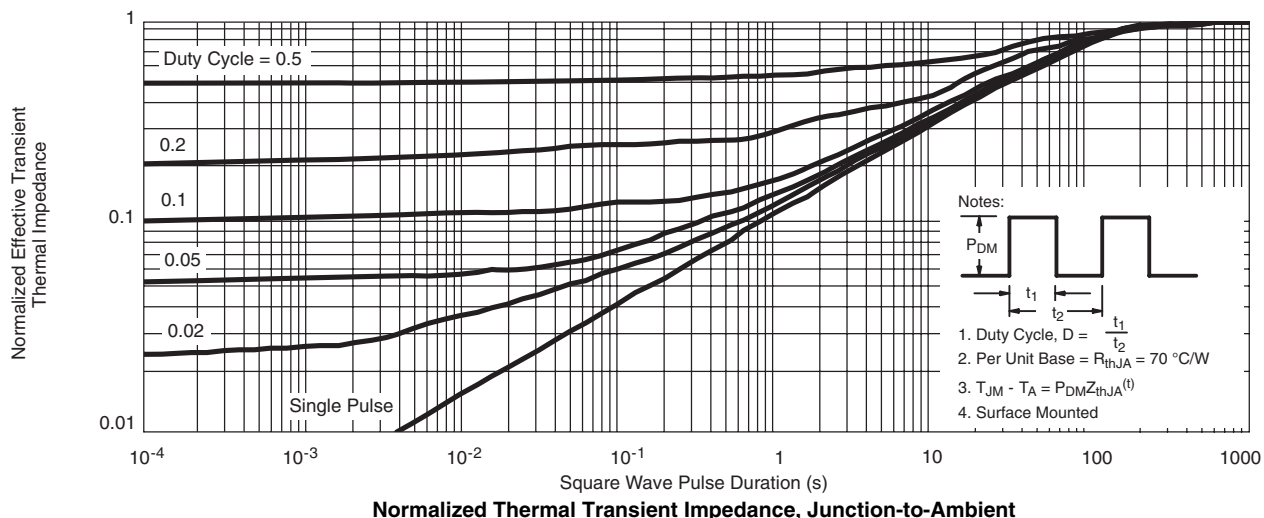
\*\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 175$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

# SUD40N02-3m3P

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## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?69819>.



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