STM1068

Smart voltage supervisor

Features

- Operating voltage 2.7 V to 5.5 V
- Supply current of 1.5 µA (typ)
- Factory-trimmed voltage threshold from 3.2 V to 3.5 V in 50 mV increments
- 3% voltage threshold accuracy across temperature
- Enable and inhibit inputs (EN, INH)
- Power supply transient immunity
- Current limited output of 15 mA (max)
- Available in flip chip 8-bump package
- Operating temperature –30°C to +85°C

Flip chip
(8-bump)

Applications

- Portable devices
- Cell phones/smart phones
- PDA
- Palmtops
- Organizers
- Portable audio/video players
- Portable terminals

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1 Description

STM1068 device monitors supply voltage V_{CC} and the state of EN and INH inputs. Depending on logical combination of these inputs, the output OUT is connected to V_{IN} or GND and the pass gate between PKX and POX is either enabled or disabled (see *Table 2* and *Table 3* for more details).

The device offers several voltage thresholds, V_{TH+} (see *Table 9*) and it is available in miniature flip chip 8-bump package.

Figure 1. Logic diagram

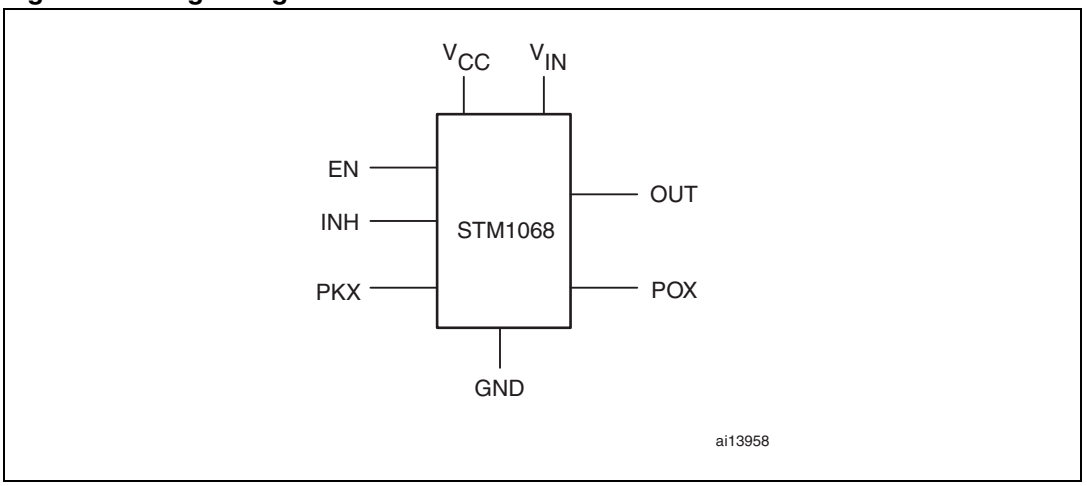


Table 1. Pin descriptions

Pin	Symbol	Function
1A	V_{IN}	Supply for output pin (OUT)
1B	EN	Enable from USB VBUS
1C	GND	Ground
1D	PKX	Pass gate input
2A	OUT	Output
2B	INH	Inhibit input
2C	V_{CC}	Supply voltage
2D	POX	Pass gate output

Figure 2. 8-bump flip chip connections

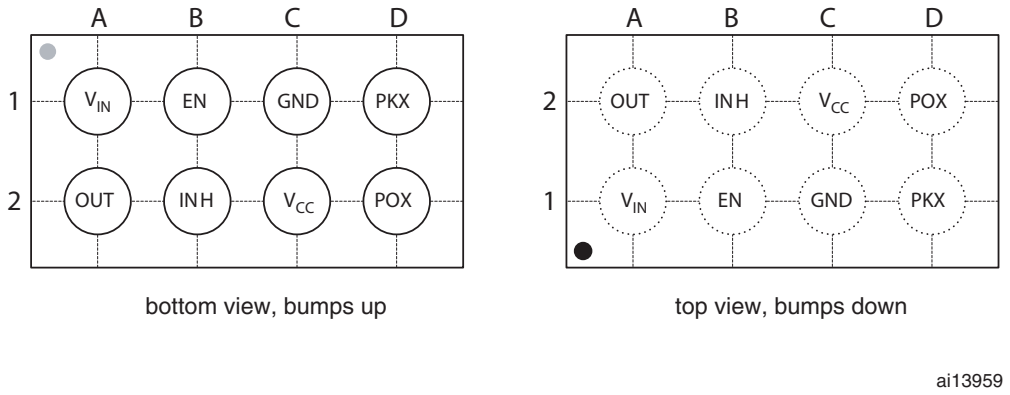


Figure 3. Block diagram

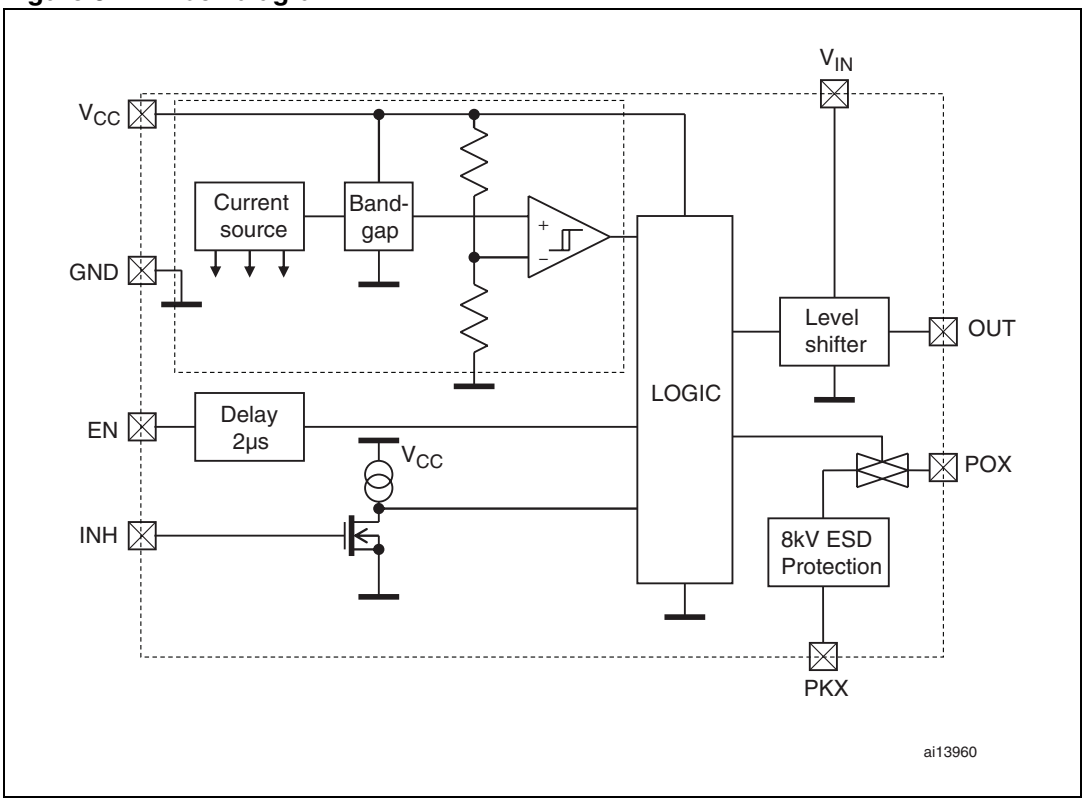
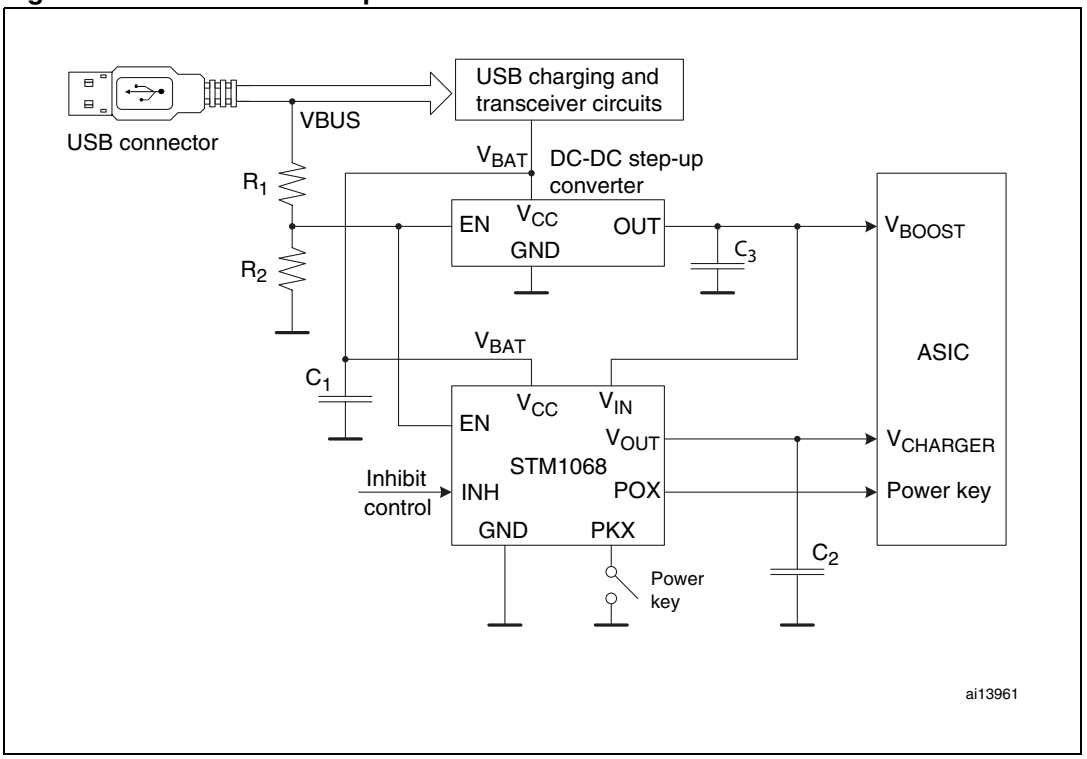


Figure 4. Hardware hookup



2 Operation

The STM1068 device monitors supply voltage V_{CC} and logic states of EN and INH inputs. According to detected states is the output OUT connected to V_{IN} or GND and the pass gate between PKX and POX is either enabled or disabled (see *Table 2*, *Table 3* , and *Figure 11* for more details).

2.1 Output, OUT

If the enable input is in a logic high state and inhibit input is in a logic low state, the output will be connected to V_{IN} input as V_{CC} rises above the V_{TH+} voltage threshold. Otherwise, the output is connected to ground GND. The output is current limited (see *Table 6*).

2.2 Enable input, EN

A logic low on the enable input disconnects the output, OUT, from V_{IN}, the POX will follow the PKX and the device enters a standby mode with very low current consumption (see *Table 6*).

2.3 Inhibit input, INH

A logic high on the inhibit input disconnects the output, OUT, from V_{IN} and the POX will follow the PKX.

2.4 Pass gate, PKX and POX

Pass gate between PKX and POX is disabled only if enable input is in logic high, inhibit input is in logic low and the supply voltage is below the voltage threshold.

Table 2. Truth table for output, OUT

EN(1)	INH	V_{CC}	OUT
L	x	x	connected to GND
x	H	x	connected to GND
x	x	$<V_{TH+}$ (rising edge) $<V_{TH-}$ (falling edge)	connected to GND
H	L	$>V_{TH+}$ (rising edge) $>V_{TH-}$ (falling edge)	connected to V_{IN}

1. Once the device is disabled by EN input, the V_{CC} must be above V_{TH+} to reconnect output to V_{IN}.

Table 3. Truth table for pass gate between PKX and POX

EN	INH	V_{CC}	POX
L	x	x	follows PKX
x	H	x	follows PKX
x	x	$>V_{TH+}$ (rising edge) $>V_{TH-}$ (falling edge)	follows PKX
H	L	$<V_{TH+}$ (rising edge) $<V_{TH-}$ (falling edge)	open

Note: Table valid for $V_{CC} > 2.7$ V.

3 Typical operating characteristics

Figure 5. Supply current vs. supply voltage, V_{EN} = 4 V

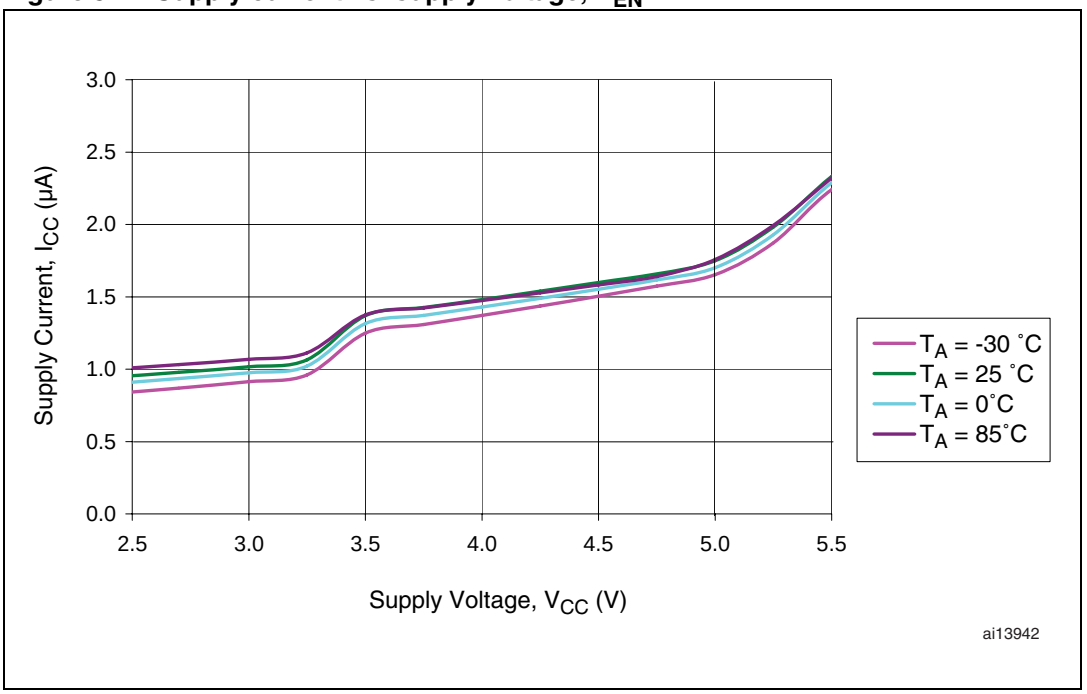


Figure 6. Supply current vs. temperature, V_{EN} = 4 V

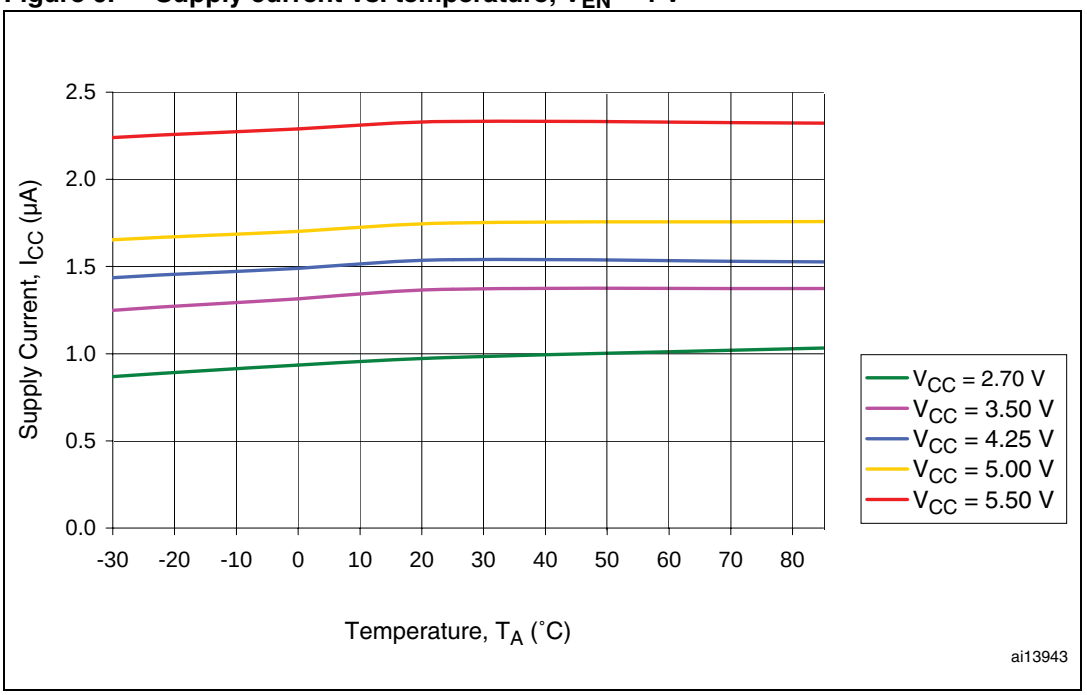


Figure 7. Supply current vs. supply voltage, V_{EN} = 0 V

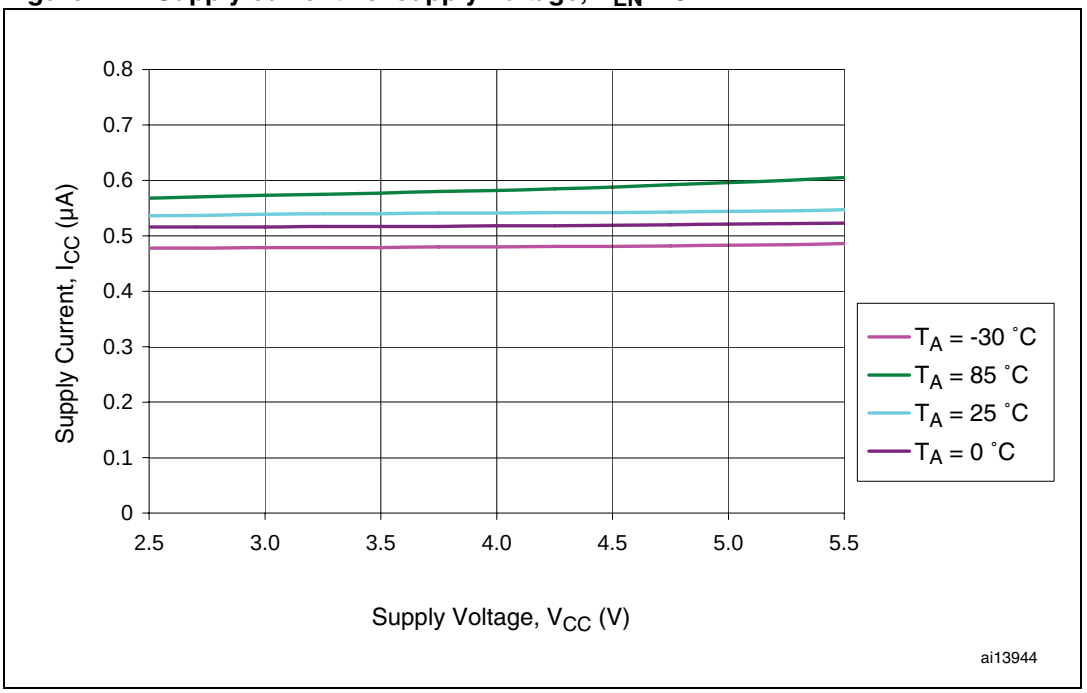


Figure 8. Supply current vs. temperature, V_{EN} = 0 V

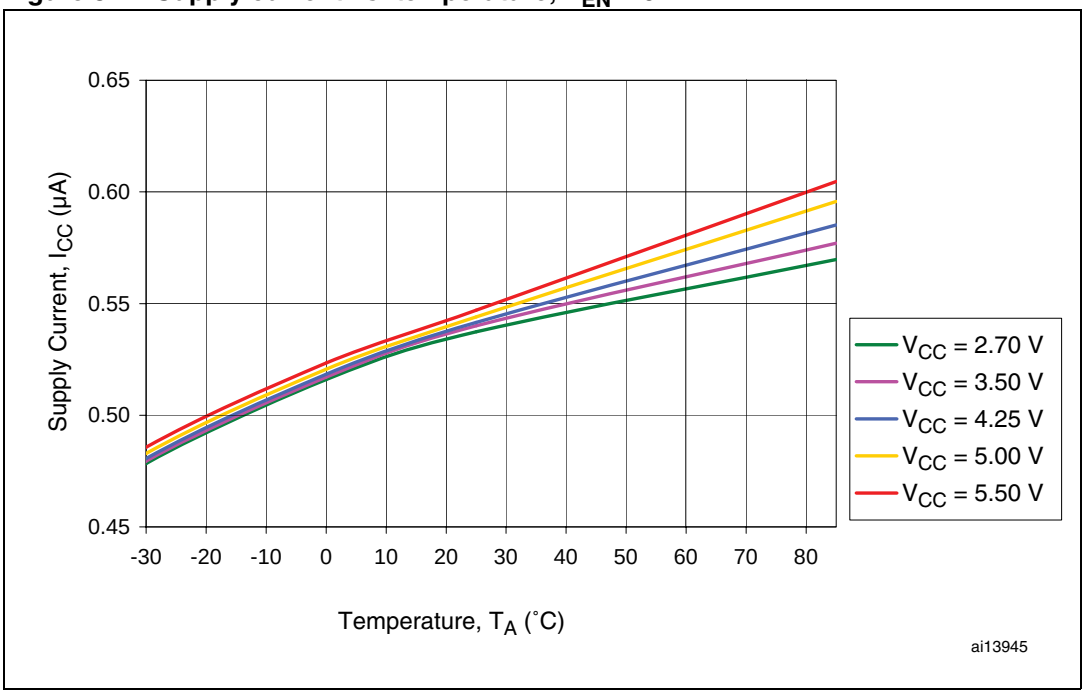


Figure 9. Rising voltage detector threshold vs. temperature

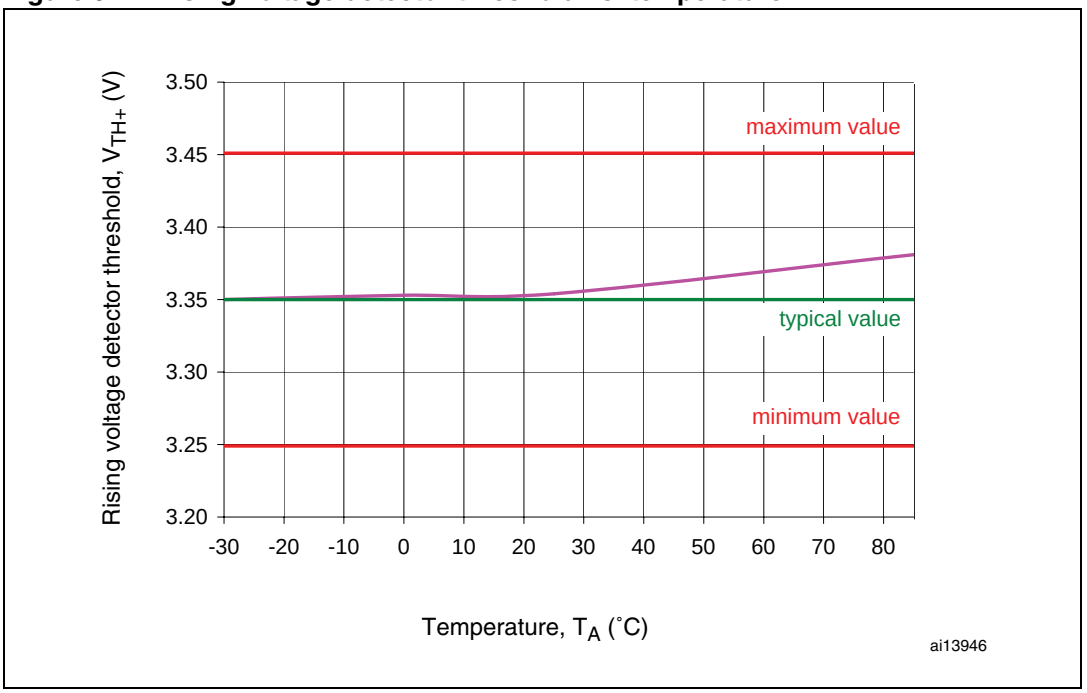
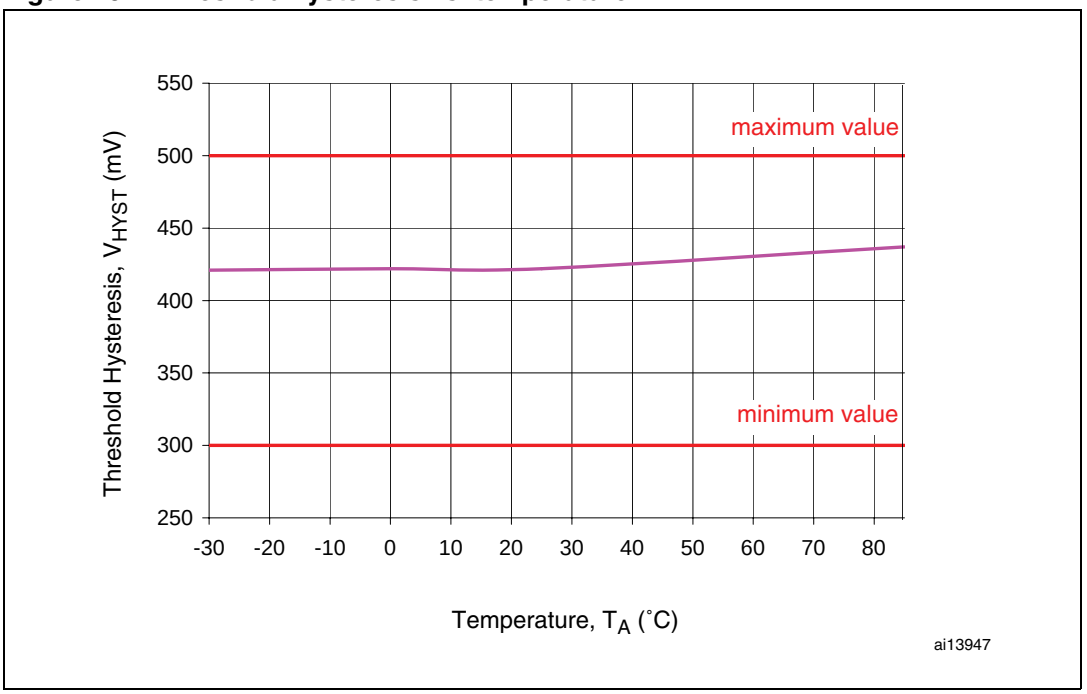


Figure 10. Threshold hysteresis vs. temperature



4 Maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit	Remarks
V_{CC}	Supply voltage	–0.2		+7.0	V	
V_{IN}	Output source voltage	–0.2		+7.0	V	Independent of V_{CC}
V_{EN}	VBUS input	–0.2		V_{CC} + 0.3	V	Series 1M external resistor for protection
V_{OUT}	Output pin	–0.3		V_{IN} + 0.3	V	
V_{INH}	Inhibit pin	–0.3		V_{CC} + 0.3	V	
V_{ESD}	Electrostatic protection	–2		+2	kV	Human body model (all pins)
		–8		+8	kV	Human body model (PKX only)
V_{ESD}	Electrostatic protection	–500		+500	V	Charged device model
V_{ESD}	Electrostatic protection	–100		+100	V	Machine model
V_{ESD}	Point discharge on PKX key	–8		+8	kV	IEC61000-4-2
V_{ESD}	Air discharge on PKX key	–15		+15	kV	IEC61000-4-2
T_A	Operating ambient temperature	–30		+85	°C	
	Storage temperature	–45		+150	°C	

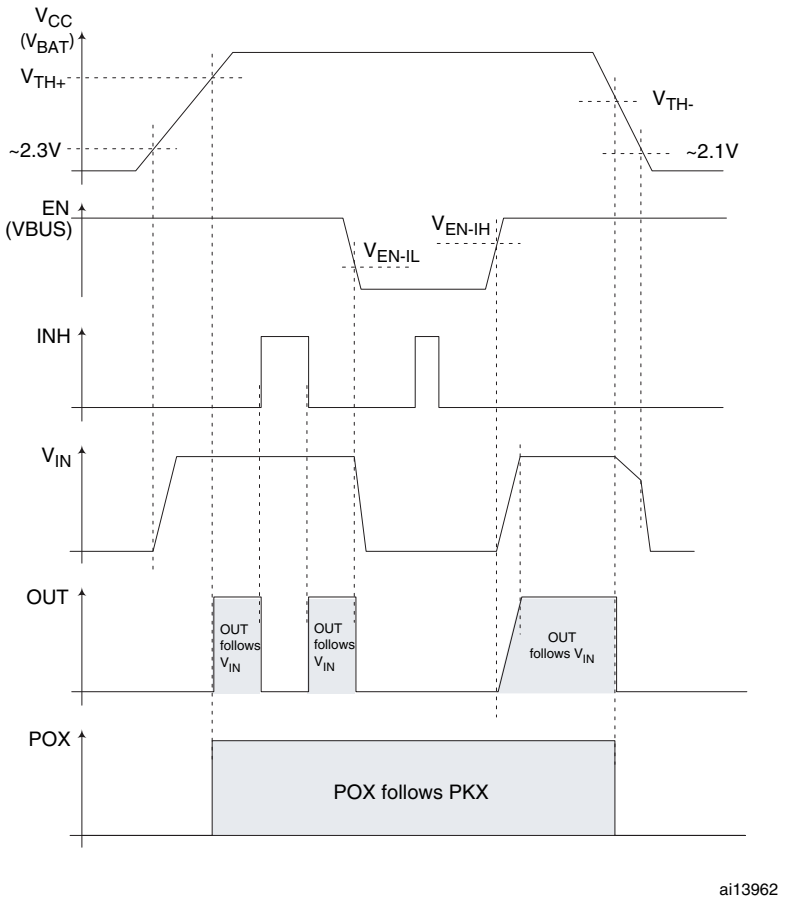
5 DC and AC characteristics

This section summarizes the operating measurement conditions and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow are derived from tests performed under the measurement conditions summarized in *Table 5: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 5. Operating and AC measurement conditions

Parameter	Condition	Unit
V_{CC} supply voltage	2.7 to 5.5	V
Ambient operating temperature (T_A)	–30 to 85	°C
Input rise and fall times	≤ 5	ns

Figure 11. Waveforms



Note: V_{IN} assumed to be from 1.65 V to 5.5 V. No V_{IN} means no signal on OUT pin. If there is no V_{CC} then there will be no V_{IN}.

Table 6. DC and AC characteristics

Sym	Parameter	Test condition(1)	Min	Typ	Max	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Supply current into V_{CC} pin	V_{EN} = 0 V		0.6	1	µA
		V_{EN} = 4 V		1.5	15	µA
I_{CC} +I_{IN}	Current into V_{CC} + V_{IN} pins	V_{EN} = 0 V			5	µA
		V_{EN} = 4 V			15	µA
V_{TH+}	Rising voltage detector threshold (see *Table 8 on page 19* for detailed listing)		–3%	V_{TH+}	+3%	V
V_{HYST}	Threshold hysteresis		0.3		0.5	V
V_{TH-}	Falling voltage detector threshold			V_{TH+} - V_{HYST}		V
$t_{PD-FALL}$(2)	V_{CC} falling to OUT delay	V_{CC} falling from (V_{TH-} + 100 mV) to (V_{TH-} - 100 mV) at 10 mV/µs		30		µs
$t_{PD-RISE}$(2)	V_{CC} rising to OUT delay	V_{CC} rising from (V_{TH+} - 100 mV) to (V_{TH+} + 100 mV) at 10 mV/µs		70		µs
V_{IN}	Voltage on V_{IN} pin Supply for output pin	Allows 2.5 V rail, V_{BAT} or +5 V	2.4		5.5	V
Output pin, OUT(3)						
V_{OUT-OH}	Output high voltage	I_{SOURCE} = 5 mA	V_{IN} - 0.2		V_{IN}	V
V_{OUT-OL}	Output low voltage	I_{SINK} = 10 mA			0.3	V
I_{OUT}	Output current		5		15	mA
Enable input, EN						
V_{EN-IH}	When VBUS is valid		1.2			V
V_{EN-IL}	When VBUS is not valid				0.4	V
I_{EN-IN}	Enable input current				0.1	µA
	EN glitch immunity		1			µs
Inhibit input, INH						
V_{INH-IH}	Inhibit logic high		1.2			V
V_{INH-IL}	Inhibit logic low				0.4	V
V_{INH-IN}	Inhibit input current				0.1	µA
	INH glitch immunity		1			µs

Table 6. DC and AC characteristics (continued)

Sym	Parameter	Test condition(1)	Min	Typ	Max	Unit
Pass gate between PKX and POX						
$R_{DS(on)}$	Static pass gate on resistance			300		Ω

1. Valid for ambient operating temperature: T_A = –30°C to +85°C; V_{CC} = 2.7 V to 5.5 V (except where noted).
2. Guaranteed by design.
3. For V_{CC} below V_{TH-}, the output remains low down to V_{CC} = 1 V. Below V_{CC} = 1 V the voltage V_{IN} must be less than V_{OUT-OL} (max.) to guarantee output low voltage less than 0.3 V.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 12. Flip chip 8-bump, package mechanical outline

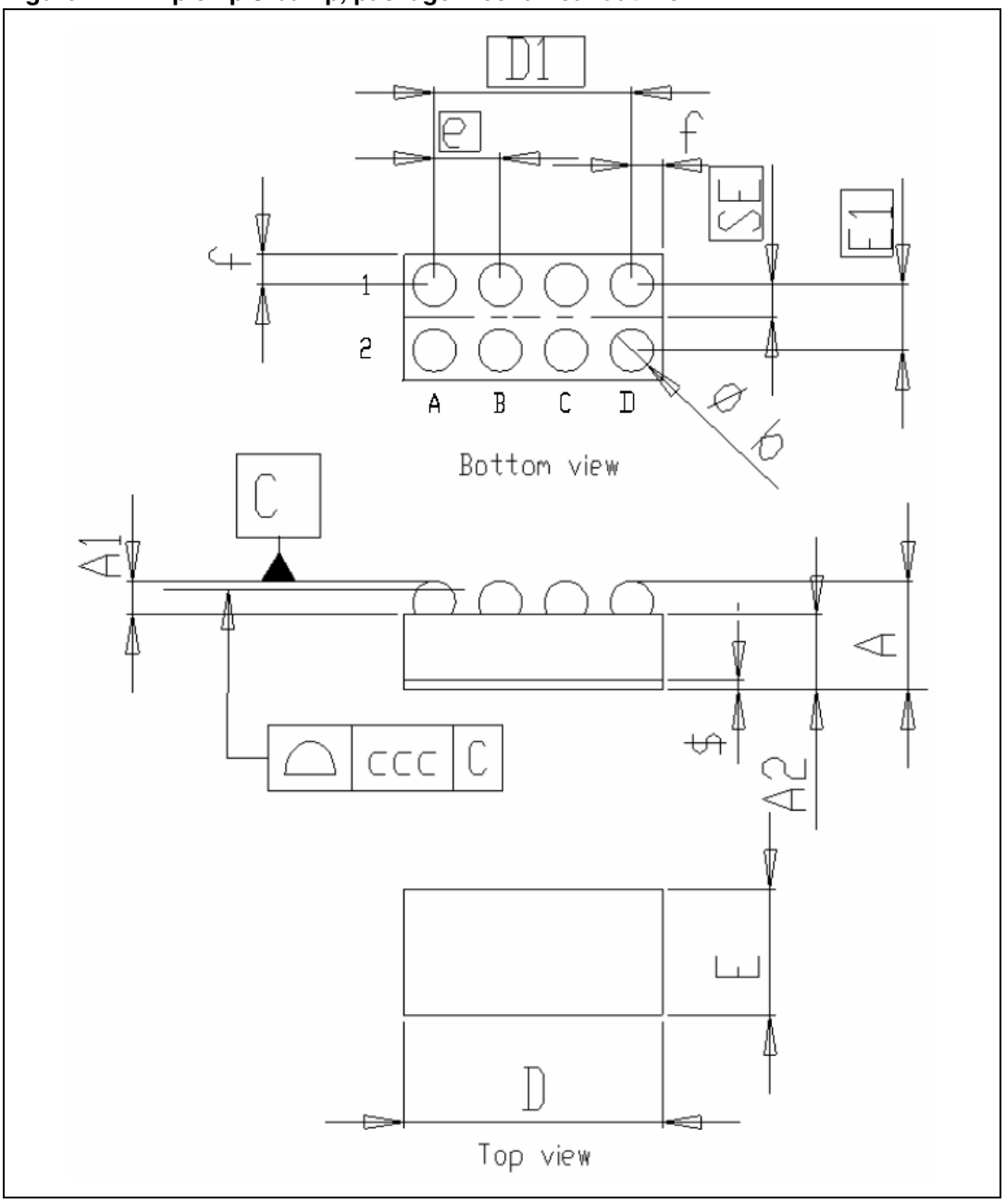
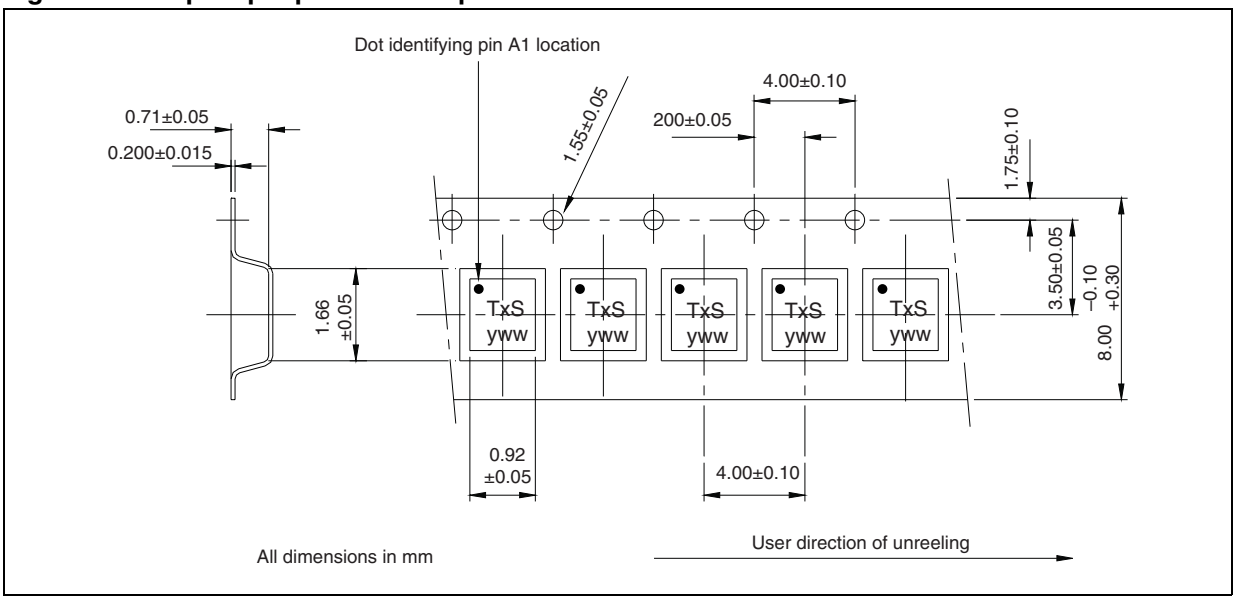


Table 7. Flip chip 8-bump, package mechanical data

Symbol	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.54	0.60	0.66	0.021	0.024	0.026
A1	0.170	0.205	0.240	0.007	0.008	0.009
A2		0.395			0.015	
b	0.215	0.255	0.295	0.008	0.010	0.012
D	1.570	1.600	1.605	0.062	0.063	0.063
D1		1.20			0.047	
e	0.36	0.40	0.44	0.014	0.016	0.017
E	0.77	0.80	0.83	0.030	0.031	0.033
E1	0.36	0.40	0.44	0.014	0.016	0.017
SE	0.18	0.20	0.22	0.007	0.008	0.009
f		0.20			0.008	
ccc		0.05			0.002	
$	0.035	0.045	0.050	0.001	0.002	0.002

Figure 13. Flip chip tape and reel specifications



7 Part numbering

Table 8. Ordering information scheme

Example: STM1068 C35 F3 8 F

Device type

STM1068

Threshold voltage (3.2V to 3.5V in 0.05V increments)

C20: 3.20V(1)

C25: 3.25V(1)

C30: 3.30V(1)

C35: 3.35V

C40: 3.40V(1)

C45: 3.45V(1)

C50: 3.50V(1)

Package

F3: Flip chip, lead-free, pitch = 400µm, bump = 250µm, 8-bump

Temperature range

8: –30°C to 85°C

Shipping method

F = ECOPACK® package, tape & reel

1. Contact local ST sales office for availability.

8 Package marking information

Table 9. Factory-trimmed thresholds with marking description

Part number	Rising voltage detector threshold V_{TH+} at ambient temperature T_A from –30 to +85°C			Topside marking(1)
	Min (–3%)	Typ	Max (+3%)	
STM1068C20F38F	3.104	3.20	3.296	THS yww
STM1068C25F38F	3.152	3.25	3.348	TIS yww
STM1068C30F38F	3.201	3.30	3.399	TJS yww
STM1068C35F38F	3.249	3.35	3.451	TKS yww
STM1068C40F38F	3.298	3.40	3.502	TLS yww
STM1068C45F38F	3.346	3.45	3.554	TMS yww
STM1068C50F38F	3.395	3.50	3.605	TNS yww

1. Where “y” = assembly year (0 to 9) and “ww” = assembly work week (01 to 52).

9 Revision history

Table 10. Document revision history

Date	Revision	Changes
31-Aug-2007	1	Initial release.
07-Sep-2007	2	Updated cover page, *Section 1: Description*, *Figure 3*, and *Table 6*.
03-Jan-2008	3	Updated *Figure 1*, *11*, *13*, and *Table 3*, *5*, *6*, *9*; added *Section 3: Typical operating characteristics*; minor presentation changes.
26-Mar-2008	4	Updated *Table 6*, *7*.
09-Apr-2008	5	Document status upgraded to full datasheet; updated *Figure 12*.
27-May-2008	6	Minor document reformatting.

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