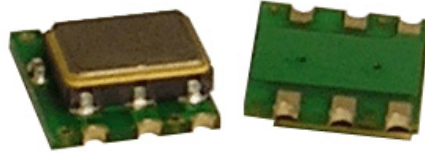


## LV76D / LV78D Series 2.5 V LVDS Clock Oscillators

January 2008



### Do Not Use for New Designs - use LV55 or LV77

- Pletronics' LV76D / LV78D Series is a quartz crystal controlled precision square wave generator with an LVDS output.
- FR4 base with a mechanical metal cover.
- Solder pad compatible with many 9x14mm plastic J lead packages.
- Tape and Reel or cut tape packaging is available.
- 80 to 250 MHz
- 9.04mm x 8.23mm (S package)
- Enable/Disable LV76D on pad 1  
LV78D on pad 2
- Disable function includes low standby power mode
- 3<sup>rd</sup> Overtone Crystals used
- Low Jitter
- 5x7 mm LV77xxDW is used

**Pletronics Inc. certifies this device is in accordance with the RoHS 5/6 (2002/95/EC) and WEEE (2002/96/EC) directives.**

Pletronics Inc. guarantees the device does not contain the following:

Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's

Weight of the Device: 0.4 grams

Moisture Sensitivity Level: 1 As defined in J-STD-020C

Second Level Interconnect code: e4

### Absolute Maximum Ratings:

Parameter	Unit
V <sub>CC</sub> Supply Voltage	-0.5V to +5.0V
V <sub>i</sub> Input Voltage	-0.5V to V <sub>CC</sub> + 0.5V
V <sub>o</sub> Output Voltage	-0.5V to V <sub>CC</sub> + 0.5V

### Thermal Characteristics

The maximum die or junction temperature is 155°C

The thermal resistance junction to board is 60 to 100°C/Watt depending on the solder pads, ground plane and construction of the PCB.



# LV76D / LV78D Series 2.5 V LVDS Clock Oscillators

January 2008

## Part Number:

LV7x 45 D E W -125.0M -XX

## Part Marking:

PLE LV77  
FF.FFF M  
• YMDXX

	<b>Packaging code or blank</b> T250 = 250 per Tape and Reel T500 = 500 per Tape and Reel T1K = 1000 per Tape and Reel
	<b>Frequency in MHz</b>
	<b>Supply Voltage V<sub>CC</sub></b> W = 2.5V ± 10%
	<b>Optional Enhanced OTR</b> Blank = Temp. range -10 to +70°C E = Temp. range -40 to +85°C
	<b>Series Model</b>
	<b>Frequency Stability</b> 45 = ± 50 ppm 44 = ± 25 ppm 20 = ± 20 ppm
	<b>Series Model</b> LV76 or LV78

### Marking Legend:

PLE = Pletronics

FF.FFF M = Frequency in MHz

YMD = Date of Manufacture (year and week, or year-month-day)

All other marking is internal factory codes

The marking is on the cover of the LV77 device

The marking is that of the LV77 device

Specifications such as frequency stability, supply voltage and operating temperature range, etc. are not identified from the marking. External packaging labels and packing list will correctly identify the ordered Pletronics part number.

### Codes for Date Code YMD

Code	6	7	8	9	0	1	2
Year	2006	2007	2008	2009	2010	2011	2012

Code	A	B	C	D	E	F	G	H	J	K	L	M
Month	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC

Code	1	2	3	4	5	6	7	8	9	A	B	C
Day	1	2	3	4	5	6	7	8	9	10	11	12
Code	D	E	F	G	H	J	K	L	M	N	P	R
Day	13	14	15	16	17	18	19	20	21	22	23	24
Code	T	U	V	W	X	Y	Z					
Day	25	26	27	28	29	30	31					



# LV76D / LV78D Series 2.5 V LVDS Clock Oscillators

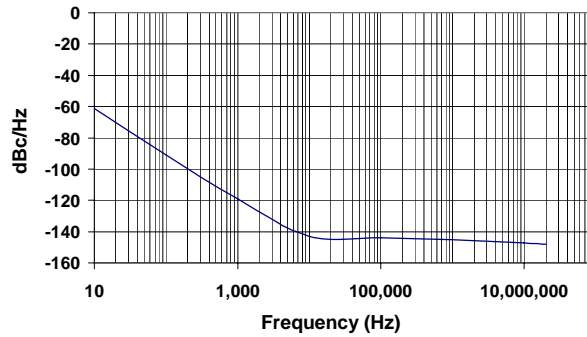
January 2008

## Electrical Specification for 2.50V $\pm 10\%$ over the specified temperature range

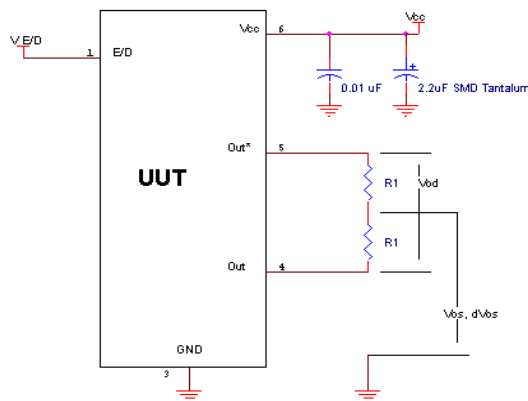
Item	Min	Max	Unit	Condition
Frequency Range	80	250	MHz	
Frequency Accuracy "45"	-50	+50	ppm	For all supply voltages, load changes, aging for 1 year, shock, vibration and temperatures
"44"	-25	+25		
"20"	-20	+20		
Output Waveform	LVDS			
Output High Level	--	1.60	Volts	See load circuit R1 = 50 ohms
Output Low Level	0.90	--	Volts	See load circuit R1 = 50 ohms
Differential Output ( $V_{OD}$ )	247	454	mVolts	See load circuit R1 = 50 ohms
Output Offset Voltage ( $V_{OS}$ )	1.125	1.375	Volts	See load circuit R1 = 50 ohms
Differential Output Error ( $dV_{OS}$ )	--	50	mVolts	See load circuit R1 = 50 ohms
Output Symmetry	45	55	%	Referenced to 50% of amplitude or crossing point
Output $T_{RISE}$ and $T_{FALL}$	300	700	pS	$V_{th}$ is 20% and 80% of waveform
Jitter	-	0.15	pS RMS	Measured from 12KHz to 20MHz from $F_{nominal}$
	-	2.8		Measured from 10Hz to 1MHz from $F_{nominal}$
Vcc Supply Current	-	63	mA	Includes current of properly terminated device
Enable/Disable Internal Pull-up	50	-	Kohm	To Vcc (equivalent resistance)
V disable	-	0.8	Volts	Referenced to Ground
V enable	2.0	-	Volts	Referenced to Ground
Output leakage $V_{OUT} = V_{CC}$	-10	+10	uA	Pad 1 low, device disabled
	$V_{OUT} = 0V$	-10		
Enable	-	10	nS	Time for output to reach a logic state
Disable time	-	10	nS	Time for output to reach a high Z state
Start up time	-	5	mS	Measured from the time $V_{CC} = 3.0V$
Operating Temperature Range	-10	+70	°C	Standard Temperature Range
	-40	+85	°C	Extended Temperature Range "E" Option
Storage Temperature Range	-55	+125	°C	
Standby Current $I_{CC}$	-	3	uA	Pad 1 low, device disabled

Specifications with E/D open circuit

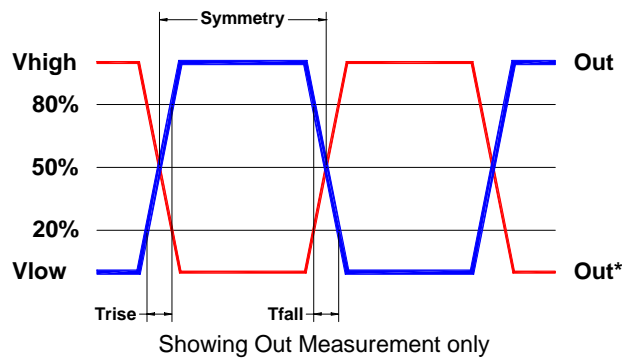
## Typical Phase-Noise Response



## Load Circuit



## Test Waveform



## Reliability: Environmental Compliance

Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002, Condition B
Vibration	MIL-STD-883 Method 2007, Condition A
Solderability	MIL-STD-883 Method 2003
Thermal Shock	MIL-STD-883 Method 1011, Condition A

## ESD Rating

Model	Minimum Voltage	Conditions
Human Body Model	1500	MIL-STD-883 Method 3115
Charged Device Model	1000	JESD 22-C101

## Package Labeling

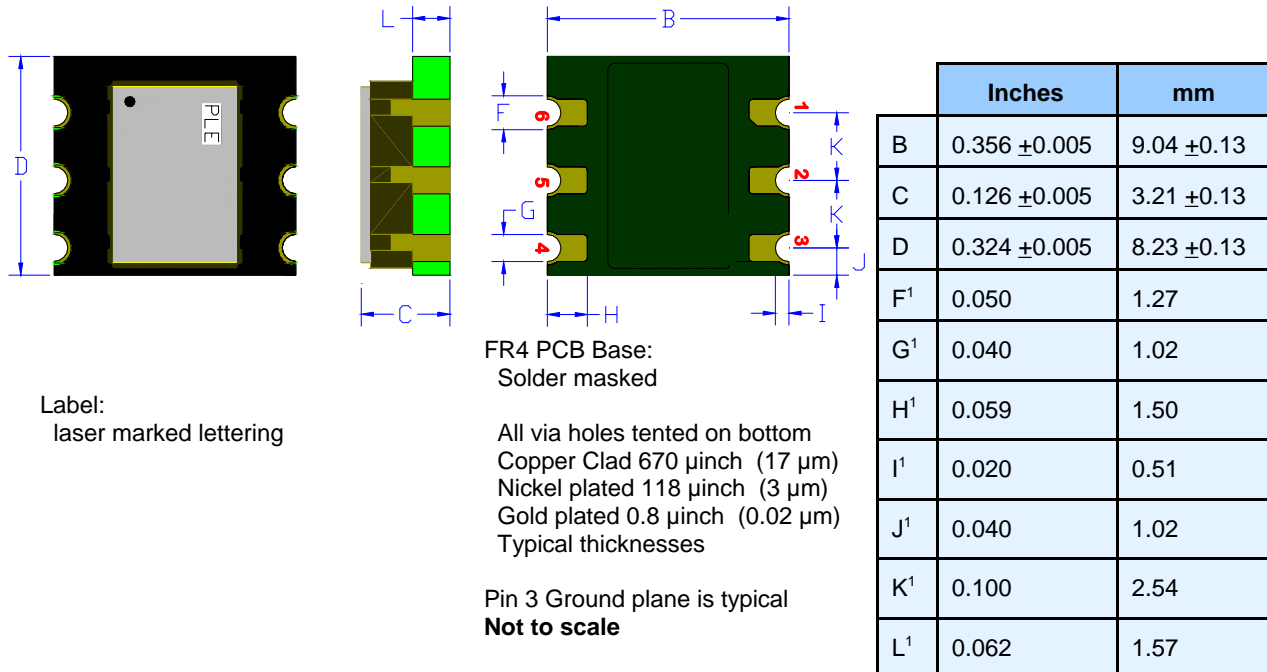
Label is 1" x 2.6" (25.4mm x 66.7mm)  
 Font is Courier New  
 Bar code is 39-Full ASCII  
 (the label will show LV76 or LV78)

Label is 1" x 2.6" (25.4mm x 66.7mm)  
 Font is Arial

P/N:		
	LV7845DW-156.25M	
Customer P/N:		
	12345678	
Qty:		D/C 
	1000	75409

RoHS Compliant
2nd Lvl Interconnect
Category=e4
Max Safe Temp=245C for 10s 2X Max

## Mechanical:



Pad		Function	Note
76	78		
1	2	No connect	There is no internal connection to this pad
2	1	Output Enable/Disable	When this pad is not connected the oscillator shall operate. When this pad is <0.30 volts, the output will be inhibited (high impedance state.) Recommend connecting this pad to $V_{CC}$ if the oscillator is to be always on.
3		Ground (GND)	
4		Output	The outputs must be terminated, 100 ohms between the outputs is the ideal termination.
5		Output*	
6		Supply Voltage ( $V_{CC}$ )	Recommend connecting appropriate power supply bypass capacitors as close as possible.

## Layout and application information

Recommend connecting Pad 1 and Pad 2 together to permit the design to accept Enable/Disable on both input pads (see LV76D for E/D on pad 1)

For Optimum Jitter Performance, Pletronics recommends:

- a ground plane under the device
- no large transient signals (both current and voltage) should be routed under the device
- do not layout near a large magnetic field such as a high frequency switching power supply

## Mechanical (obsolete version):

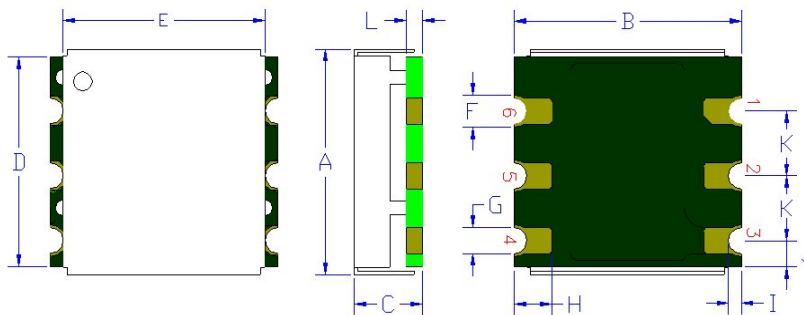
The cover is no longer being supplied over this part. This part is made with a hermetically sealed LV77xxDW series oscillator. This part is now exposed.

The cover has been deleted, the cover was causing problems with the newer high temperature RoHS lead free processes. The cover purpose was only cosmetic.

All parts with 2008 date codes will be made in the new fashion.

There is no change in electrical properties.

Pletronics does recommend that all designs should transition to the LV77xxDW ceramic part.



	Inches	mm
A	0.351 ±0.003	8.91 ±0.07
B	0.356 ±0.005	9.04 ±0.13
C	0.103 ±0.005	2.62 ±0.13
D <sup>1</sup>	0.324	8.23
E <sup>1</sup>	0.316	8.03
F <sup>1</sup>	0.050	1.27
G <sup>1</sup>	0.040	1.02
H <sup>1</sup>	0.059	1.50
I <sup>1</sup>	0.020	0.51
J <sup>1</sup>	0.040	1.02
K <sup>1</sup>	0.100	2.54
L <sup>1</sup>	0.026 typical	0.66

### Cover:

Centered on the base  
304 Stainless Steel  
0.010 inch (0.25mm)  
Electroless Nickel Plated  
1 μinch (25 μm) typical

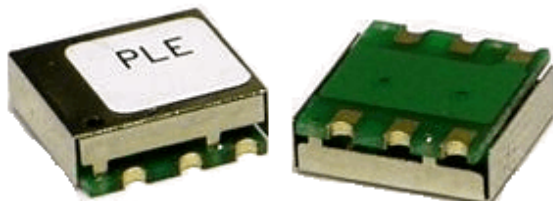
### Label:

White Kapton with Black Letters  
—or—  
Blue Epoxy heat cure ink covering  
top with laser marked lettering

### FR4 PCB Base:

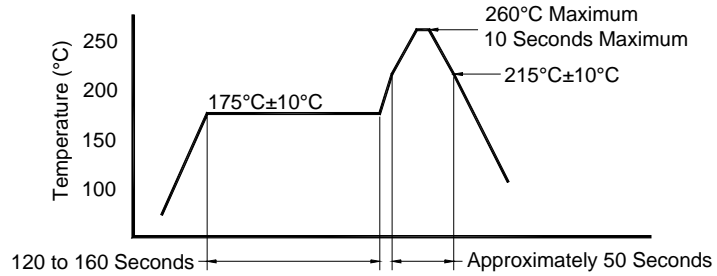
Solder masked  
Solder masked  
All via holes tented on bottom  
Copper Clad 670 μinch (17 μm)  
Nickel plated 118 μinch (3 μm)  
Gold plated 0.8 μinch (0.02 μm)  
Typical thicknesses

Pin 3 Ground plane is typical  
**Not to scale**



- The package is not hermetically sealed.
- The sides are intentionally left open to permit cleaning material to freely flow in the package, thus minimizing the accumulation of contaminants during cleaning processes.
- The internal part of the package must be thoroughly dry before operating.

## Reflow Cycle (typical for lead free processing)



The part may be reflowed 2 times without degradation.

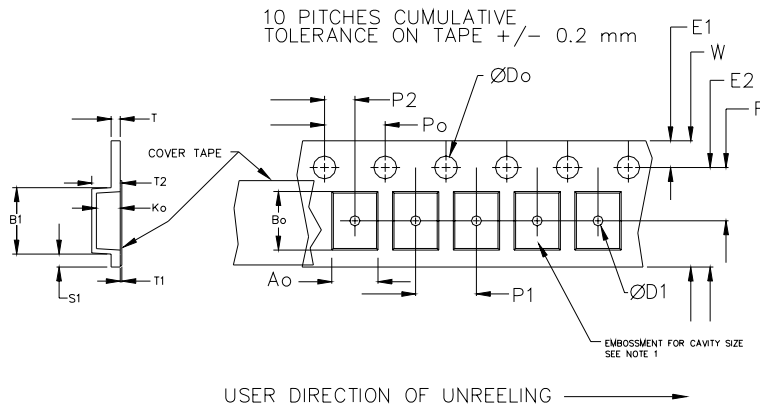
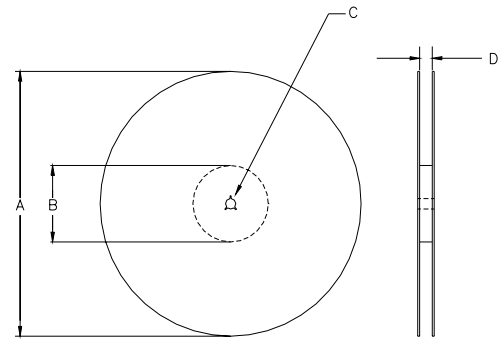
Allowed rate of temperature change  
Maximum 4°C per second

## Tape and Reel: available for quantities of 250 to 1000 per reel, cut tape for < 250

Constant Dimensions Table 1									
Tape Size	D0	D1 Min	E1	P0	P2	S1 Min	T Max	T1 Max	
8mm	1.5	1.0	1.75	4.0	2.0 ±0.05	0.6	0.6	0.1	
12mm		1.5			2.0 ±0.1				
16mm		+0.1 -0.0			±0.1				±0.1
24mm		1.5			±0.1				

Variable Dimensions Table 2							
Tape Size	B1 Max	E2 Min	F	P1	T2 Max	W Max	Ao, Bo & Ko
24 mm	9.88	22.25	11.5 ±0.1	16.0 ±0.1	3.22	24.3	Note 1

Note 1: Embossed cavity to conform to EIA-481-B      Dimensions in mm      Not to scale



REEL DIMENSIONS					
A	inches	7.0	10.0	13.0	Tape Width
	mm	177.8	254.0	330.2	
B	inches	2.50	4.00	3.75	Tape Width
	mm	63.5	101.6	95.3	
C	mm	13.0 +0.5 / -0.2			Tape Width
D	mm	---	---	24.4 +2.0 -0.0	

Reel dimensions may vary from the above





# LV76D / LV78D Series 2.5 V LVDS Clock Oscillators

January 2008

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