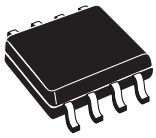
STS9NH3LL

N-channel 30 V - 0.018 Ω - 9 A - SO-8 low gate charge STripFET™ III Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STS9NH3LL	30 V	0.022 Ω	9 A

- Optimal $R_{DS(on)}$ x Qg trade-off @ 4.5 V
- Conduction losses reduced
- Switching losses reduced



SO-8

Application

- Switching applications

Description

This application specific Power MOSFET is the third generation of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

Figure 1. Internal schematic diagram

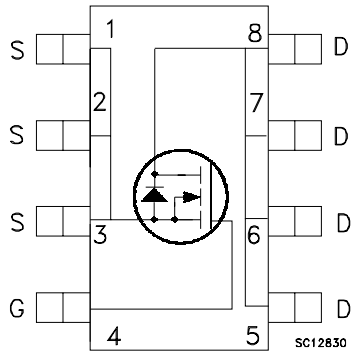


Table 1. Device summary

Order code	Marking	Package	Packaging
STS9NH3LL	S9NH3LL	SO-8	Tape & reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}	Gate-source voltage	±16	V
I_D	Drain current (continuous) at T_C = 25 °C	9	A
I_D	Drain current (continuous) at T_C= 100 °C	6	A
I_{DM} (1)	Drain current (pulsed)	36	A
P_{TOT}	Total dissipation at T_C = 25 °C	2.5	W
E_{AS} (2)	Single pulse avalanche energy	100	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area
2. Starting T_J = 25 °C, I_D = 6 A.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$ (1)	Thermal resistance junction-ambient max	50	°C/W

1. When mounted on 1 inch² FR-4 board, 2oz Cu (t < 10 sec.)

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating @ 125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±16 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 4.5 A V_{GS}= 4.5 V, I_D= 4.5 A		0.018 0.020	0.022 0.025	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =10 V, I_D = 4.5 A		8.5		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f=1 MHz, V_{GS}=0		857 147 20		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}= 15 V, I_D = 9 A V_{GS} = 4.5 V, *(see Figure 16)*		7.0 2.5 2.3	10	nC nC nC

1. Pulsed: pulse duration=300 µs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}=15 V, I_D= 4.5 A, R_G= 4.7 Ω, V_{GS}= 4.5 V *(see Figure 15)*		12 14.5		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD}=15 V, I_D= 4.5 A, R_G= 4.7 Ω, V_{GS}= 4.5 V *(see Figure 15)*		23 8		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)				9 36	A A
V_{SD}(2)	Forward on voltage	I_{SD}= 4.5 A, V_{GS}=0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 9 A, di/dt = 100 A/µs, V_{DD} = 15 V, Tj=150 °C *(see Figure 17)*		15 5.7 0.76		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

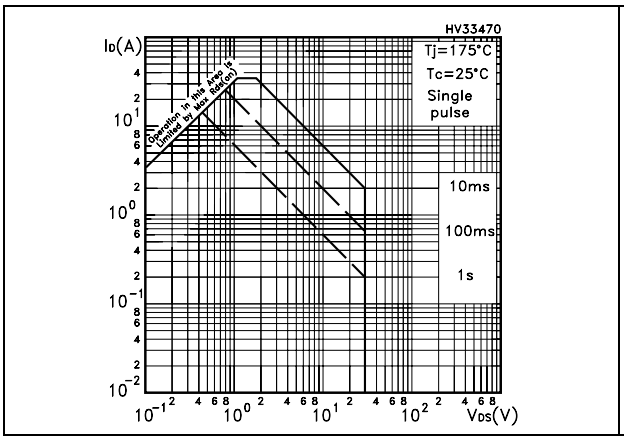


Figure 3. Thermal impedance

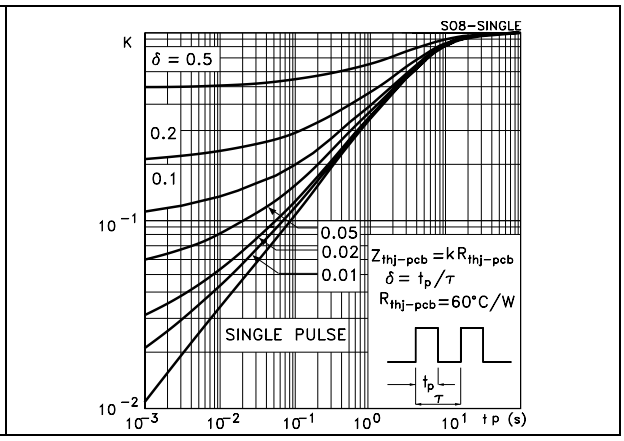


Figure 4. Output characteristics

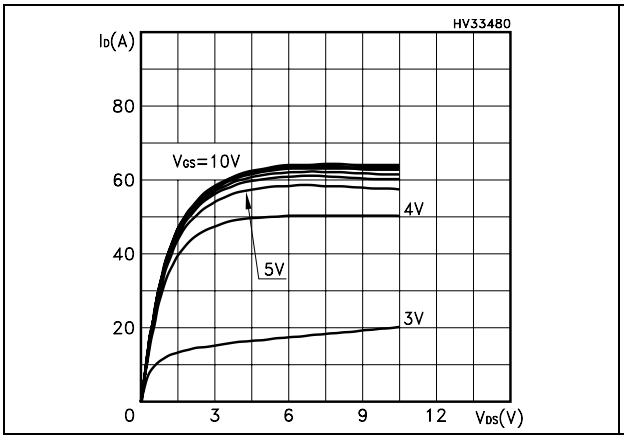


Figure 5. Transfer characteristics

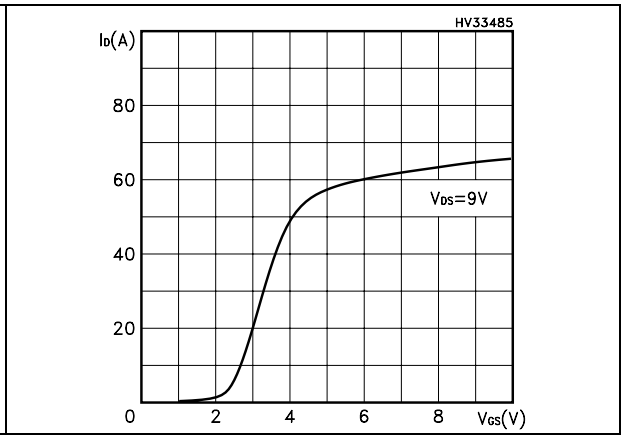


Figure 6. Transconductance

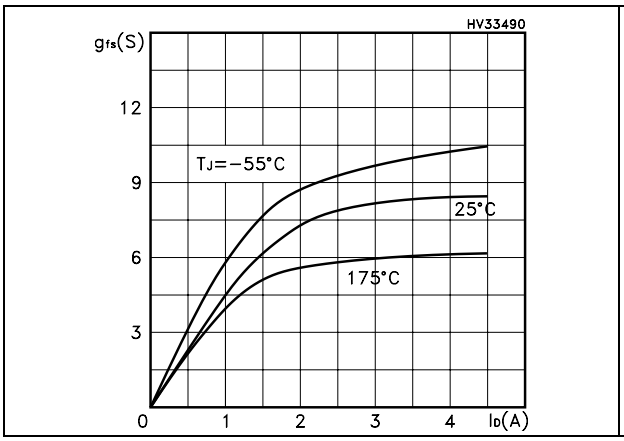


Figure 7. Static drain-source on resistance

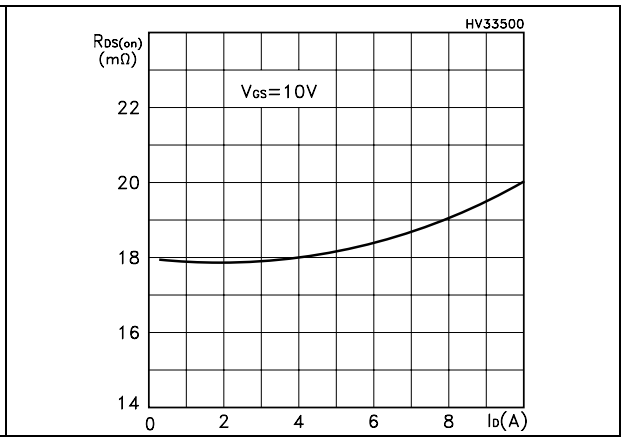


Figure 8. Gate charge vs gate-source voltage

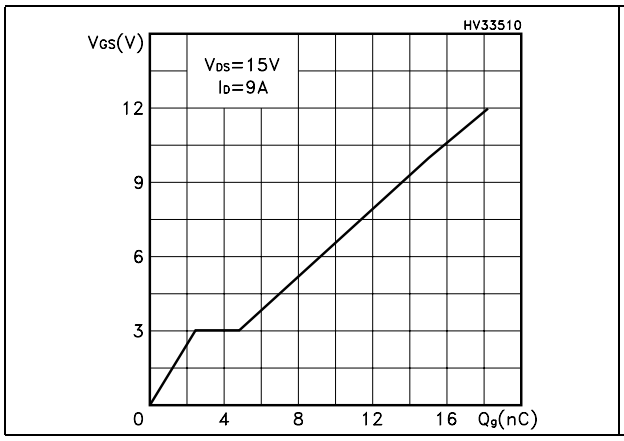


Figure 9. Capacitance variations

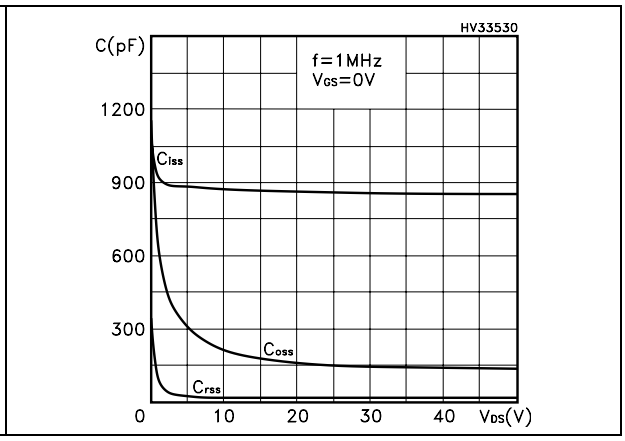


Figure 10. Normalized gate threshold voltage vs temperature

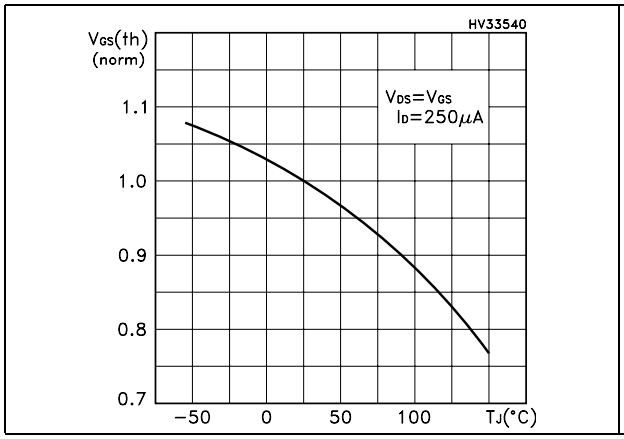


Figure 11. Normalized on resistance vs temperature

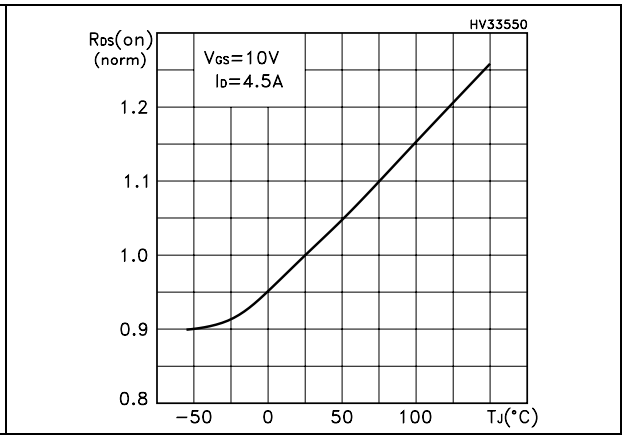


Figure 12. Source-drain diode forward characteristics

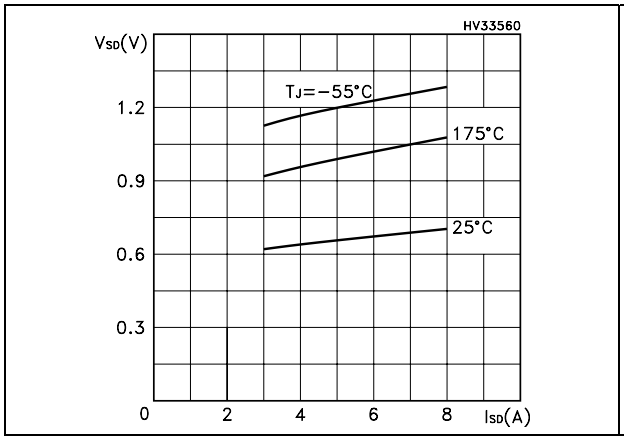


Figure 13. Normalized breakdown voltage vs temperature

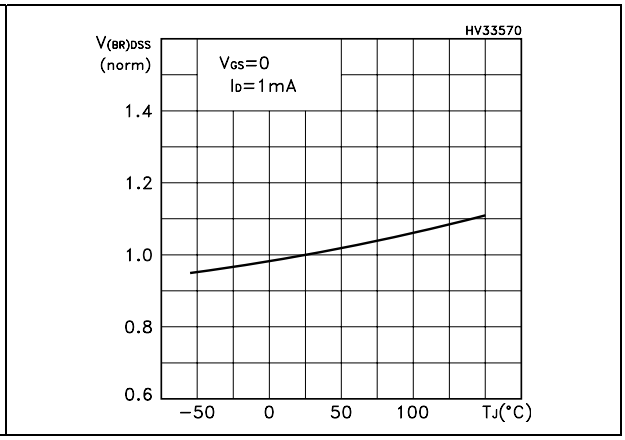
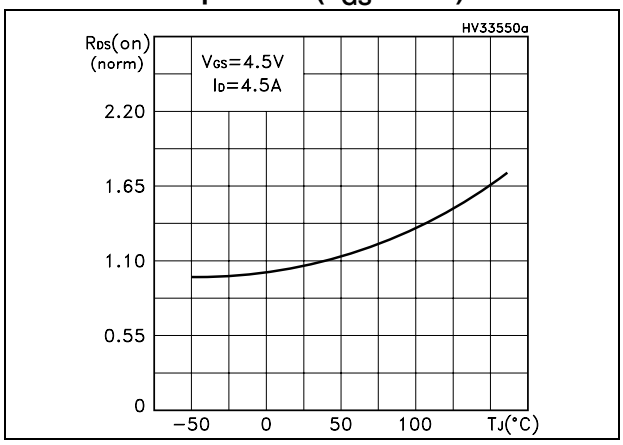


Figure 14. Normalized on resistance vs temperature (V_{GS} = 4.5V)



3 Test circuit

Figure 15. Switching times test circuit for resistive load

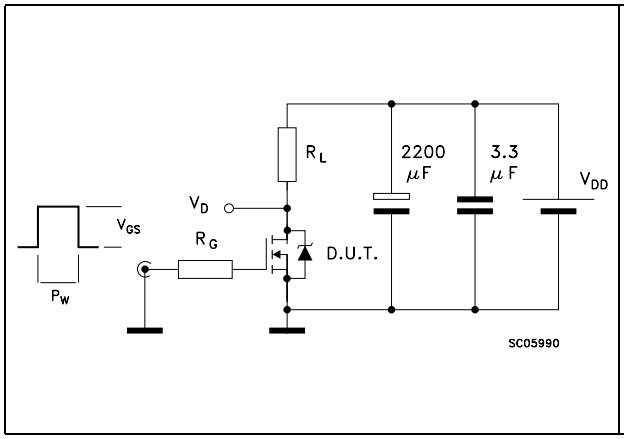


Figure 16. Gate charge test circuit

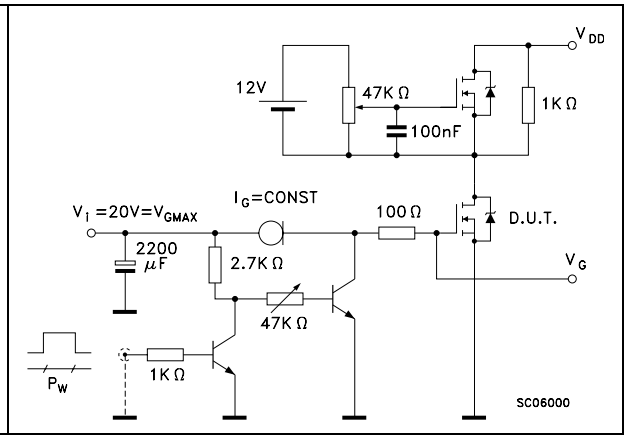


Figure 17. Test circuit for inductive load switching and diode recovery times

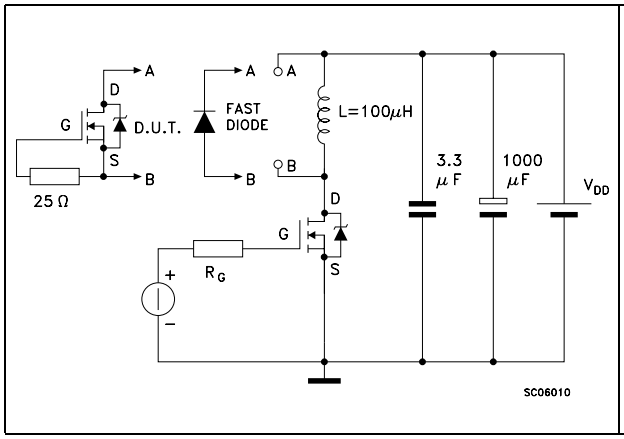


Figure 18. Unclamped inductive load test circuit

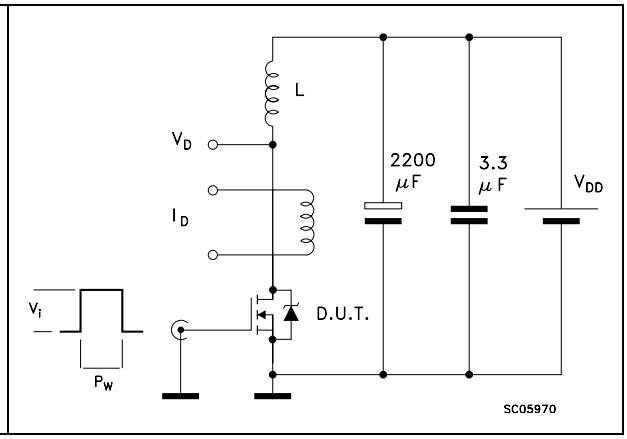


Figure 19. Unclamped inductive waveform

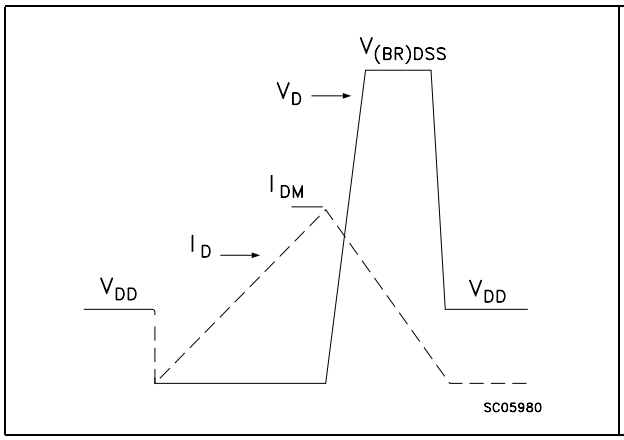
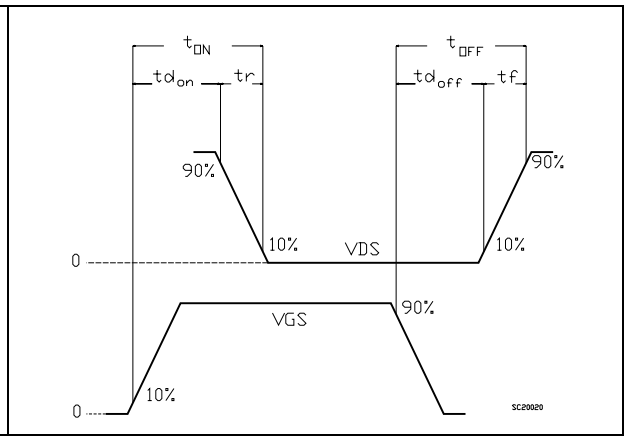


Figure 20. Switching time waveform

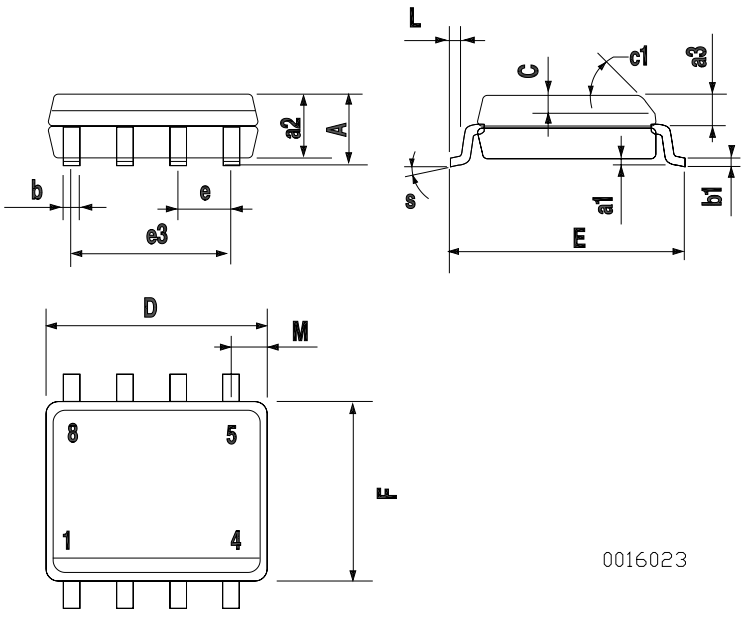


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
24-Jul-2006	1	Initial release.
15-May-2007	2	Update on *Table 2.*
12-Dec-2007	3	– Inserted *Figure 14: Normalized on resistance vs temperature (V_{GS} = 4.5V)* – Inserted new E_{AS} value on *Table 2.*

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