NE57810

Advanced DDR memory termination power with external reference voltage in

Rev. 04 — 24 November 2008 Product data sheet

1. Introduction

The NE57810 is designed to provide power for termination of a Double Data Rate (DDR) SDRAM memory bus. It significantly reduces parts count, board space, and overall system cost compared to previous solutions.

2. General description

The NE57810 DDR termination regulator maintains an output voltage (DDR reference bus voltage) that is half the RAM supply voltage. It is capable of providing up to ± 3.5 A for sustained periods. Overcurrent limiting protects the NE57810 from inrush currents at start-up. Overtemperature shutdown protects the device in extreme temperature situations.

The package is thermally robust for flexibility of thermal design. The NE57810 is a linear regulator so no external inductors or switching FETs are necessary. Fast response to load changes reduces the need for output capacitors.

3. Features

- Fast transient response time
- Overtemperature protection
- Overcurrent protection
- Commercial (0 °C to +70 °C) temperature range
- Reduced need for external components (switching FETs, inductors, decoupling capacitors)
- Internal divider maintains termination voltage at half the memory supply voltage
- Reference out for other memory and control components
- Optional external voltage reference in for flexible application
- Compatible with DDR-I (V_{DD} = 2.5 V) or DDR-II (V_{DD} = 1.8 V) SDRAM systems

4. Applications

- Desktop microcomputer systems
- Workstations
- Servers
- Game machines
- Set top boxes
- Embedded systems

NXP founded by Philips

- Digital video recorders

5. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
NE57810S	-	plastic single-ended surface-mounted package; 5 leads	SOT756

6. Functional diagram

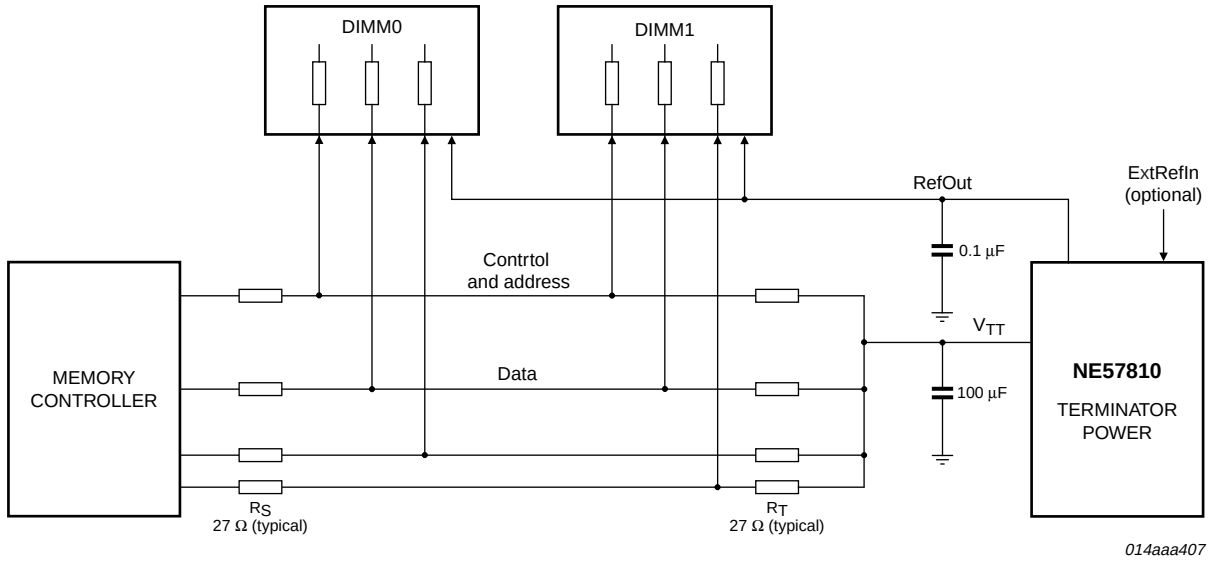


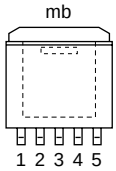
Fig 1. Simplified system diagram

7. Pinning information

7.1 Pinning

Table 2. Pinning

Symbol	Pin	Description	Simplified outline
V_{TT}	1	Regulated terminator voltage	
V_{DD}	2	Power supply	
V_{SS}	3	Circuit ground[1]	
ExtRefIn	4	External reference voltage in	
RefOut	5	Reference voltage out	



[1] The thermal pad on the rear of the device (shown by dotted outline) is connected electrically to V_{SS} internally and provides enhancement to thermal conductivity. It should not be used as the primary connection to ground as device specifications indicate the use of the V_{SS} pin for this purpose.

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8. Application design-in information

The NE57810 can be used in a variety of DDR memory configurations. Its small footprint, fast transient response and reduced need for large bulk output capacitance, makes it highly adaptable. Some of examples methods of use are described in the following sections.

8.1 Normal operating mode ($V_{TT} = V_{DDR}/2$)

The most common implementation of a DDR terminator regulator using the NE57810 is shown in Figure 2. The NE57810 has an internal resistor divider between the V_{DD} (pin 2) and V_{SS} (pin 3) pins which maintains the output voltage, V_{TT}, at $V_{DD}/2$.

Typically, the V_{DD} voltage is the DDR RAM supply voltage, which can range from 1.8 V to 2.5 V. The center node of this resistor divider is connected to ExtRefIn (pin 4). This node acts as the reference for the V_{TT} output voltage and the buffered RefOut signal (pin 5).

If the ExtRefIn pin is not connected to other voltage sources, two small bypass capacitors (0.01 µF) should be placed between the ExtRefIn pin and the V_{SS} and V_{DD} pins to improve the terminator's noise performance. These two capacitors improve enable the terminator to better track any variations in the memory V_{DD} voltage. This method can be seen in Figure 2.

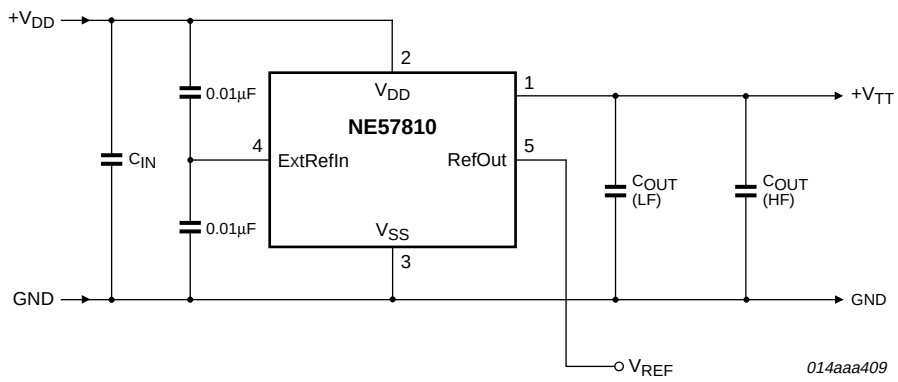

Fig 2. Normal operating method ($V_{TT} = V_{DD}/2$)

There are two components to the memory signal load: a high frequency component caused by the 266 MHz plus speed of the address, data and control buses, and a low frequency component caused by the time-average skew of all of the bus states away from an equal number of 1s and 0s. Electrolytic and tantalum capacitors show inductance at the high frequencies, so two types of capacitors are required for output filtering.

A very good, low ESR bulk electrolytic capacitor of no less than 470 µF should be placed next to the terminator which, in turn, should be placed as close as possible to the memory array. Multiple high frequency ceramic filter capacitors are also needed for high speed transient filtering and output stability. These capacitors may be from V_{TT} to V_{SS} (shown in the diagrams) or one half from V_{TT} to V_{DD} and the other half from V_{TT} to V_{SS} so the output will better track any variations in the V_{DD} voltage.

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For different memory sizes, the values of the recommended output filter capacitances will change. For a 256 MB memory space, for example, approximately 100 µF of ceramic surface mount chip capacitors should be evenly distributed across the physical memory layout. Depending upon the PCB noise environment, this can be 10 pieces of 10 µF, 20 pieces of 5 µF, and so on.

8.2 Externally programmed V_{TT} output voltage

The NE57810 enables use of an external reference voltage to set its V_{TT} output voltage. This pin (ExtRefIn pin 4) is used for applications where the V_{TT} voltage is not V_{DD} divided by 2. This allows V_{TT} voltage and current to be drawn from a power supply bus that is not the DDR RAM supply voltage. This has some advantages when you are attempting to better match the power being drawn from the outputs emerging from the main system power supply. This can be seen in Figure 3.

The internal reference voltage is set by two matched 100 kΩ resistors connected in a resistor divider between the V_{DD} and V_{SS} pins of the NE57810

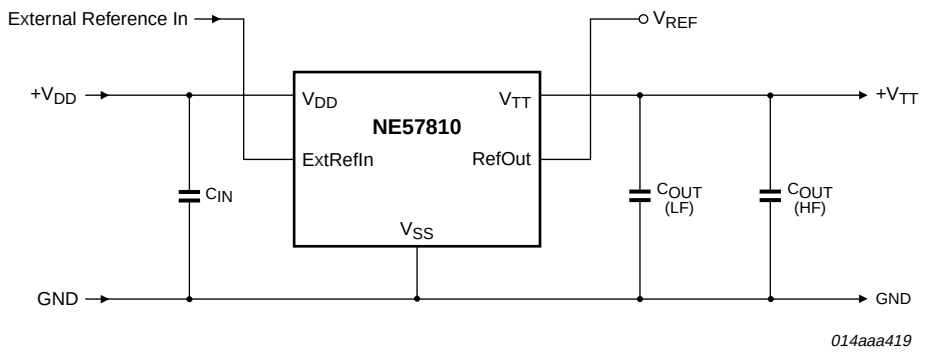

Fig 3. Externally programmed V_{TT}

8.3 Cascading the NE57810

For high-performance computer systems, sometimes memory banks are driven 180 degrees out of phase with one another in such a way that the apparent access time is halved (even and odd memory addresses). To do this, NXP recommends that two NE57810s are used, one to terminate each memory bank.

Cascading NE57810 terminators offers two advantages, it improves the system noise performance by bringing the memory SIMMs closer to the terminator, and it distributes any heat generated by the terminator system. By using the RefOut pin from one NE57810 to the ExtRefIn pin for the other NE57810(s) used in the system, one can always guarantee that the V_{TT} voltages are identical.

Because of the very tight output voltage regulation of the NE57810, the V_{TT} outputs should never be wired together. This is because the terminators would 'fight' one another if their output were different by only a few millivolts. This method can be used in either the normal operating mode and the externally programmed operating mode. This method of use can be seen in Figure 4.

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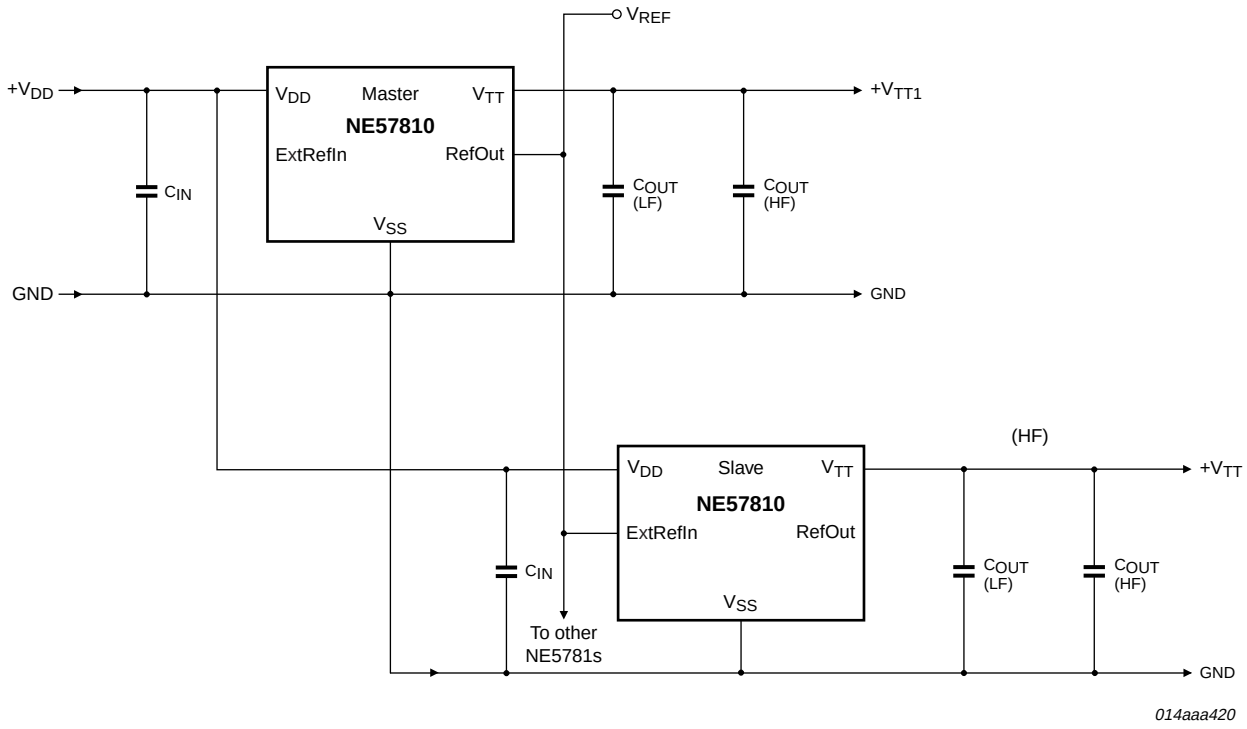

Fig 4. Cascading terminator systems for complex memory systems

9. Technical description

The NE57810 supplies power to the DDR memory bus termination resistors at nominally half the voltage supplied to the memory ICs or DIMMs. DDR memory output drivers source and sink current into and out of their outputs.

A typical DDR memory system is seen in Figure 1. Each input/output pin on the bus has a series 20 Ω resistor connected to it. The bus is terminated to the DDR terminator through a 27 Ω to 50 Ω resistance. The memory system then requires current from the V_{TT} terminator bus only when the instantaneous values of the aggregate bus state are not equal amounts of 1s and 0s.

When memory bus speeds are in the 200 MHz to 300 MHz region, the period of any single bus state is extremely small. This permits the DDR bus termination regulator to be a linear power operational amplifier that can source and sink current instantly to the DDR bus from the V_{DD} supply voltage.

Figure 6 models the V_{TT} loading condition of each bus line equivalent circuit during operation and with terminating resistors.

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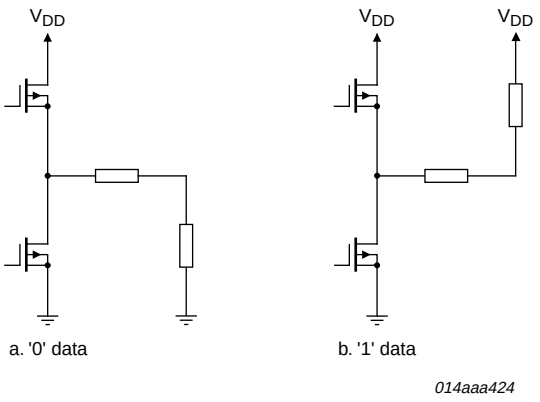

Fig 5. V_{TT} loading conditions

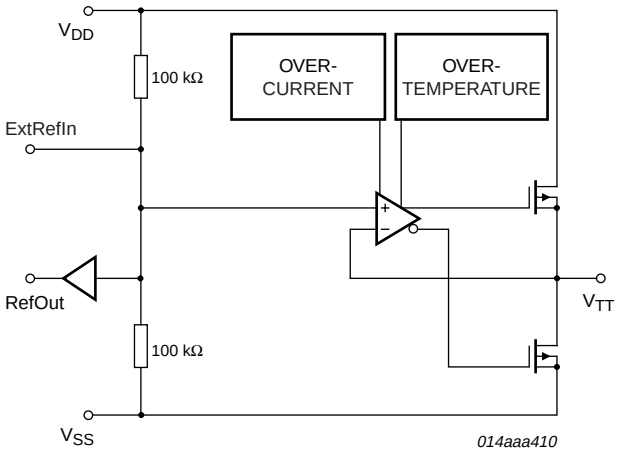

Fig 6. Block diagram

This yields the worst case current loading Equation 1:

$$I_{O(max)} = \frac{N_{DDR} V_{DD}}{2(R_T + R_S)} \quad (1)$$

Where:

- N_{DDR} is the total number of terminated control, address and data lines within the DDR memory system. (typically 192).
- R_T is the value of the terminating resistors.
- R_S is the value of the series resistors from the active output driver.

Hence the worst case current loading condition, where there are either all 1s or all 0s for an instant, and R_T is 27 Ω and R_S is 20 Ω, produces an instantaneous output current of either +3.5 A or –3.5 A.

10. Thermal design

Designing the proper thermal system for the NE57810 is important for its reliable operation. The NE57810 will be operating at an average power level less than the maximum rating of the part. In a typical DDR terminator system the average power dissipation is between 0.8 W and 1.5 W.

The termination power will vary as the average number of 1s and 0s changes during normal operation of the DDR memory. The load current will assume a new value for each bus cycle at a 266 MHz rate, and will increase and decrease as the statistical average of bus states change.

The terminator heat sink must be designed to accommodate the average power as a steady state condition and be able to withstand momentary periods of increased dissipation, typically 2 seconds to 5 seconds duration. For the typical NE57810 application, the power dissipated by the terminator can be calculated by Equation 2:

$$P_D = I_{DD} \times V_{TT} W \quad (2)$$

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The thermal resistance of a surface mount package is given as $R_{th(j-a)}$, the thermal resistance from the junction to air. JESD51-7 specifies a 4-layer multilayer PCB (2 oz/1 oz/1 oz/2 oz copper) that is 4 inches on each side.

This is probably the best (or lowest) thermal resistance you will see in any application. Most applications cannot afford the PCB area to create this situation, but the thermal performance of a multilayer PCB will still provide a significant heatsinking effect. The actual thermal resistance will be higher than the 16.5 °C/W given for the 4-layer JEDEC PCB.

Figure 7 shows the thermal resistance you can expect for heatsinking PCB areas less than the JEDEC specification. The graph is for a 2 oz single-sided PCB with a square area of the side dimension as given on the X-axis. If you use a double-sided PCB with some plated-through holes to help transfer heat to the bottom side, the thermal resistance only improves by about 3 °C/W to 4 °C/W.

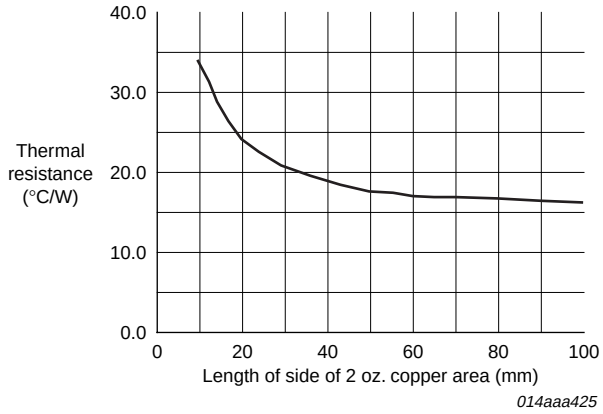

Fig 7. PCB heat sink area versus thermal resistance

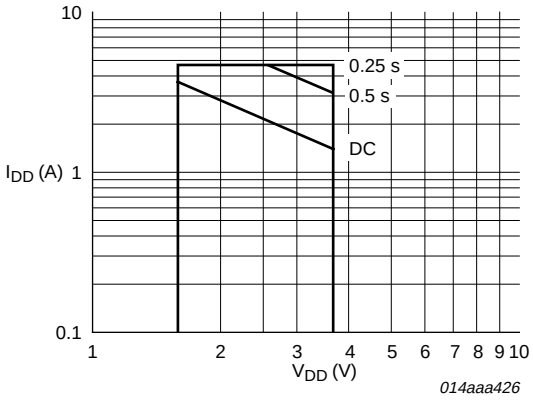

Fig 8. Safe operating area for the NE57810

After the power is estimated, the minimum PCB area can be determined by calculating the worst case thermal resistance and, based on Figure 7, determine the PCB area. This is done by Equation 3:

$$R_{qJA(min)} = \frac{T_j - T_{amb}}{P_D} \quad (3)$$

Where:

- T_j is the maximum desired junction temperature.
- T_{amb} is the highest expected local ambient temperature.
- P_D is the estimated average power

The junction temperature should be kept well away from the overtemperature cut-off threshold temperature (+150 °C) in normal operation. Using the above power dissipation, the highest ambient temperature and a junction temperature of +125 °C, calculate the maximum thermal resistance using Equation 4, (1.5 W is used only as an example).

$$R_{th((j-a)(min))} = \frac{125°C - 70°C}{1.5W} = 36.6°C/W \quad (4)$$

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Looking at Figure 7, you see that this power dissipation requires a minimum PCB island area of 225 mm^2 (15 mm on each side). This is the smallest area you could use at this power dissipation. Of course, increasing this area will allow the NE57810 to operate at cooler temperatures, thus enhancing its long-term reliability.

11. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage	V_{DD} to V_{SS} voltage	–0.3	+3.6	V
T_{amb}	ambient temperature		0	+70	°C
T_{stg}	storage temperature		–40	+165	°C
T_j	junction temperature		-	160	°C
P_D	power dissipation	[1]	-	3.3	W

[1] Tested on a minimum footprint on a four-layer PCB per JEDEC specification JESD51-7

12. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		16.5	°C/W

13. Characteristics

Table 5. Characteristics

T_{amb} = 0 °C to +70 °C, V_{DD} = 2.5 V; I_{TT} = –3.5 A to +3.5 A, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{TT}	output voltage	ExtRefIn not connected		-	$V_{DD}/2$	-	V
V_{ACC}	output voltage accuracy		[1]	–15	-	+15	mV
V_{DD}	supply voltage			1.6	-	3.6	V
I_Q	supply current	I_{TT} = 0 A		-	14	30	mA
I_{TT}	output current	2.5 V ≤ V_{DD} ≤ 3.6 V		–3.5	-	+3.5	A
		V_{DD} = 1.6 V		–2.5	-	+2.5	A
ΔV_{TT}	load regulation	I_{TT} = ± 1.0 A		-	±6	-	mV
		I_{TT} = ± 3.5 A		–18	-	+18	mV
C_{LOAD}	load capacitance	stable operation	[2]	-	100	-	µF
External reference in							
V_{TT}	output voltage swing			0.8	-	V_{DD} – 0.8	V
$R_{in(ExtRefIn)}$	input impedance			35	50	-	kΩ
	output voltage accuracy	I_{TT} = 0 A	[3]	–15	-	+15	mV
	line regulation	ExtRefIn = 1.25 V; V_{DD} = 2.25 – 3.6 V		–6	-	+6	mV

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Table 5. Characteristics *...continued*

T_{amb} = 0 °C to +70 °C, V_{DD} = 2.5 V; I_{TT} = –3.5 A to +3.5 A, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference out							
RefOut	voltage reference out	IrefOut = 0 A; source or sink	[4]	–15	ExtRefIn	+15	mV
IrefOut	reference out current max			2.2	3	-	mA
C_{LOAD}	load capacitance	stable operation		0.1	-	-	µF
Power stage							
I_{Ilim}	current limit			3.6	4.5	6.5	A
T_{lim}	temperature shutdown			-	150	-	°C
	temperature shutdown hysteresis			-	20	-	°C

[1] $V_{ACC} = V_{TT} – V_{DD}/2$.

[2] Ceramic capacitors only. Low ESR electrolytic capacitors are not necessary.

[3] Voltage accuracy refers to voltage at ExtRefIn pin.

[4] RefOut voltage referenced to 0.5 V_{DD} if ExtRefIn is not connected.

14. Typical performance curves

Figure 9 through Figure 13 show the typical performance curves for the NE57810.

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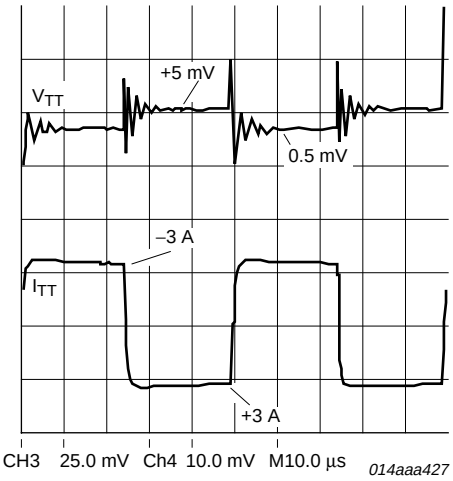

Fig 9. V_{TT} transient response (output filter 50 µF ceramic)

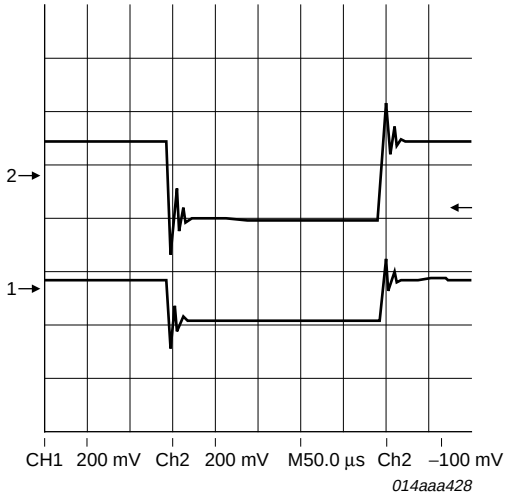

Fig 10. V_{DD} to V_{TT} response (output filter 50 µF ceramic)

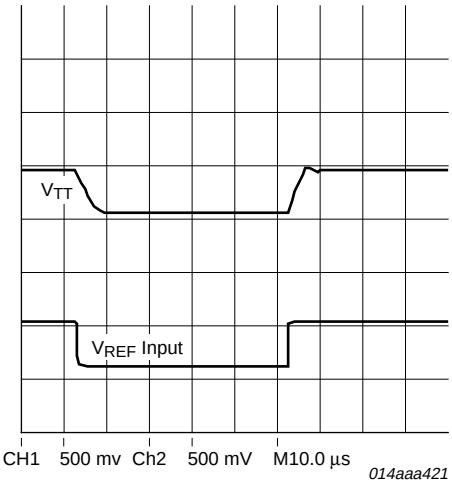

Fig 11. V_{REF} to V_{TT} transient response (output filter 820 µF + 50 µF ceramic)

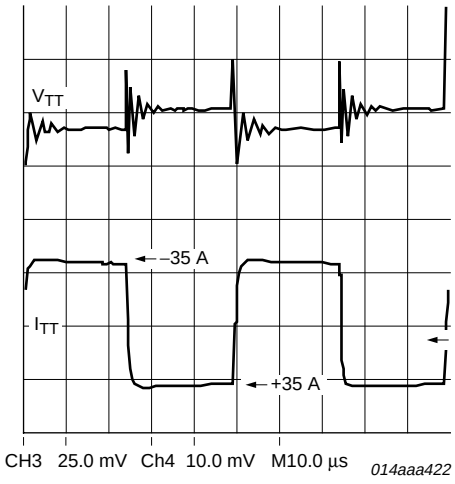

Fig 12. V_{REF} to V_{TT} transient response (output filter 50 µF ceramic)

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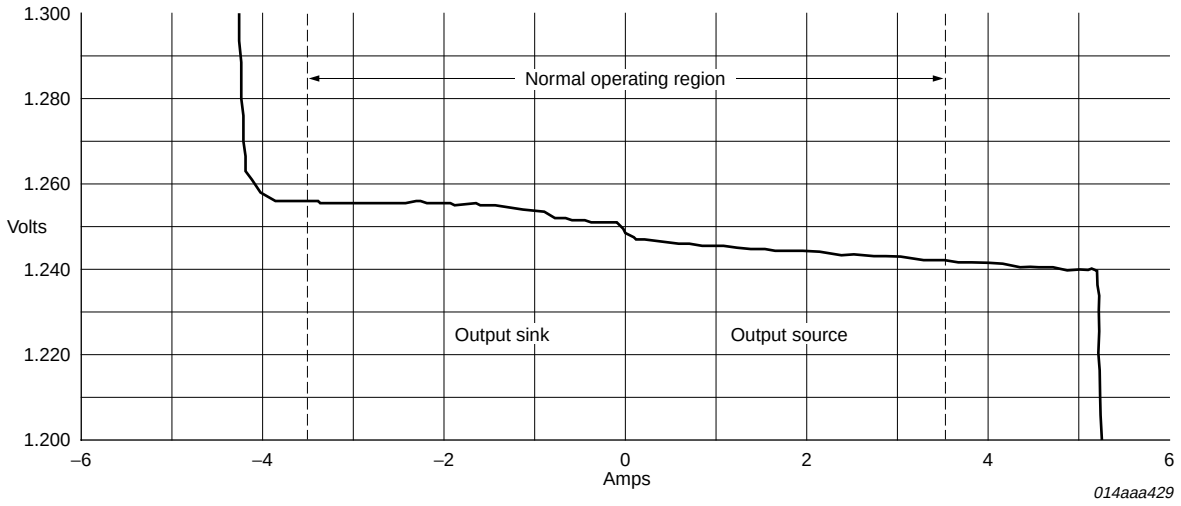

Fig 13. Typical V_{TT} versus output current (V_{DD} = 2.5 V at 25 °C)

15. Test information

Figure 14, Figure 15 and Figure 16 show the diagrams for the NE57810 test circuits.

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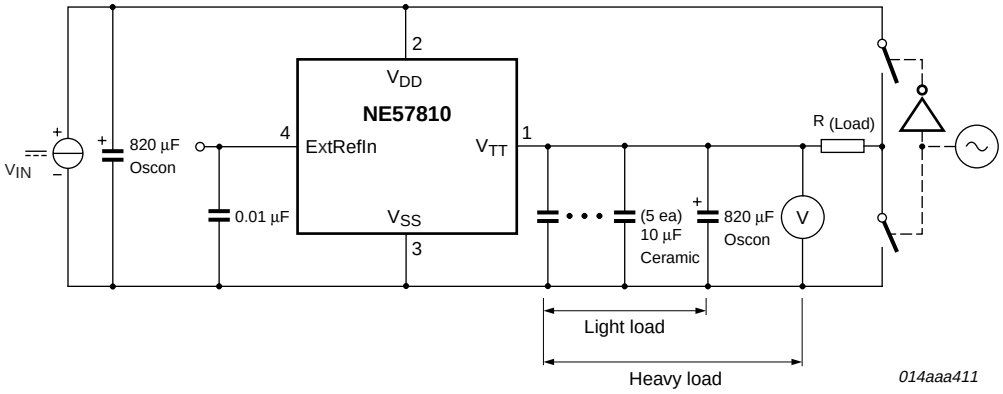

Fig 14. Load transient test (+3 A to –3 A)

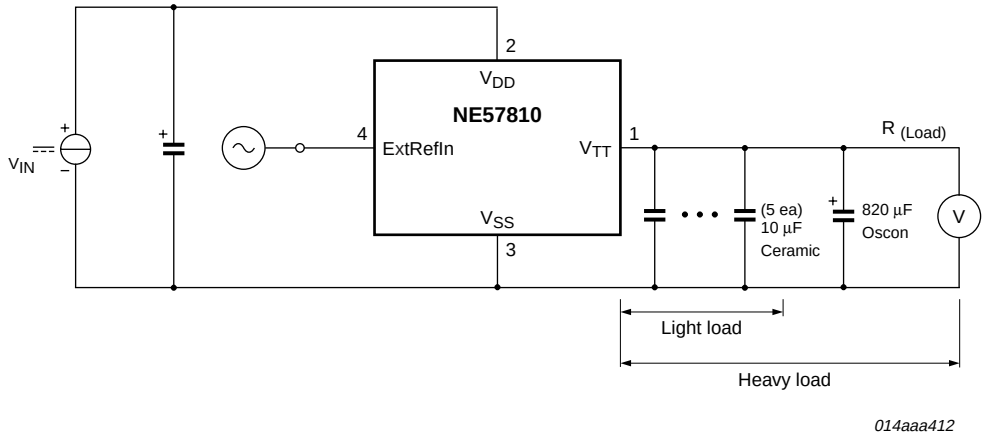

Fig 15. ExtRefIn to V_{TT} transient test

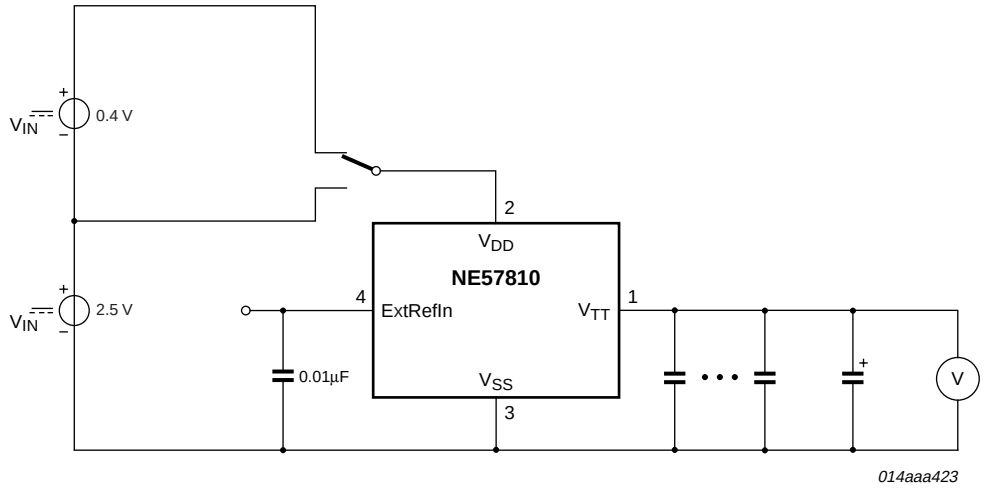

Fig 16. V_{DD} to V_{TT} transient test

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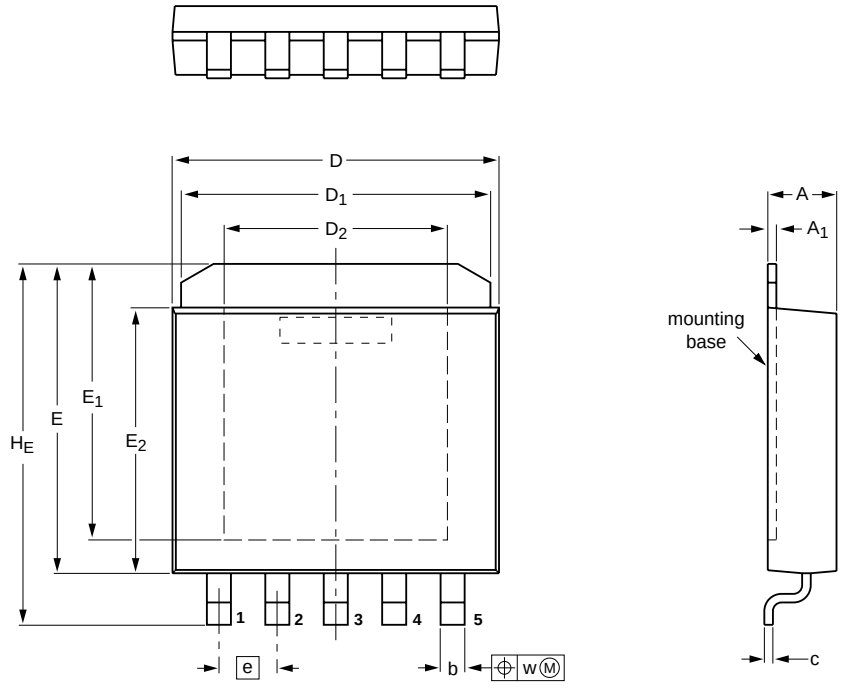
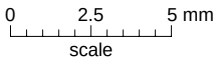
16. Package outline

Plastic single-ended surface-mounted package; 5 leads **SOT756**





DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D	D_1	D_2	E	E_1	E_2	e	H_E	w
mm	2.05 1.75	0.3 0.2	0.76 0.65	0.3 0.2	9.60 9.25	9.15 8.85	5.75 5.45	9.20 8.85	7.65 7.40	8.15 7.85	1.7	10.7 10.4	0.25

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT756						~~08-02-08~~ 08-02-15

Fig 17. Package outline SOT756

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17. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NE57810_4	20081124	Product data sheet	-	NE57810_3
Modifications:	• The values for I_{Ilim} in Table 5 has been updated.			
NE57810_3	20080702	Product data sheet	-	NE57810_2
NE57810_2	20030912	Product data sheet	-	NE57810_1
NE57810_1	20020716	Product data sheet	-	-

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18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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