Document Number: MRF7S35120HS
Rev. 1, 6/2008

RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

MRF7S35120HSR3

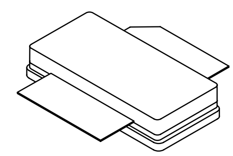
3100-3500 MHz, 120 W PEAK, 32 V PULSED LATERAL N-CHANNEL RF POWER MOSFET

Designed for pulsed wideband applications operating at frequencies between 3100 and 3500 MHz.

- Typical Pulsed Performance: V_{DD} = 32 Volts, I_{DQ} = 150 mA, P_{out} = 120 Watts Peak (24 Watts Avg.), Pulsed Signal, f = 3500 MHz, Pulse Width = 100 µsec, Duty Cycle = 20%
  - Power Gain — 12 dB
  - Drain Efficiency — 40%
- Typical WiMAX Performance: V_{DD} = 32 Volts, I_{DQ} = 900 mA, P_{out} = 18 Watts Avg., f = 3500 MHz, 802.16d, 64 QAM $^3/_4$, 4 Bursts, 7 MHz Channel Bandwidth, Input Signal PAR = 9.5 dB @ 0.01% Probability on CCDF
  - Power Gain — 13 dB
  - Drain Efficiency — 16%
  - RCE — -33 dB (EVM — 2.2% rms)
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 3300 MHz, 120 Watts Peak Power
- Capable of Handling 3 dB Overdrive @ 32 Vdc

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 32 V_{DD} Operation
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.



CASE 465A-06, STYLE 1
NI-780S

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 79°C, 120 W Pulsed, 100 µsec Pulse Width, 20% Duty Cycle Case Temperature 72°C, 120 W Pulsed, 500 µsec Pulse Width, 10% Duty Cycle	$R_{\theta JC}$	 0.11 0.12	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

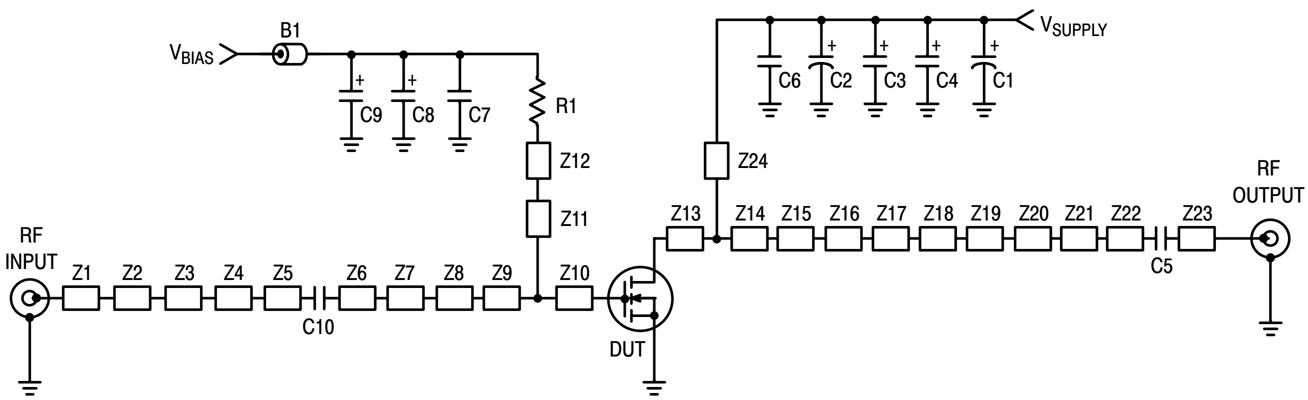
Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 400 μAdc)	$V_{GS(th)}$	1.2	1.9	2.7	Vdc
Gate Quiescent Voltage (V_{DD} = 32 Vdc, I_D = 150 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.5	2.4	3	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.0 Adc)	$V_{DS(on)}$	0.1	0.17	0.3	Vdc
Dynamic Characteristics [1]					
Reverse Transfer Capacitance (V_{DS} = 32 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	0.87	—	pF
Output Capacitance (V_{DS} = 32 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	464	—	pF
Input Capacitance (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	214	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 32 Vdc, I_{DQ} = 150 mA, P_{out} = 120 W Peak (24 W Avg.), f = 3100 MHz and f = 3500 MHz, Pulsed, 100 μsec Pulse Width, 20% Duty Cycle, 25 ns Input Rise Time					
Power Gain	G_{ps}	10.5	12	13.5	dB
Drain Efficiency	η_D	38	40	—	%
Input Return Loss	IRL	—	-15	-8	dB
Pulsed RF Performance (In Freescale Application Test Fixture, 50 ohm system) V_{DD} = 32 Vdc, I_{DQ} = 150 mA, P_{out} = 120 W Peak (24 W Avg.), f = 3100 MHz and f = 3500 MHz, Pulsed, 100 μsec Pulse Width, 20% Duty Cycle, 25 ns Input Rise Time					
Output Pulse Droop (500 μsec Pulse Width, 10% Duty Cycle)	DRP_{out}	—	0.3	—	dB
Load Mismatch Tolerance (VSWR = 10:1 at all Phase Angles)	VSWR-T	No Degradation in Output Power			

1. Part internally matched both on input and output.



Z1	0.120″ x 0.082″ Microstrip	Z14	0.390″ x 0.576″ Microstrip
Z2*	0.094″ x 0.310″ Microstrip	Z15	0.202″ x 0.082″ Microstrip
Z3*	0.3502″ x 0.082″ Microstrip	Z16	0.066″ x 0.162″ Microstrip
Z4	0.120″ x 0.629″ Microstrip	Z17	0.084″ x 0.330″ Microstrip
Z5, Z22	0.050″ x 0.082″ Microstrip	Z18	0.105″ x 0.082″ Microstrip
Z6	0.052″ x 0.082″ Microstrip	Z19	0.080″ x 0.147″ Microstrip
Z7	0.084″ x 0.436″ Microstrip	Z20	0.366″ x 0.082″ Microstrip
Z8	1.142″ x 0.082″ Microstrip	Z21	0.070″ x 0.207″ Microstrip
Z9	0.144″ x 0.564″ Microstrip	Z23	0.734″ x 0.082″ Microstrip
Z10	0.078″ x 0.564″ Microstrip	Z24	0.071″ x 0.477″ Microstrip
Z11	0.048″ x 1.349″ Microstrip	PCB	Arlon CuClad 250GX-0300-55-22, 0.030″, ε_r = 2.55
Z12	0.120″ x 0.175″ Microstrip		* Line length includes microstrip bends
Z13	0.087″ x 0.576″ Microstrip		

Figure 1. MRF7S35120HSR3 Test Circuit Schematic

Table 5. MRF7S35120HSR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1	47 Ω, 100 MHz Short Ferrite Bead	2743019447	Fair-Rite
C1	470 μF, 63 V Electrolytic Capacitor	477KXM063M	Illinois Cap.
C2	47 μF, 50 V Electrolytic Capacitor	476KXM050M	Illinois Cap.
C3, C4	22 μF, 35 V Tantalum Capacitors	T491X226K035AT	Kemet
C5	3.3 pF Chip Capacitor	ATC100B3R3CT500XT	ATC
C6, C7, C10	2.7 pF Chip Capacitors	ATC100B2R7BT500XT	ATC
C8, C9	22 μF, 25 V Tantalum Capacitors	ECS-T1ED226R	Panasonic TE series
R1	51 Ω, 1/4 W Chip Resistor	CRCW120651R0FKEA	Vishay

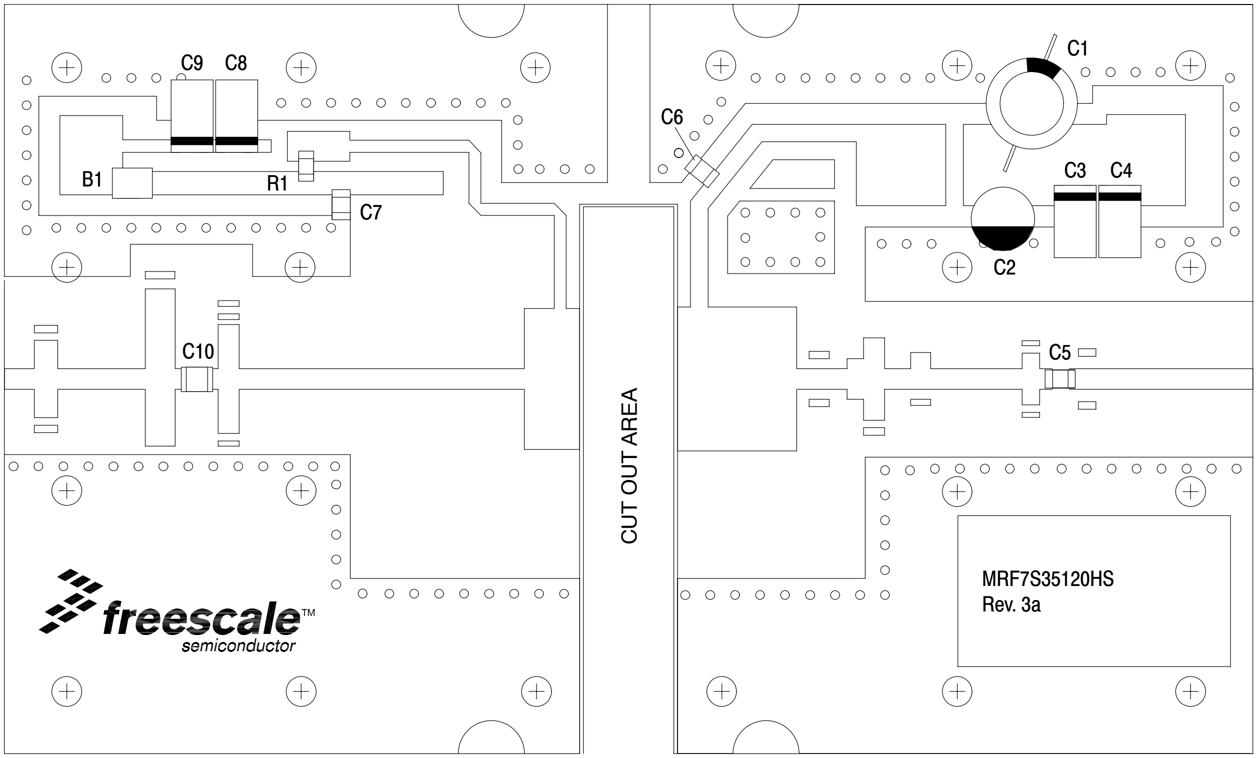


Figure 2. MRF7S35120HSR3 Test Circuit Component Layout

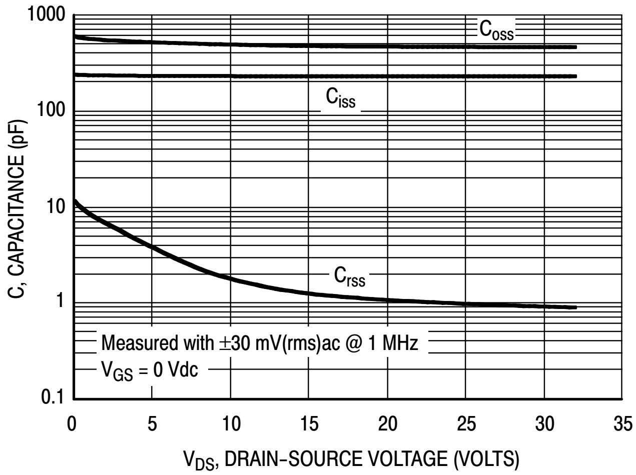


Figure 3. Capacitance versus Drain-Source Voltage

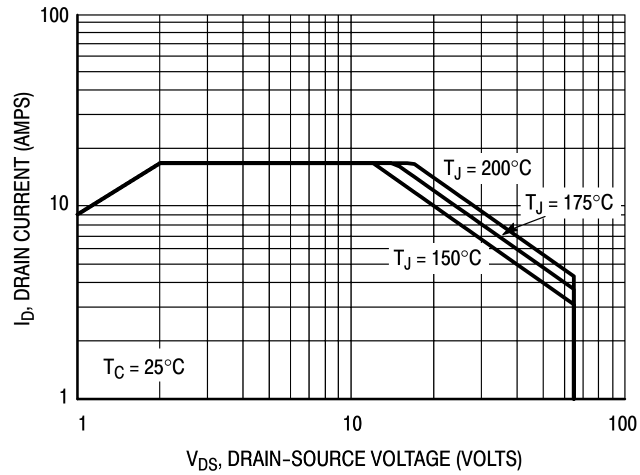


Figure 4. DC Safe Operating Area

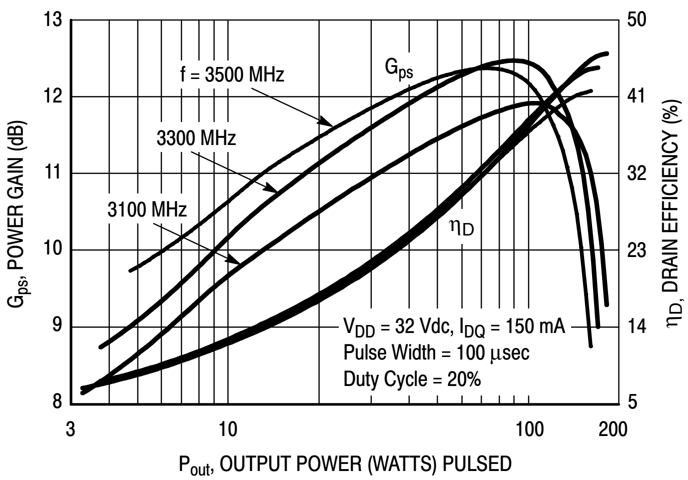


Figure 5. Pulsed Power Gain and Drain Efficiency versus Output Power

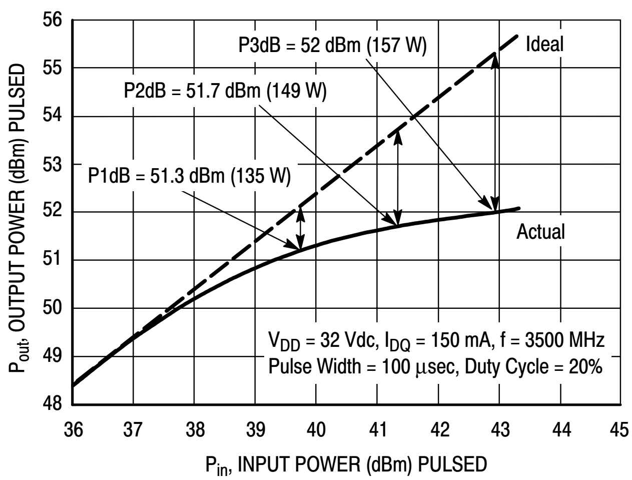


Figure 6. Pulsed Output Power versus Input Power

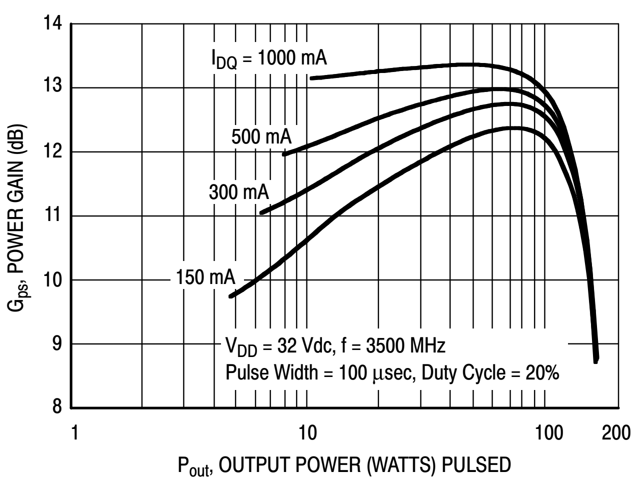


Figure 7. Pulsed Power Gain versus Output Power

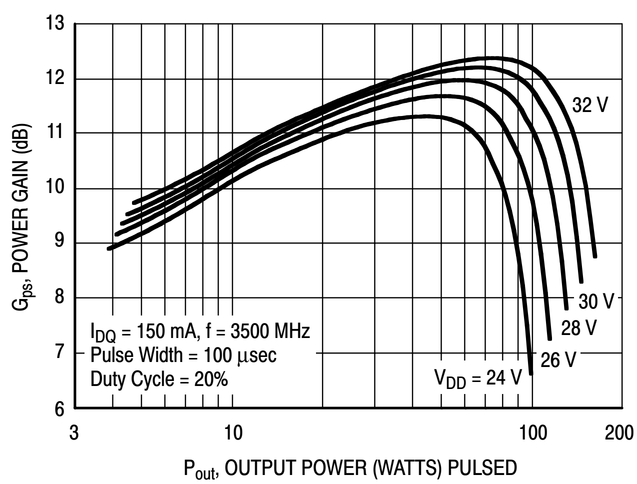


Figure 8. Pulsed Power Gain versus Output Power

TYPICAL CHARACTERISTICS

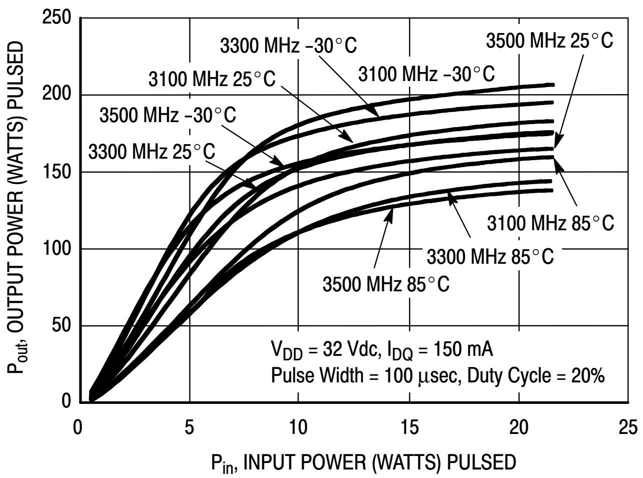


Figure 9. Pulsed Output Power versus Input Power

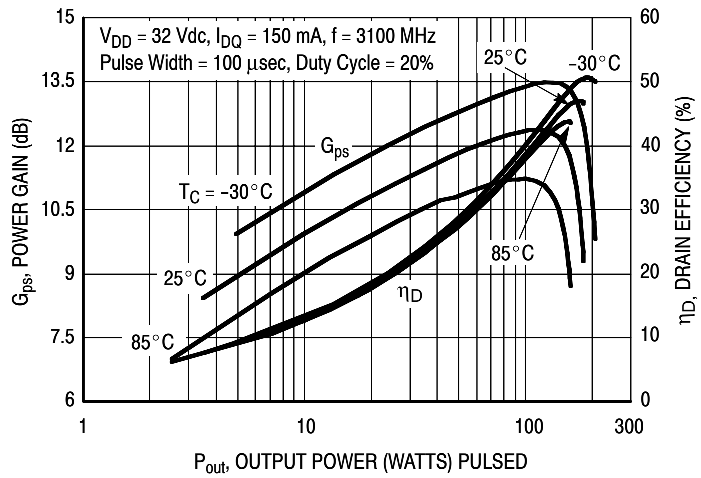


Figure 10. Pulsed Power Gain and Drain Efficiency versus Output Power — 3100 MHz

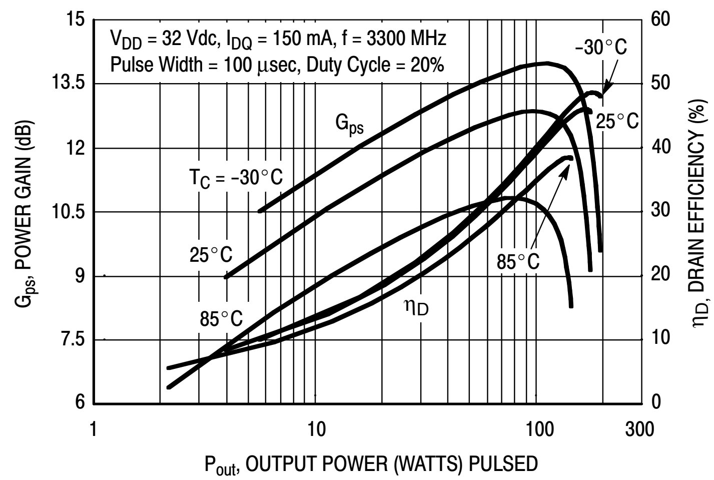


Figure 11. Pulsed Power Gain and Drain Efficiency versus Output Power — 3300 MHz

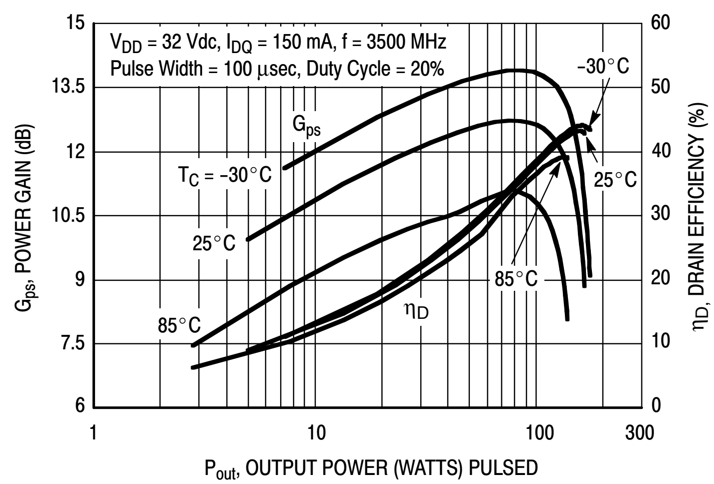


Figure 12. Pulsed Power Gain and Drain Efficiency versus Output Power — 3500 MHz

TYPICAL CHARACTERISTICS

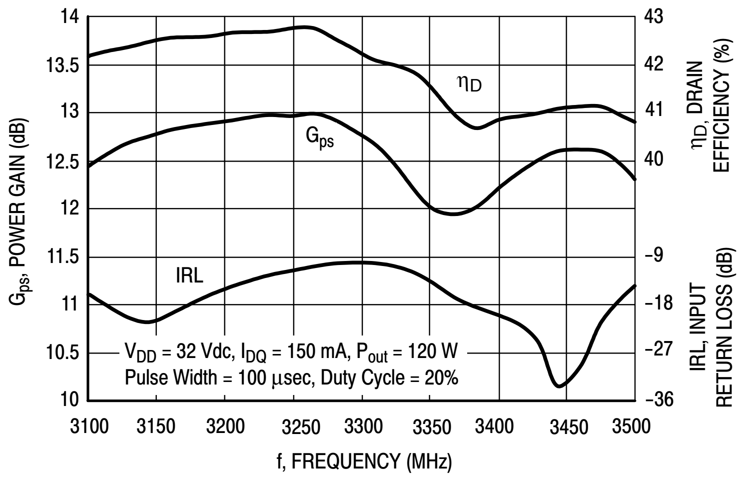


Figure 13. Pulsed Power Gain, Drain Efficiency and IRL versus Frequency

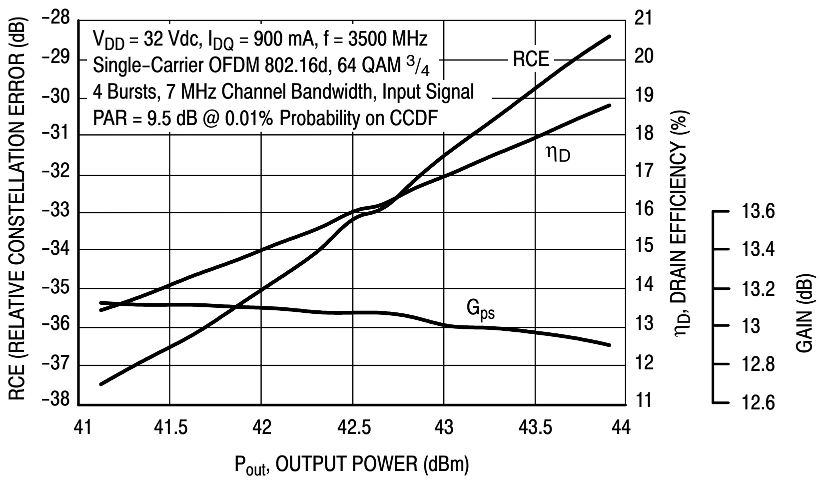
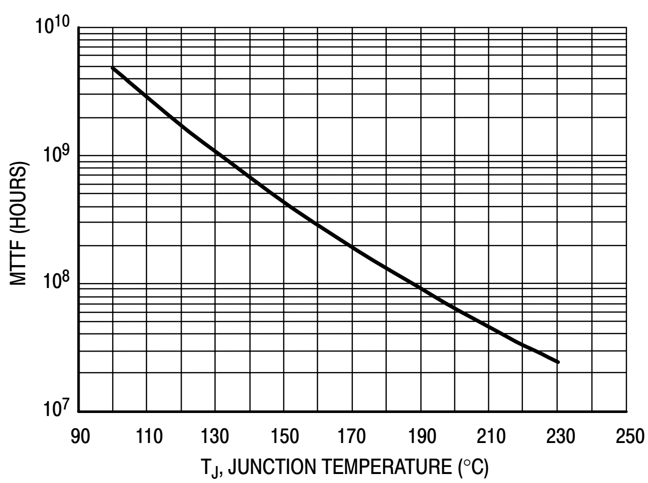


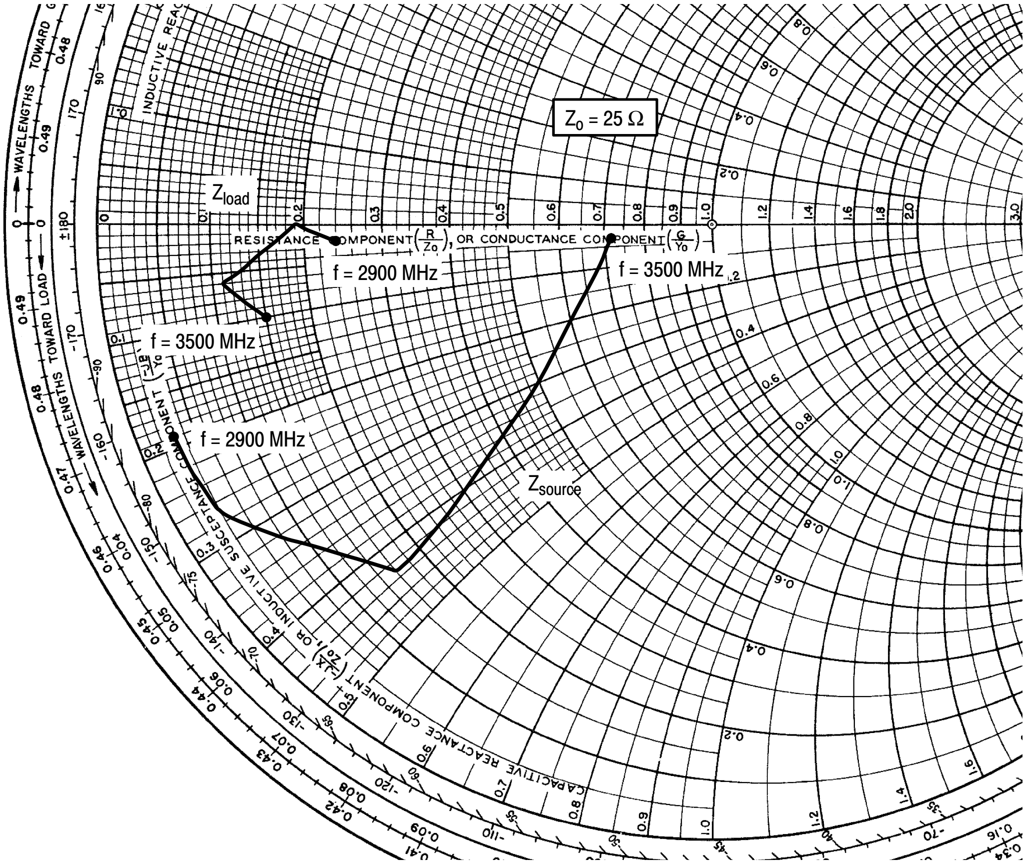
Figure 14. Single-Channel OFDM Relative Constellation Error, Drain Efficiency and Gain versus Output Power



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 32 Vdc, P_{out} = 120 W Peak, Pulse Width = 100 μsec, Duty Cycle = 20%, and η_D = 40%.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 15. MTTF versus Junction Temperature



V_{DD} = 32 Vdc, I_{DQ} = 150 mA, P_{out} = 120 W Peak

f MHz	Z_{source} Ω	Z_{load} Ω
2900	0.825 - j4.72	6.03 - j0.487
3100	1.1 - j6.74	4.63 - j0.0472
3300	3.95 - j10.8	2.65 - j1.44
3500	18 - j1.1	3.65 - j2.56

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

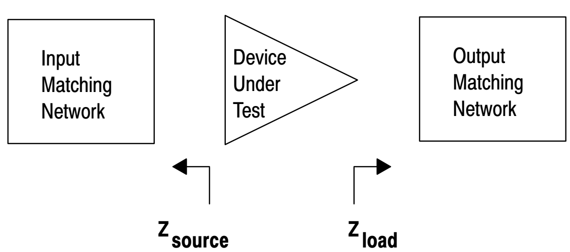
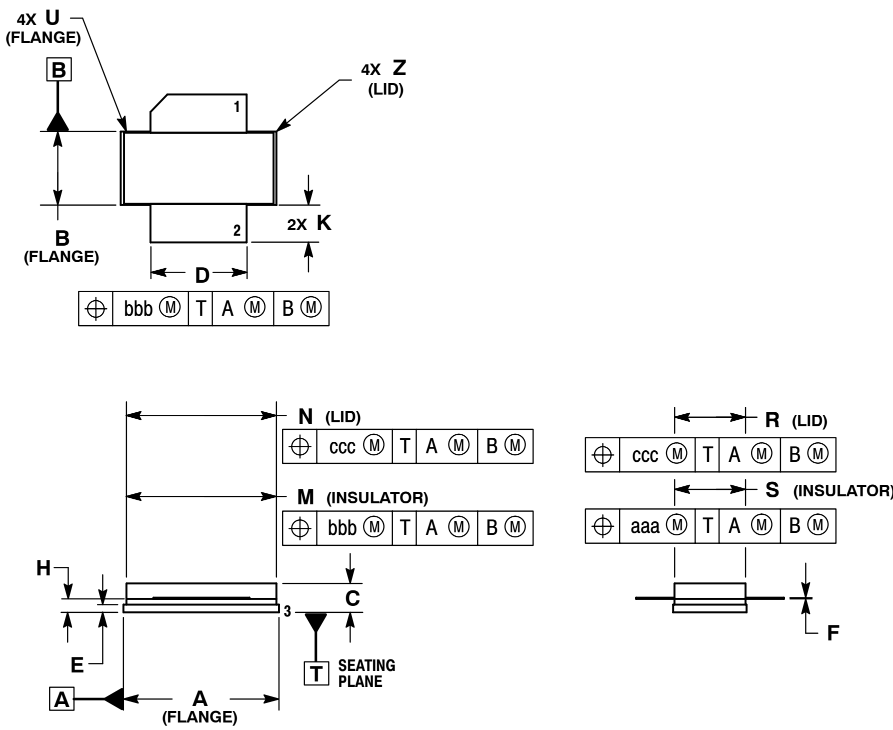


Figure 16. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M−1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
5. SOURCE

CASE 465A-06
ISSUE H
NI-780S

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2008	• Initial Release of Data Sheet
1	June 2008	• Corrected P_{out} error and changed from 42.5 Watts to 18 Watts, Typical WiMAX Performance bullet, p. 1

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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
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