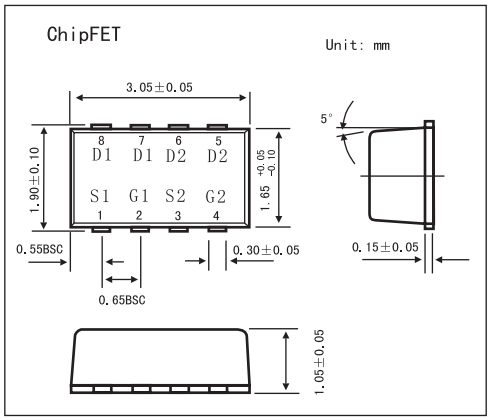
Silicon P, N Channel MOS Type Transistor

KPCF8402

Features

- Low drain-source ON resistance
  : P Channel $R_{DS\ (ON)}$ = 60 mΩ (typ.)
  N Channel $R_{DS\ (ON)}$ = 38 mΩ (typ.)
- High forward transfer admittance
  : P Channel $|Y_{fs}|$ = 5.9 S (typ.)
  N Channel $|Y_{fs}|$ = 6.8 S (typ.)
- Low leakage current
  : P Channel I_{DSS} = -10 μA (V_{DS} = -30 V)
  N Channel I_{DSS} = 10 μA (V_{DS} = 30 V)
- Enhancement-mode
  : P Channel V_{th} = -0.8 to -2.0 V (V_{DS} = -10 V, I_D = -1mA)
  N Channel V_{th} = 1.3 to 2.5 V (V_{DS} = 10 V, I_D = 1mA)



Absolute Maximum Ratings Ta = 25℃

Parameter		Symbol	P-Channel	N-Channel	Unit
Drain-source voltage		V_{DSS}	-30	30	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	-30	30	V
Gate-source voltage		V_{GSS}	±20	±20	V
Drain current	DC (Note 1)	I_D	-3.2	4	A
	Pulse (Note 1)	I_{DP}	-12.8	16	A
Drain power dissipation (t = 5 s)	Single-device operation (Note 3a)	$P_{D\ (1)}$	1.35	1.35	W
	Single-device value at dual operation(Note 3b)	$P_{D\ (2)}$	1.12	1.12	
Drain power dissipation (t = 5 s) (Note 2b)	Single-device operation (Note 3a)	$P_{D\ (1)}$	0.53	0.53	
	Single-device value at dual operation(Note 3b)	$P_{D\ (2)}$	0.33	0.33	
Single pulse avalanche energy(Note 4)		E_{AS}	0.67	2.6	mJ
Avalanche current		I_{AR}	-1.6	2	A
Repetitive avalanche energy Single-device value at dual operation (Note 2a, 3b, 5)		E_{AR}	0.11		mJ
Channel temperature		T_{ch}	150		℃
Storage temperature range		T_{stg}	-55 to 150		℃
Thermal resistance,channel to ambient (t = 5 s) (Note 2a)	Single-device operation (Note 3a)	$R_{th\ (ch-a)\ (1)}$	92.6		℃/W
	Single-device value at dual operation (Note 3b)	$R_{th\ (ch-a)\ (2)}$	111.6		
Thermal resistance,channel to ambient (t = 5 s) (Note 2b)	Single-device operation (Note 3a)	$R_{th\ (ch-a)\ (1)}$	235.8		
	Single-device value at dual operation (Note 3b)	$R_{th\ (ch-a)\ (2)}$	378.8		

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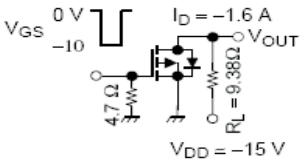
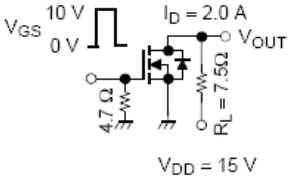
■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Gate leakage current	I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	P-Ch			±10	μA
		V_{GS} = ±16 V, V_{DS} = 0 V	N-Ch			10	μA
Drain cut-off current	I_{DSS}	V_{DS} = ?30 V, V_{GS} = 0 V	P-Ch			-10	μA
		V_{DS} = 30 V, V_{GS} = 0 V	N-Ch			10	μA
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	I_D = -10 mA, V_{GS} = 0 V	P-Ch	-30			V
	$V_{(BR)\ DSX}$	I_D = -10 mA, V_{GS} = 20 V		-15			V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	I_D =10 mA, V_{GS} = 0 V	N-Ch	30			V
	$V_{(BR)\ DSX}$	I_D = 10 mA, V_{GS} = -20 V		15			V
Gate threshold voltage	V_{th}	V_{DS} = -10 V, I_D = -1 mA	P-Ch	-0.8		-2.0	V
		V_{DS} = 10 V, I_D = 1 mA	N-Ch	1.3		2.5	V
Drain-source ON resistance	$R_{DS\ (ON)}$	V_{GS} = -4.5 V, I_D = -1.6A	P-Ch		80	105	mΩ
		V_{GS} = -10 V, I_D = -1.6 A			60	72	
Drain-source ON resistance	$R_{DS\ (ON)}$	V_{GS} = 4.5 V, I_D = 2.0A	N-Ch		58	77	mΩ
		V_{GS} = 10 V, I_D = 2.0 A			38	50	
Forward transfer admittance	$\|Y_{fs}\|$	V_{DS} = -10 V, I_D = -1.6 A	P-Ch	2.9	5.9		S
		V_{DS} = 10 V, I_D = 2.0 A	N-Ch	3.4	6.8		S
Input capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	P-Ch		600		pF
Reverse transfer capacitance	C_{rss}				60		
Output capacitance	C_{oss}				70		
Input capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	N-Ch		470		pF
Reverse transfer capacitance	C_{rss}				60		
Output capacitance	C_{oss}				80		
Switching time Rise time	t_r		P-Ch		5.3		ns
Switching time Turn-on time	t_{on}				12		
Switching time Fall time	t_f				8.4		
Switching time Turn-off time	t_{off}				34		
Switching time Rise time	t_r		N-Ch		5.2		ns
Switching time Turn-on time	t_{on}				8.3		
Switching time Fall time	t_f				4.0		
Switching time Turn-off time	t_{off}				22		
Total gate charge (gate-source plus gate-drain)	Q_g	V_{DD}=-24V,V_{GS}=-10V,I_D=-3.2A	P-Ch		14		nC
Gate-source charge 1	Q_{gs1}				1.4		
Gate-drain (Gate-source charge "miller") charge	Q_{gd}				2.7		

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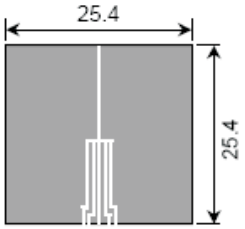
Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	V_{DD}=24V,V_{GS}=10V,I_D=6A	N-Ch		10		nC
Gate-source charge 1	Q_{gs1}				1.7		
Gate-drain ("miller") charge	Q_{gd}				2.4		
Drain reverse current Pulse (Note 1)	I_{DRP}		P-Ch			-12.8	A
						16	A
Forward voltage (diode)	V_{DSF}	I_{DR} =-3.2 A, V_{GS} = 0 V	N-Ch			1.2	V
		I_{DR} =4.0 A, V_{GS} = 0 V				-1.2	V

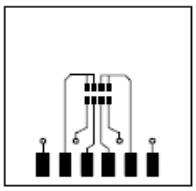
Note 1: Please use devices on condition that the channel temperature is below 150°C.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

(a)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

(b)

Note 3: a) The power dissipation and thermal resistance values are shown for a single device (During single-device operation, power is only applied to one device.).

b) The power dissipation and thermal resistance values are shown for a single device (During dual operation, power is evenly applied to both devices.).

Note 4: P Channel: V_{DD} = –24 V, T_{ch} = 25°C (initial), L = 0.2 mH, R_G = 25 Ω, I_{AR} = –1.6 A
N Channel: V_{DD} = 24 V, T_{ch} = 25°C (initial), L = 0.5 mH, R_G = 25 Ω, I_{AR} = 2.0 A

Note 5: Repetitive rating; Pulse width limited by Max. Channel temperature.

Note 6: Black round marking "• " locates on the left lower side of parts number marking "F6B indicates terminal No. 1.

■ Circuit Configuration