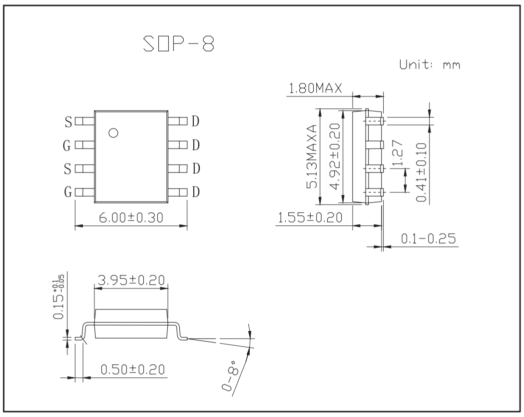
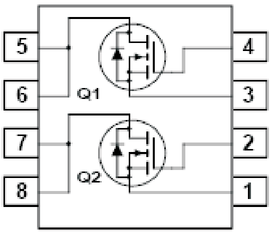
100V Dual N-Channel PowerTrench MOSFET

KDS3601



■ Features

- 1.3 A, 100 V. $R_{DS(ON)}$ = 480mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 530mΩ @ V_{GS} = 6 V
- Low gate charge (3.7 nC typical)
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability



■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current Continuous (Note 1a)	I_D	1.3	A
Drain Current Pulsed		6	A
Power Dissipation for Dual Operation	P_D	2	
Power Dissipation for Single Operation (Note 1a)	P_D	1.6	W
Power Dissipation for Single Operation (Note 1b)		1	
Power Dissipation for Single Operation (Note 1c)		0.9	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	℃
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	40	℃/W
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	78	℃/W

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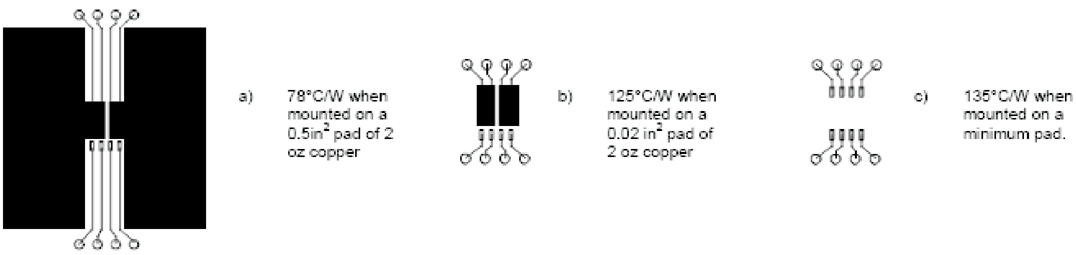
■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Single Pulse Drain-Source Avalanche Energy	W_{DSS}	Single Pulse, V_{DD}=50V, I_D=1.3A(Not 2)			26	mJ
Maximum Drain-Source Avalanche Current	I_{AR}	(Not 2)			1.3	A
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250 µA	100			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D = 250 µA, Referenced to 25℃		105		mV/℃
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			10	µA
Gate-Body Leakage, Forward	I_{GSSF}	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
Gate-Body Leakage, Reverse	I_{GSSR}	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2	2.6	4	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D = 250 µA, Referenced to 25℃		-5		mV/℃
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 1.3 A		350	480	mΩ
		V_{GS} = 6 V, I_D = 1.3 A		376	530	
		V_{GS} = 10 V, I_D =1.3 A, TJ = 125℃		664	955	
On-State Drain Current	$I_{D(on)}$	V_{GS} = 10 V, V_{DS} = 10V	3			A
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 1.3 A		3.6		S
Input Capacitance	C_{iss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1.0 MHz		153		pF
Output Capacitance	C_{oss}			5		pF
Reverse Transfer Capacitance	C_{rss}			1		pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		8	16	ns
Turn-On Rise Time	t_r			4	8	ns
Turn-Off Delay Time	$t_{d(off)}$			11	20	ns
Turn-Off Fall Time	t_f			6	5	ns
Total Gate Charge	Q_g	V_{DS} = 50 V, I_D = 1.3 A, V_{GS} = 10 V (Note 2)		3.7	80	nC
Gate-Source Charge	Q_{gs}			0.8		nC
Gate-Drain Charge	Q_{gd}			1		nC
Maximum Continuous Drain-Source Diode Forward Current	I_S				1.3	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1.3 A (Not 2)		0.8	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



2. Pulse Test: Pulse Width < 300us. Duty Cycle < 2.0%