FAIRCHILD

SEMICONDUCTOR®

December 2007

FDMS5672
N-Channel UltraFET Trench® MOSFET
60V, 22A, 11.5mΩ

Features

- Max $r_{DS(on)}$ = 11.5mΩ at V_{GS} = 10V, I_D = 10.6A
- Max $r_{DS(on)}$ = 16.5mΩ at V_{GS} = 6V, I_D = 8A
- Typ Qg = 32nC at V_{GS} = 10V
- Low Miller Charge
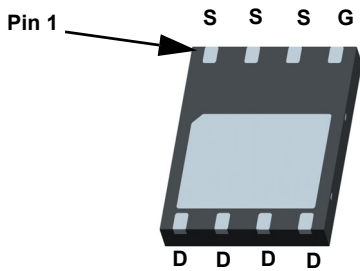- Optimized efficiency at high frequencies
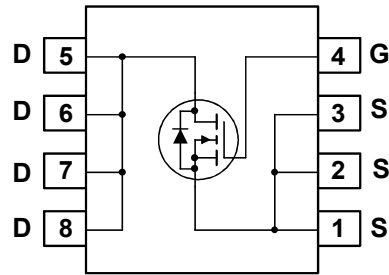- RoHS Compliant

General Description

UltraFET devices combine characteristics that enable benchmark efficiency in power conversion applications. Optimized for $r_{DS(on)}$, low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

Application

- DC - DC Conversion

S S S G

Pin 1

Power 56 (Bottom view)

D D D D

D	5		4	G
D	6		3	S
D	7		2	S
D	8		1	S

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			60	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25°C		22	A
	-Continuous (Silicon limited)	T_C = 25°C		65	
	-Continuous	T_A = 25°C	(Note 1a)	10.6	
	-Pulsed			60	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	337	mJ
P_D	Power Dissipation	T_C = 25°C		78	W
	Power Dissipation	T_A = 25°C	(Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS5672	FDMS5672	Power 56	13"	12mm	3000 units

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Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250µA, referenced to 25°C		59		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48V, V_{GS} = 0V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA	2	3.2	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250µA, referenced to 25°C		-11		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10V, I_D = 10.6A		9.4	11.5	mΩ
		V_{GS} = 6V, I_D = 8A		13.0	16.5	
		V_{GS} = 10V, I_D = 10.6A, T_J = 125°C		15.0	18.0	
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 10.6A		26		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 30V, V_{GS} = 0V, f = 1MHz		2100	2800	pF
C_{oss}	Output Capacitance			375	500	pF
C_{rss}	Reverse Transfer Capacitance			120	180	pF
R_g	Gate Resistance	f = 1MHz		1.2		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 30V, I_D = 10.6A V_{GS} = 10V, R_{GEN} = 6Ω		16	29	ns
t_r	Rise Time			17	31	ns
$t_{d(off)}$	Turn-Off Delay Time			22	35	ns
t_f	Fall Time			8	16	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V, V_{DD} = 30V, I_D = 10.6A		32	45	nC
Q_{gs}	Gate to Source Gate Charge			10		nC
Q_{gd}	Gate to Drain "Miller" Charge			8.3		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 10.6A (Note 2)		0.80	1.20	V
t_{rr}	Reverse Recovery Time	I_F = 10.6A, di/dt = 100A/µs		35	53	ns
Q_{rr}	Reverse Recovery Charge			42	63	nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
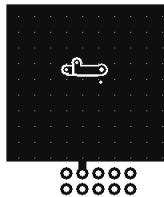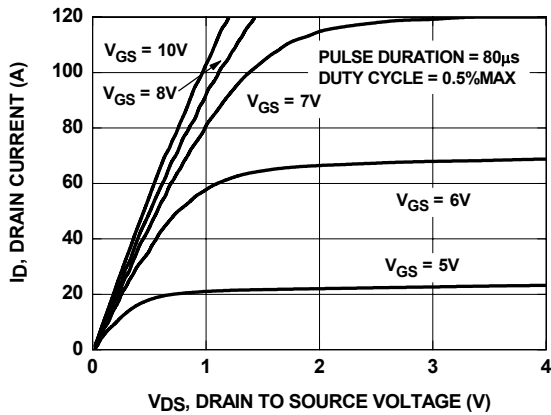
a. 50°C/W when mounted on a 1 in² pad of 2 oz copper

b. 125°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300µs, Duty cycle < 2.0%.

3: Starting T_J = 25°C, L = 3mH, I_{AS} = 15A, V_{DD} = 60V, V_{GS} = 10V.

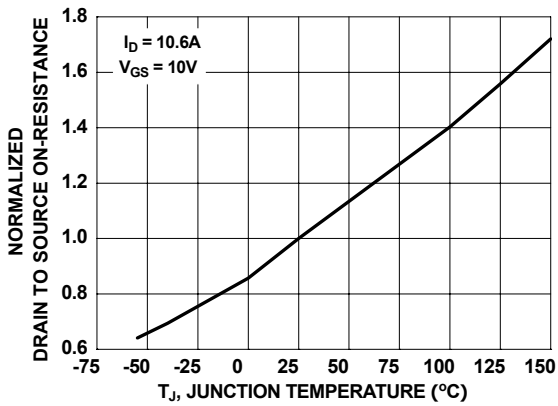## Typical Characteristics T_J = 25°C unless otherwise noted
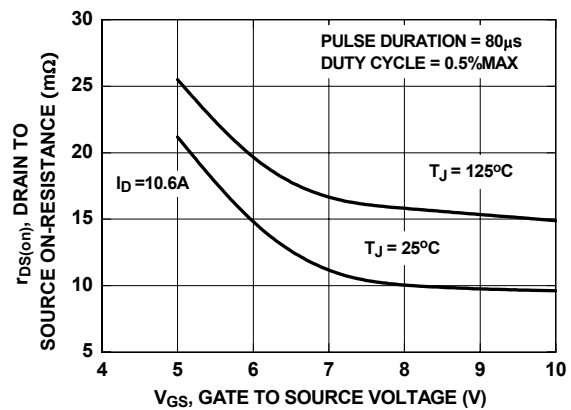
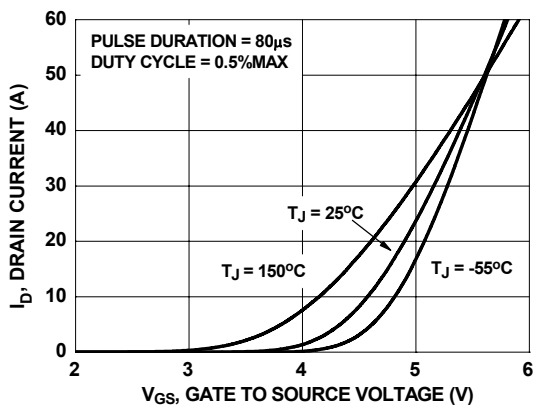**Figure 1. On Region Characteristics**
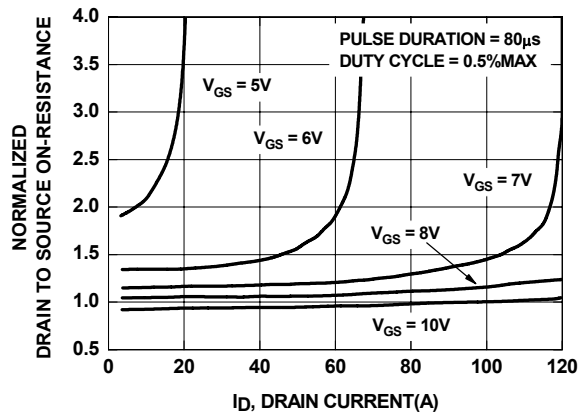
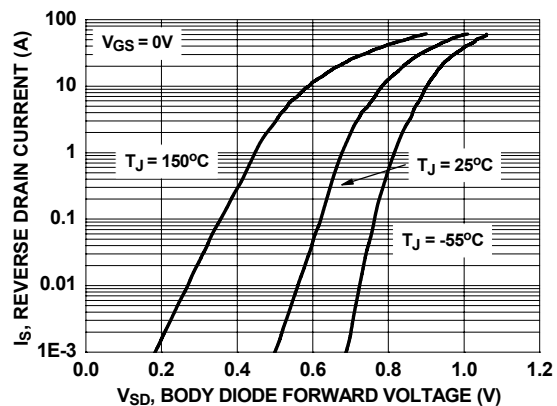**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

Figure 3. Normalized On Resistance vs Junction Temperature

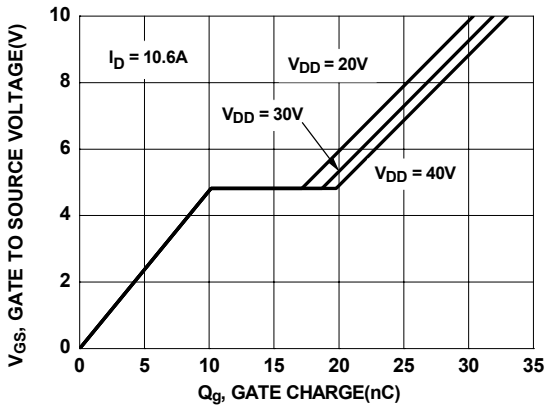**Figure 4. On-Resistance vs Gate to Source Voltage**

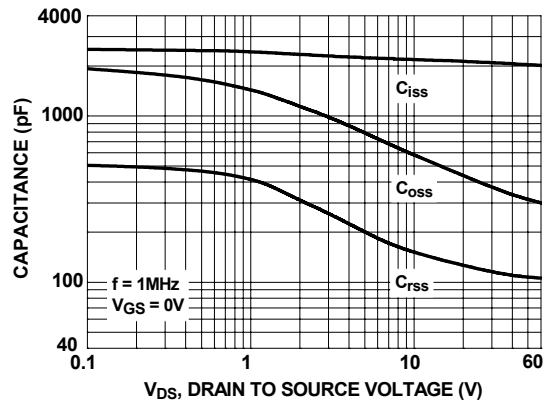**Figure 5. Transfer Characteristics**

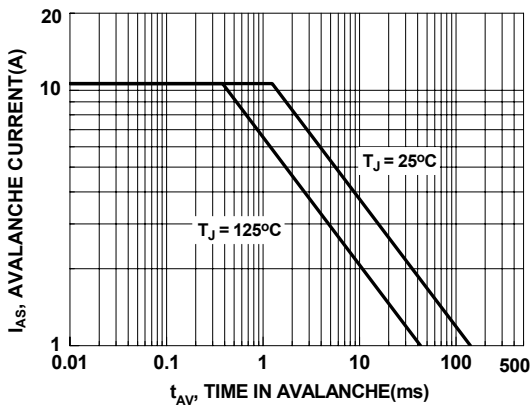**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

Typical Characteristics T_J = 25°C unless otherwise noted
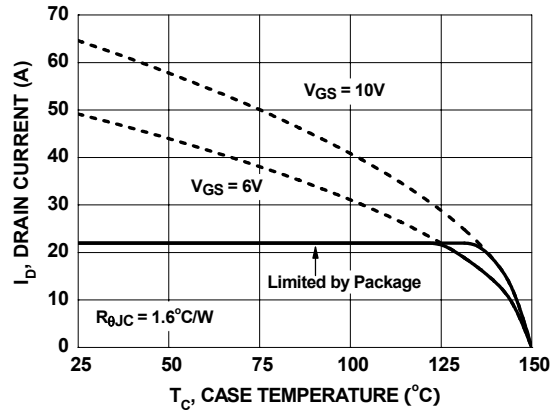

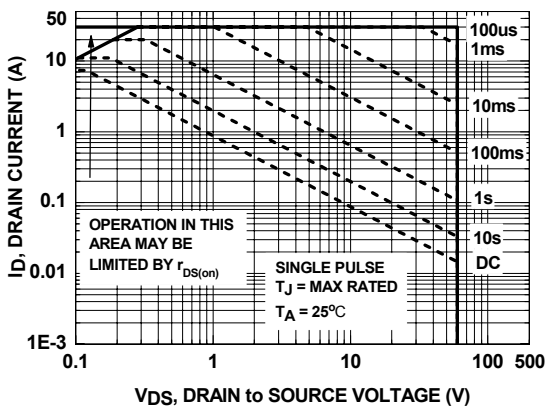**Figure 7. Gate Charge Characteristics**

Figure 8. Capacitance vs Drain to Source Voltage
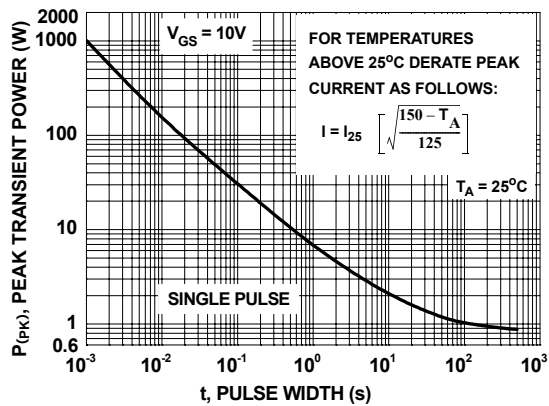

Figure 9. Unclamped Inductive Switching Capability

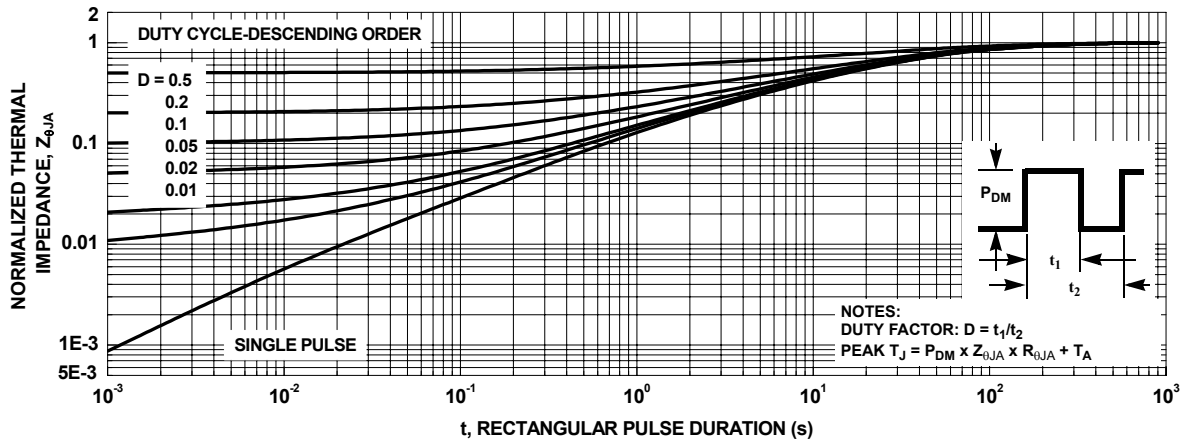**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

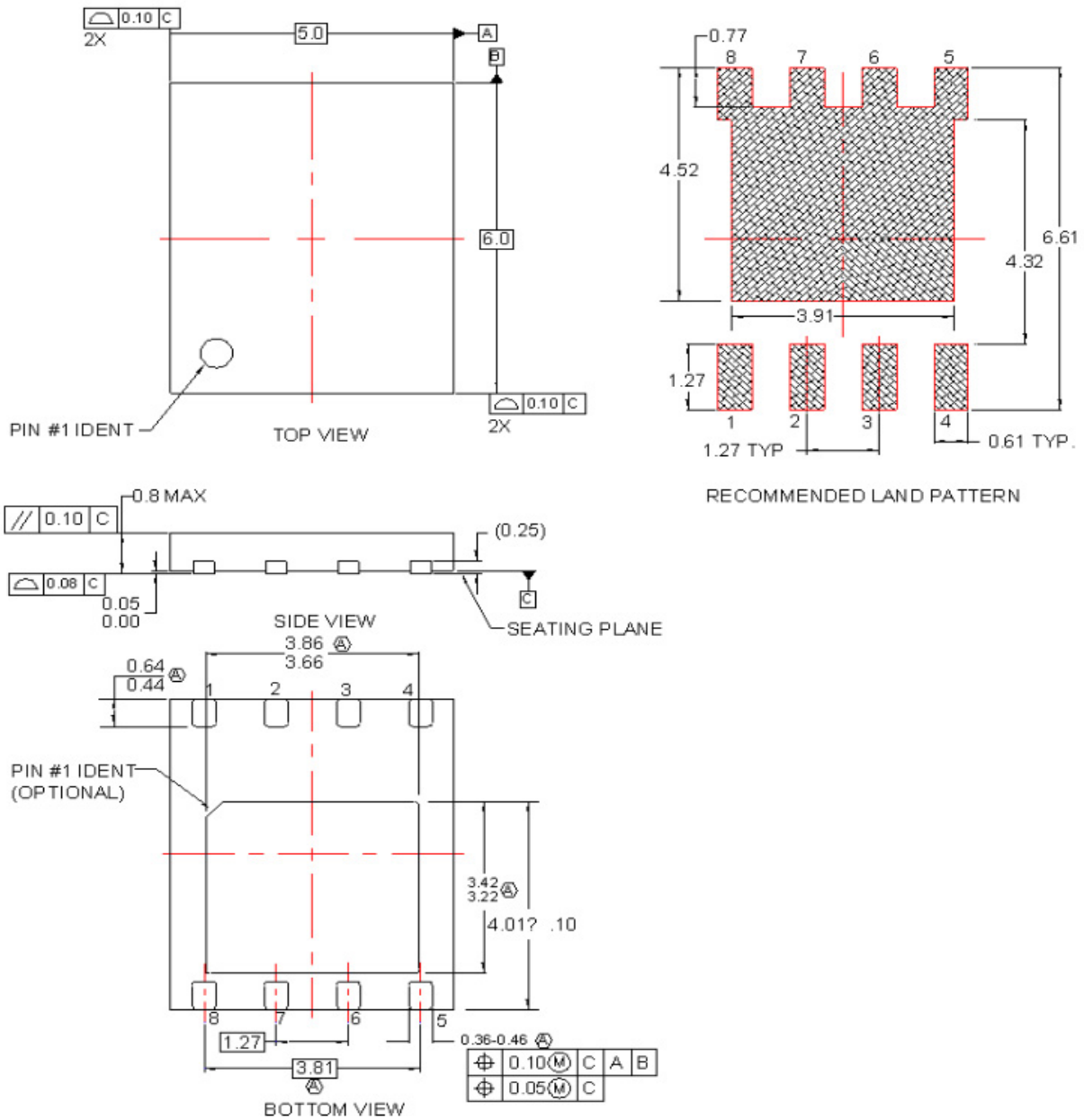**Figure 11. Forward Bias Safe Operating Area**

Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

Figure 13. Transient Thermal Response Curve

TOP VIEW

PIN #1 IDENT

2X

5.0

6.0

0.10 C

0.10 C

2X

SIDE VIEW

0.8 MAX

0.10 C

0.08 C

0.05
0.00

(0.25)

SEATING PLANE

BOTTOM VIEW

PIN #1 IDENT
(OPTIONAL)

0.64
0.44

3.86
3.66

3.42
3.22

4.01? .10

0.36-0.46

1.27

3.81

| ⊕ | 0.10 Ⓜ | C | A | B |
| ⊕ | 0.05 Ⓜ | C | | |

RECOMMENDED LAND PATTERN

0.77

4.52

3.91

6.61

4.32

1.27

1.27 TYP

0.61 TYP.

NOTES:

Ⓐ DOES NOT FULLY CONFORM TO JEDEC REGISTRATION,
   MO-229. DATED 11/2001.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER
   ASME Y14.5M, 1994

D. TERMINALS 5,6,7 AND 8 ARE TIED
   TO THE EXPOSED PADDLE

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