18-30GHz Low Noise Amplifier

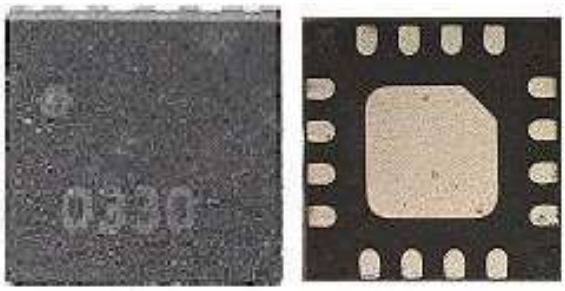
GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHA2693-QAG is a two-stage wide band monolithic low noise amplifier.

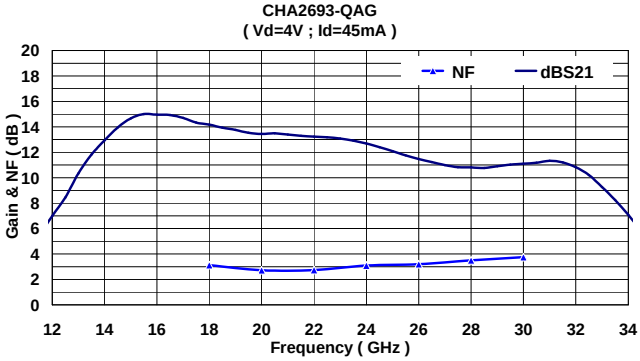
The circuit is manufactured with a standard P-HEMT process : 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in ROHS compliant SMD package.



Main Features

- Broadband performance 18-30GHz
- 3.0dB noise figure, 18-26GHz
- 13dB gain, ± 2.0dB gain flatness
- Low DC power consumption.
- 20dBm 3rd order intercept point
- 16L-QFN3x3 SMD package



Main Characteristics

Tamb = +25°C, Vd = +4.0V, Id = 45mA

Symbol	Parameter	Min	Typ	Max	Unit
NF	Noise figure, 18-26GHz		3.0		dB
G	Gain	10	13		dB
IP3	3rd order intercept point	18	20		dBm

ESD Protections : Electrostatic discharge sensitive device observe handling precautions !

United Monolithic Semiconductors S.A.S.
Route Départementale 128 - BP46 - 91401 Orsay Cedex France
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Electrical Characteristics

Tamb = +25℃, Vd = +4.0V, Vg1=Vg2 to adjust Id = 45 mA

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	18		30	Ghz
G	Gain	10	13		dB
ΔG	Gain flatness		± 2.0	± 2.5	dB
NF	Noise figure (18 to 26 GHz)		3.0		dB
VSWRin	Input VSWR (18 to 26 GHz)		3.0:1		
VSWRout	Ouput VSWR (18 to 26 GHz)		3.0:1		
IP3	3rd order intercept point	18	20		dBm
P1dB	Output power at 1dB gain compression	10	12		dBm
Id	Drain bias current		45	55	mA

These values are representative of onboard measurements as defined on the drawing 95542 (see below).

Absolute Maximum Ratings (1)

Tamb = +25℃

Symbol	Parameter (1)	Values	Unit
Vd	Drain bias voltage	4.5	V
Vg	Gate bias voltage	-2 to 0	V
Pin	Maximum peak input power overdrive (2)	+2.0	dBm
Tj	Junction Temperature (3)	175	℃
Top	Operating temperature range	-40 to +85	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these paramaters may cause permanent damage.
(2) Duration < 1s.
(3) Thermal resistance to ground paddle = 170℃/W fo r Tamb. = +85℃ (Vd=4v, Id=45mA)

Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

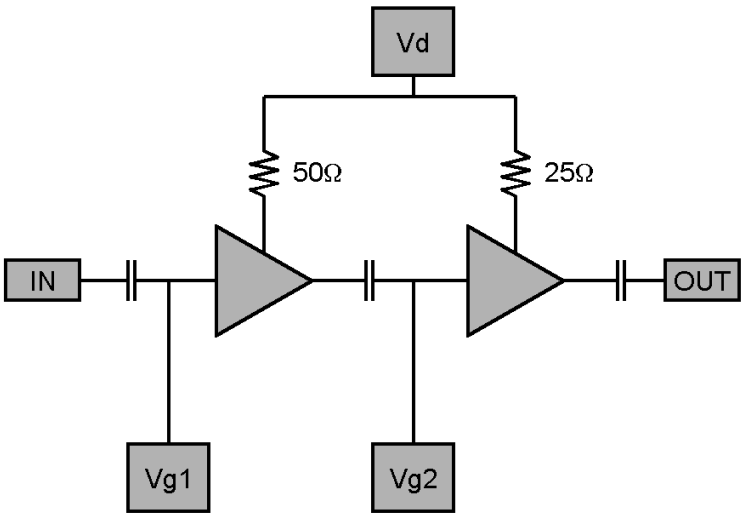
Typical Bias Conditions

for an ambient Temperature of +25°C

Symbol	Pin n°	Parameter	Values	Unit
Vd	14	Drain bias voltage	4	V
Vg1 & 2	6 & 7	First & second stages gate bias voltage (1)	-0.4	V
Id	14	Drain current	45	mA

(1) Typically, Vg1=Vg2 and Vg1&2 are adjusted so that Id=45mA

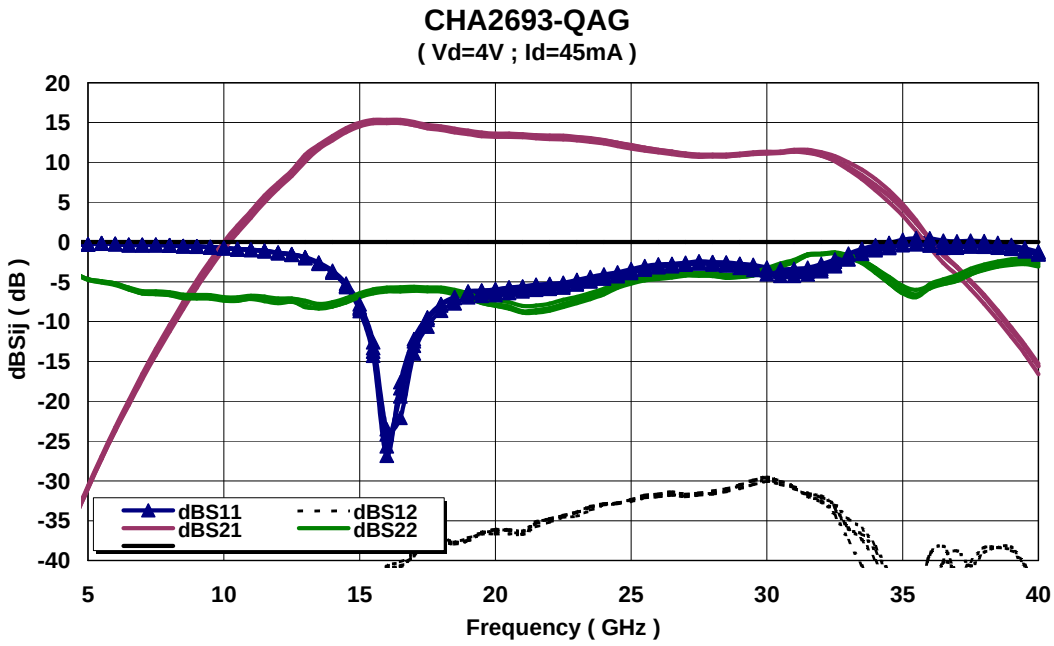
Schematic



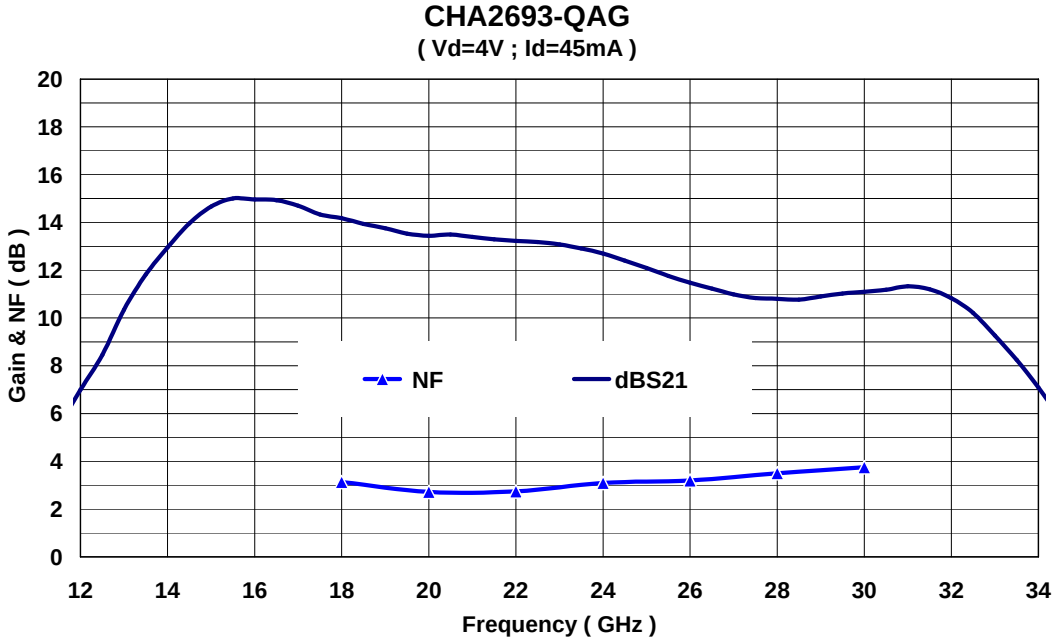
Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Typical PCB Measured Performance

Tamb = +25℃, Vd = +4.0V, Id = 45mA



Sij in the package access planes, using the proposed land pattern & board 95542
Refer to the “definition of the Sij reference planes” section below



Gain & NF in the board access planes, using the proposed land pattern & board 95542

Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Typical Package Sij parametres

Tamb = +25°C, Vd = +4.0V, Id = 45mA

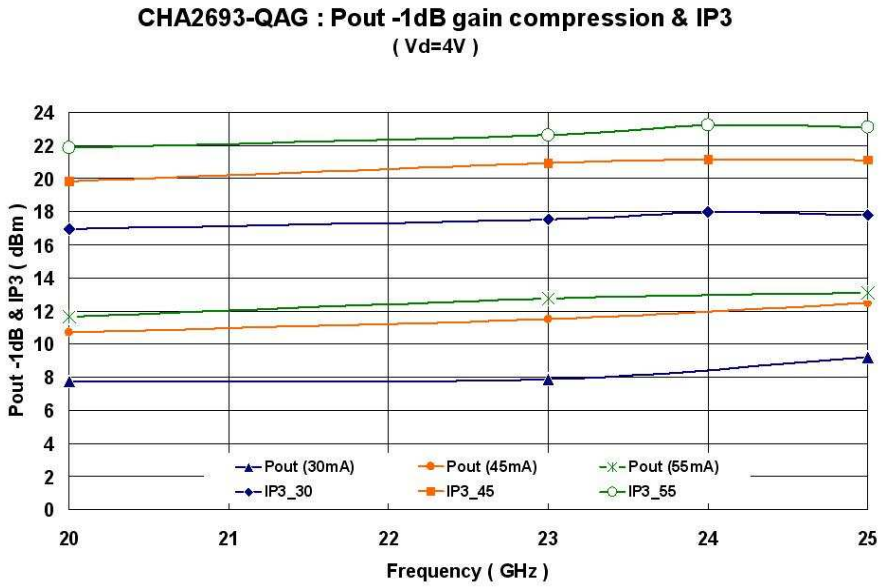
Freq (GHz)	S11	S11	S12	S12	S21	S21	S22	PS22
	dB	/°	dB	/°	dB	/°	dB	/°
1	-0.1	-73.4	-71.6	150.8	-32.8	101.4	-0.4	-47.4
2	-0.1	-129.6	-65.3	170.7	-35.4	10.7	-1.3	-90.2
3	-0.3	-172.7	-57.5	108.1	-47.5	-3.8	-2.6	-128.2
4	-0.1	151.5	-53.7	85.5	-39.7	115.6	-3.4	-163.7
5	-0.3	118.7	-53.0	48.0	-30.8	112.6	-4.8	163.2
6	-0.3	88.8	-51.3	30.0	-23.5	103.7	-5.4	130.4
7	-0.4	60.0	-51.2	9.1	-16.8	86.9	-6.5	98.1
8	-0.5	34.7	-53.5	-11.6	-10.8	62.4	-6.7	68.7
9	-0.6	10.1	-51.8	-21.1	-5.3	32.0	-6.9	41.1
10	-0.8	-11.3	-53.6	-29.2	-0.5	-2.4	-7.1	19.1
11	-1.0	-32.0	-51.4	-60.1	3.4	-39.8	-6.9	0.4
12	-1.4	-52.2	-54.6	-112.9	7.0	-79.5	-7.3	-13.7
13	-2.0	-75.6	-52.5	132.9	10.4	-117.3	-7.5	-31.2
14	-3.8	-102.2	-47.7	65.0	13.0	-165.2	-7.7	-33.4
15	-8.7	-132.8	-43.0	10.8	14.7	146.6	-6.6	-42.6
16	-26.9	-101.3	-41.3	-26.3	15.0	99.2	-5.9	-56.9
17	-12.2	-35.1	-39.3	-58.9	14.7	56.8	-5.9	-71.2
18	-7.8	-56.8	-37.5	-100.9	14.2	20.1	-6.1	-85.7
19	-6.4	-80.4	-37.5	-127.7	13.8	-14.2	-7.0	-101.1
20	-6.2	-97.9	-36.4	-159.5	13.4	-46.3	-8.0	-112.9
21	-5.9	-114.8	-36.7	178.9	13.4	-79.4	-8.9	-118.0
22	-5.7	-126.7	-34.8	154.9	13.2	-111.9	-8.6	-123.3
23	-5.2	-138.7	-33.9	129.2	13.1	-145.3	-7.7	-126.8
24	-4.5	-149.9	-32.9	103.8	12.7	-178.6	-6.6	-136.9
25	-3.7	-161.6	-32.4	81.1	12.1	149.1	-5.2	-148.2
26	-3.1	-173.5	-31.9	55.2	11.5	118.7	-4.7	-162.0
27	-2.7	174.4	-31.9	33.6	11.0	89.2	-4.2	-174.9
28	-2.6	164.9	-31.7	14.2	10.8	60.4	-4.3	175.6
29	-2.7	157.9	-31.0	-6.7	10.9	29.8	-4.4	170.2
30	-3.2	152.5	-30.1	-36.1	11.1	-4.6	-3.7	169.4
31	-3.4	154.1	-31.0	-71.0	11.3	-42.3	-2.6	163.4
32	-2.8	155.8	-32.7	-102.3	10.8	-85.4	-1.5	149.3
33	-1.5	152.8	-35.9	-145.0	9.3	-130.0	-1.7	133.7
34	-0.4	146.6	-40.0	168.3	7.1	-172.0	-3.3	118.9
35	-0.3	135.6	-46.7	113.9	4.2	146.5	-5.9	118.3
36	-0.1	123.6	-49.9	115.0	0.4	109.8	-5.8	134.0
37	0.0	113.7	-38.8	21.9	-3.1	79.9	-4.6	129.1
38	-0.1	101.3	-39.0	4.5	-6.7	48.6	-3.3	124.7
39	-0.4	87.1	-38.3	-35.0	-10.7	18.7	-2.5	109.7
40	-1.2	71.4	-41.9	-59.1	-15.3	-7.7	-2.7	91.7

Refer to the “definition of the Sij reference planes” section below.

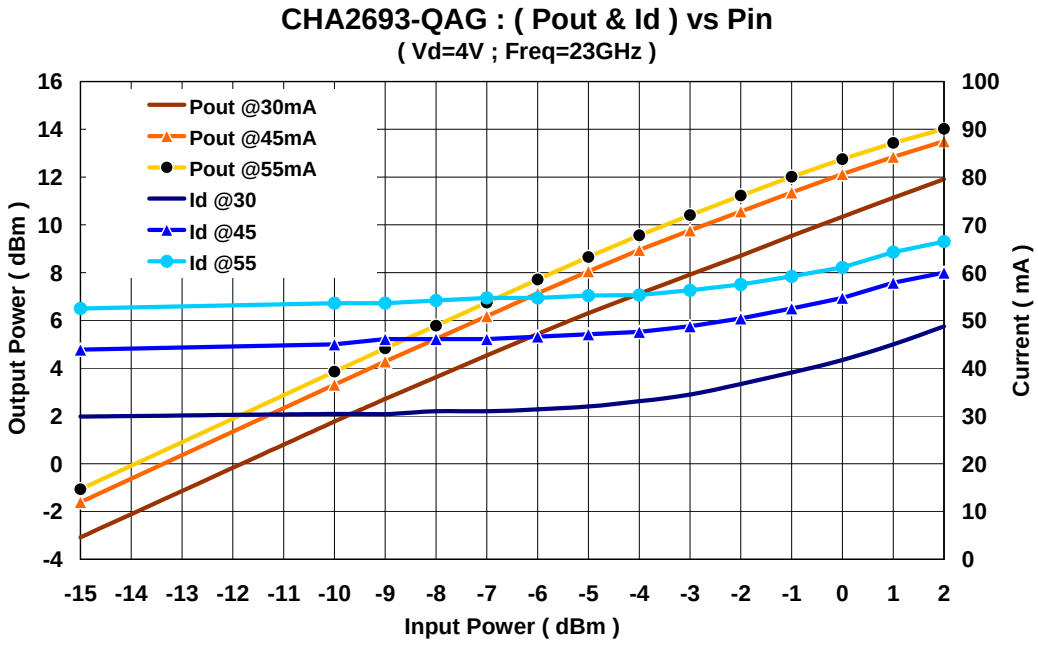
Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Typical PCB Measured Performance

Tamb = +25°C, Vd = +4.0V, Id = 30, 45 & 55mA



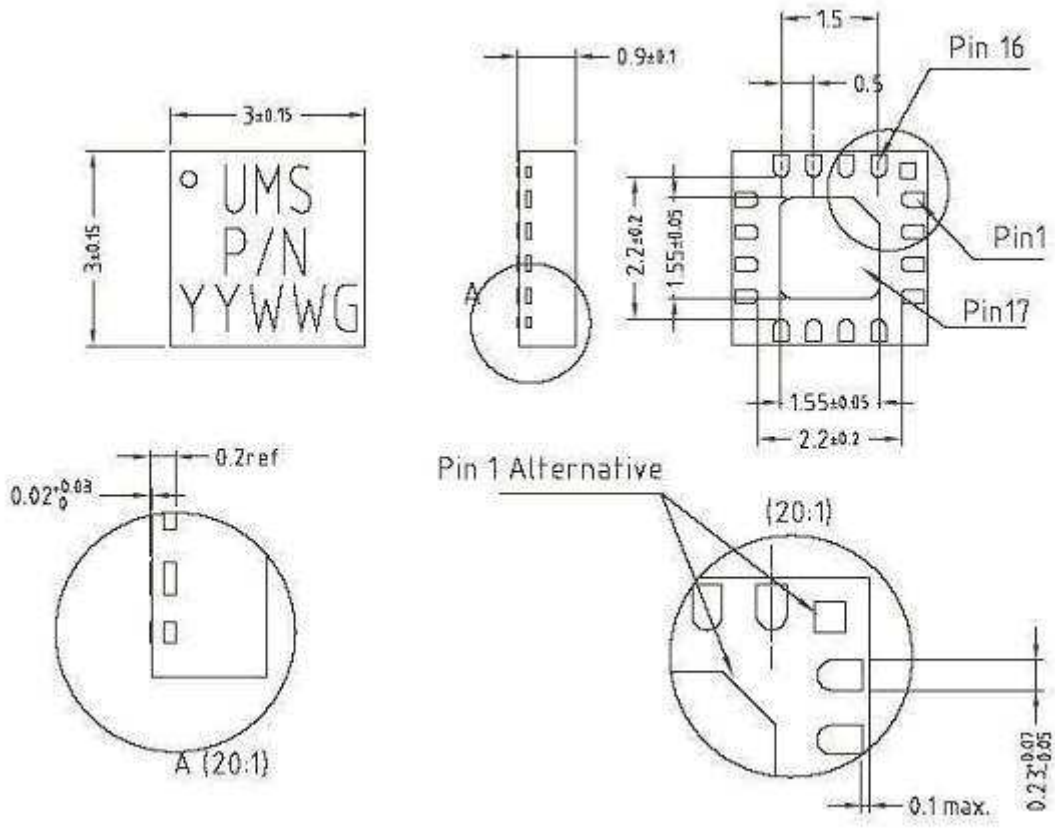
Pout –1dB & OIP3 in the in the board access planes, using the proposed land pattern & board 95542



Pin vs Pout & Id at 23GHz, in the board access planes, using the proposed land pattern & board 95542

Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Package outline:



Matt tin, Lead Free	(Green)
Units	mm
From the standard	JEDEC MO-220

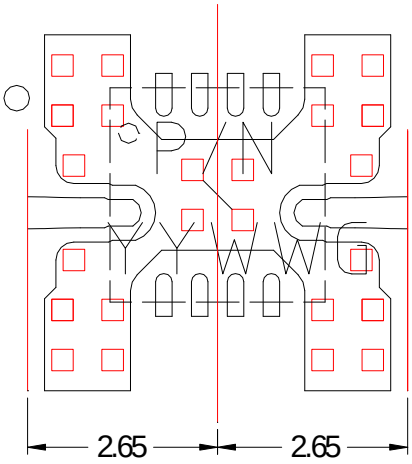
17- GND

1-	NC	9-	GND
2-	GND	10-	RF OUT
3-	RF IN	11-	GND
4-	GND	12-	NC
5-	NC	13-	NC
6-	VG1	14-	VD
7-	VG2	15-	NC
8-	NC	16-	NC

Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Definition of the Sij reference planes

The reference planes are defined from the footprint of the recommended characterization board shown below under the number 95542.
The reference is the symmetrical axis of the package. The input and output reference planes are located at 2.65mm offset (input wise and output wise respec.) from this axis. Then, the given Sij incorporates this land pattern.



Application note

The design of the motherboard has a strong impact on the over all performance since the transition from the motherboard to the package is comparably large. In case of the SMD type packages of United Monolithic Semiconductors the motherboard should be designed according to the information given in the following to achieve good performance. Other configurations are also possible but can lead to different results. If you need advise please contact United Monolithic Semiconductors for further information.

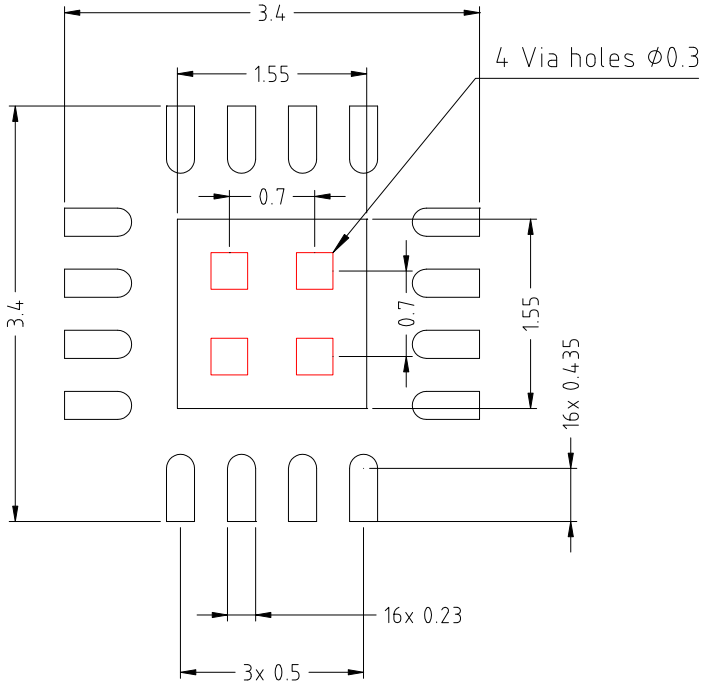
SMD type packages of UMS should allow design and fabrication of micro- and mm-wave modules at low cost. Therefore, a suitable motherboard environment has been chosen. All tests and verifications have been performed on Rogers RO4003. This material exhibits a permittivity of 3.38 and has been used with a thickness of 200µm [8 mils] and a 1/2oz or less copper cladding. The corresponding 50Ohm transmission line has a strip width of about 460µm [approx. 18 mils].

The contact areas on the motherboard for the package connections should be designed according to the footprint given above. The proper via structure under the ground pad is very important in order to achieve a good RF and lifetime performance. All tests have been done by using a grid of plenty plated through vias with a diameter of less than 300µm [12 mils] and a spacing of less than 700µm [28 mils] from the centres of two adjacent vias. The via grid should cover the whole space under the ground pad and the vias closest to the RF ports should be located near the edge of the pad to allow a good RF ground connection. Since the vias are important for heat transfer, a proper via filling should be guaranteed during the mounting procedure to get a low thermal resistance between package and heat sink. For power devices the use of heat slugs in the motherboard instead of a grid of via's is recommended.

For the mounting process the SMD type package can be handled as a standard surface mount component. The use of either solder or conductive epoxy is possible. The solder thickness after reflow should be typical 50µm [2 mils] and the lateral alignment between the package and the motherboard should be within 50µm [2 mils]. Caution should be taken to obtain a good and reliable

Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

contact over the whole pad areas. Voids or other improper connections, in particular, between the ground pads of motherboard and package will lead to a deterioration of the RF performance and the heat dissipation. The latter effect can reduce drastically reliability and lifetime of the product.



(For production, design must be adapted with regard to PCB tolerances and assembly process)

Basic footprint for a 16L-QFN3x3 (all units mm)
(Please, refer to the UMS propose footprint for optimum operation in the following “Proposed Assembly board” section)

The RF ports are DC blocked on chip. The DC connection (Vd) does not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

SMD mounting procedure

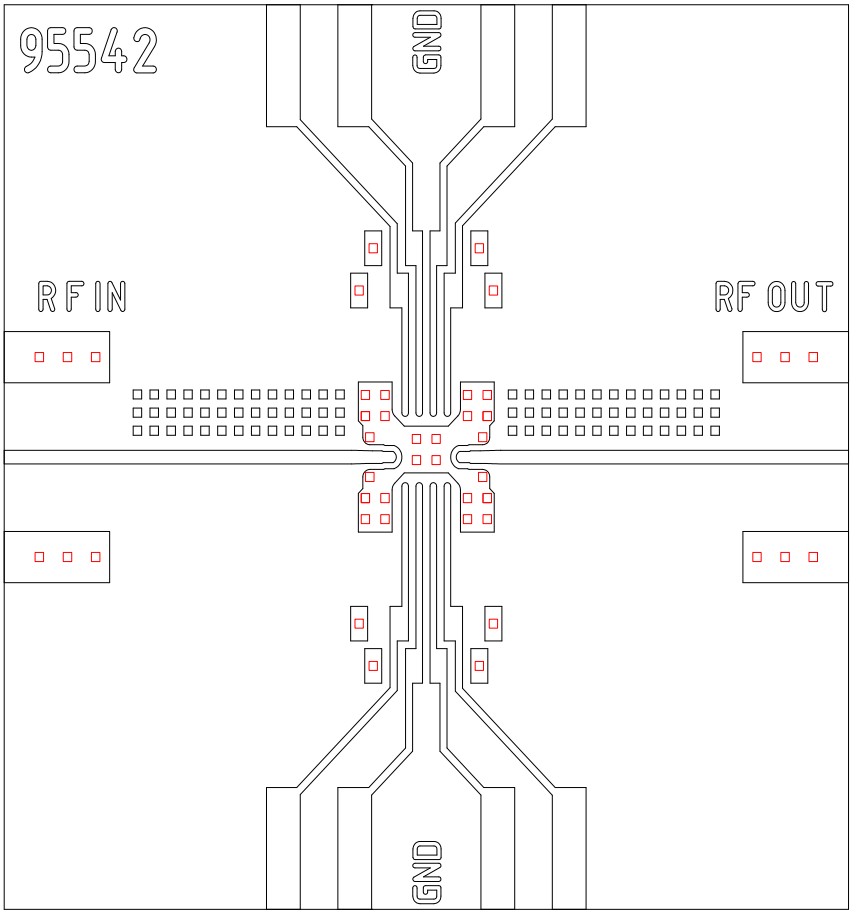
The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Proposed Assembly board for the 16L-QFN3x3 products characterization.

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.

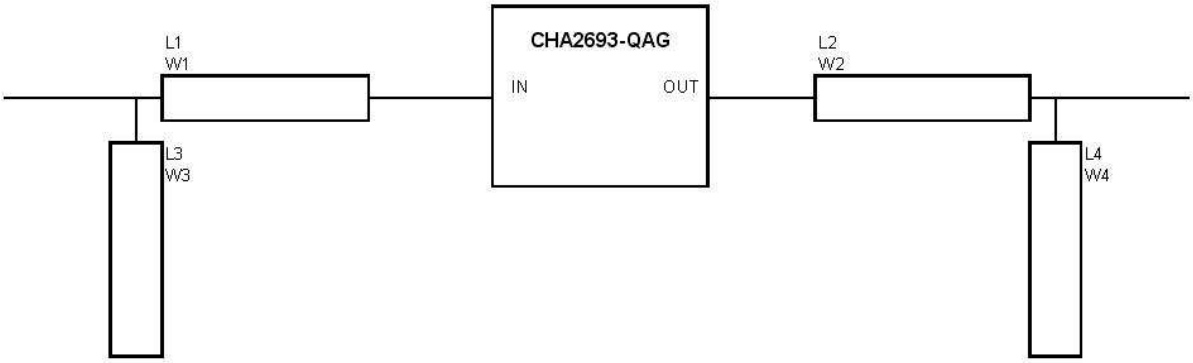


Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Proposed external on-board matching.

- The performances of this product might be enhanced using external matching components such as very simple combination of micro-strip stubs and slugs.
- The schematic shown below help to define the board dedicated to the typical sub-band in the range 18 to 30GHz.
- Based on the Sij matrix given previously, more accurate, or dedicated frequency boards may be derived.

Typical laminated substrate	
Epsilon relative	3.38
Thickness (µm)	200



	All in µm								
Freq (GHz)	L1	W1	L2	W2	L3	W3	L4	W4	Rloss (dB)
17.0-20.0	935	100	805	100	610	470	435	470	-10
21.0-24.0	555	100	455	100	980	470	415	470	-10
24.5-26.5	290	100	320	100	1025	470	770	470	-10
27.5-29.5	145	100	180	100	955	470	910	470	-10
29.5-30.0	95	100	135	100	945	470	935	470	-10
20.0-28.0	325	100	250	100	810	470	660	470	-10

Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Ordering Information

QFN 3x3 RoHS compliant package: CHA2693-QAG/XY
Stick: XY = 20 Tape & reel: XY = 21

Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09