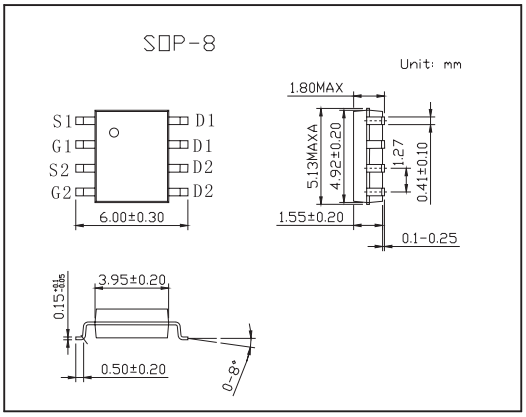
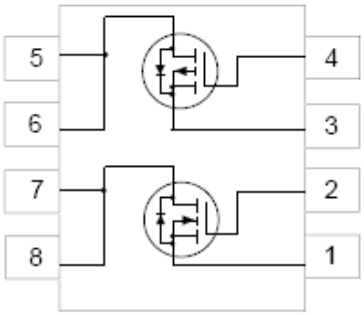
Dual N & P-Channel Enhancement Mode Field Effect Transistor KDS8928A

Features

- N-Channel
  5.5 A, 30 V $R_{DS(ON)}$ = 0.030 Ω @ V_{GS} = 4.5V
  $R_{DS(ON)}$ = 0.038 Ω @ V_{GS} =2.5V
- P-Channel
  -4 A, -20 V $R_{DS(ON)}$ = 0.055 Ω @ V_{GS} =- 4.5 V
  $R_{DS(ON)}$ = 0.070 Ω @ V_{GS} =-2.5V
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and handling capability in a widely used surface mount package
- Dual (N & P-Channel) MOSFET in surface mount package.





Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	N-Channel	P- Channel	Unit
Drain to Source Voltage	V_{DSS}	30	30	V
Gate to Source Voltage	V_{GS}	8	-8	V
Drain Current Continuous (Note 1a)	I_D	5.5	-4	A
Drain Current Pulsed		20	-20	A
Power Dissipation for Single Operation	P_D	2		W
Power Dissipation for Single Operation (Note 1a)	P_D	1.6		W
(Note 1b)		1		
(Note 1c)		0.9		
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150		℃
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	78		℃/W
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	40		℃/W

KDS8928A

■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	B_{VDSS}	V_{GS} = 0 V, I_D = 250 μA	N-Ch	30			V
		V_{GS} = 0 V, I_D = -250 μA	P-Ch	-20			
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃	N-Ch		32		mV/℃
		I_D = -250 μA, Referenced to 25℃	P-Ch		-23		
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24V, V_{GS} = 0 V	N-Ch			1	μA
		V_{DS} = -16 V, V_{GS} = 0 V	P-Ch			-1	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±8V, V_{DS} = 0 V	N-Ch			±100	nA
		V_{GS} = ±8 V, V_{DS} = 0 V	P-Ch			±100	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	N-Ch	0.4	0.67		V
		V_{DS} = V_{GS}, I_D = -250 μA	P-Ch	-0.4	-0.6		
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃	N-Ch		-3		mV/℃
		I_D = -250 μA, Referenced to 25℃	P-Ch		4		
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D =5.5A	N-Ch		0.025	0.03	mΩ
		V_{GS} = 2.5 V, I_D = 4.5A			0.031	0.038	
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -4.5 V, I_D =-4 A	P-Ch		0.043	0.055	
		V_{GS} = -2.5 V, I_D =-3.4 A			.059	0.072	
On-State Drain Current	$I_{D(on)}$	V_{GS} = 4.5 V, V_{DS} = 5V	N-Ch	20			A
		V_{GS} = -4.5 V, V_{DS} = -5V	P-Ch	-20			
Forward Transconductance	g_{FS}	V_{DS} = 5V, I_D = 5.5A	N-Ch		20		S
		V_{DS} = -5V, I_D = -4A	P-Ch		13		
Input Capacitance	C_{iss}	N-Channel	N-Ch		900		pF
		V_{DS} = 10 V, V_{GS} = 0 V,f = 1.0 MHz	P-Ch		1130		
Output Capacitance	C_{oss}		N-Ch		410		pF
		P-Channel	P-Ch		480		
Reverse Transfer Capacitance	C_{rss}	V_{DS} = -10 V, V_{GS} = 0 V,f = 1.0 MHz	N-Ch		110		pF
			P-Ch		120		
Turn-On Delay Time	$t_{d(on)}$	N-Channel	N-Ch		6	12	ns
		V_{DD} = 6 V, I_D = 1 A,	P-Ch		8	16	
Turn-On Rise Time	tr	V_{GS} = 4.5 V, R_{GEN} = 6 Ω (Note 2)	N-Ch		19	31	ns
			P-Ch		23	37	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel	N-Ch		42	67	ns
		V_{DD} = -10 V, I_D = -1 A,	P-Ch		260	360	
Turn-Off Fall Time	t_f	V_{GS} = -4.5 V, R_{GEN} = 6 Ω (Note 2)	N-Ch		13	24	ns
			P-Ch		90	125	
Total Gate Charge	Q_g	N-Channel	N-Ch		19.8	28	nC
		V_{DS} =10V,I_D=5.5A,V_{GS}=4.5V(Note 2)	P-Ch		20	28	
Gate-Source Charge	Q_{gs}		N-Ch		2		nC
		P-Channel	P-Ch		2.8		
Gate-Drain Charge	Q_{gd}	V_{DS}=-5V,I_D=-4A,V_{GS}=-5V(Note 2)	N-Ch		6.3		nC
			P-Ch		3.2		

KDS8928A

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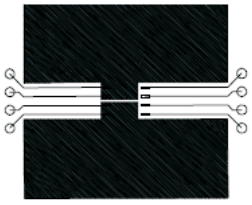
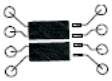
Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Maximum Continuous Drain-Source Diode Forward Current	Is		N-Ch			1.3	A
			P-Ch			-1.3	
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, Is = 1.3A (Not 2)	N-Ch		0.68	1.2	V
		V_{GS} = 0 V, Is = -1.3A (Not 2)	P-Ch		-0.7	-1.2	

Notes:

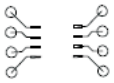
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 78°C/W on a 0.5 in² pad of 2oz copper.



b. 125°C/W on a 0.02 in² pad of 2oz copper.



c. 135°C/W on a 0.003 in² pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%..