Data Sheet November 6, 2008 FN6809.0

# Two-Phase Buck PWM Controller with Integrated MOSFET Drivers for Intel VR11 and AMD Applications

The ISL6313B two-phase PWM control IC provides a precision voltage regulation system for advanced microprocessors. The integration of power MOSFET drivers into the controller IC marks a departure from the separate PWM controller and driver configuration of previous multi-phase product families. By reducing the number of external parts, this integration is optimized for a cost and space saving power management solution.

One outstanding feature of this controller IC is its multiprocessor compatibility, allowing it to work with both Intel and AMD microprocessors. Included are programmable VID codes for Intel VR11 as well as AMD 5-bit and 6-bit DAC tables. A circuit is provided for remote voltage sensing, compensating for any potential difference between remote and local grounds. The output voltage can also be positively or negatively offset through the use of a single external resistor.

The ISL6313B also includes advanced control loop features for optimal transient response to load apply and removal. One of these features is highly accurate, fully differential, continuous DCR current sensing for load line programming and channel current balance. Active Pulse Positioning (APP) Modulation and Adaptive Phase Alignment (APA) are two other unique features, allowing for quicker initial response to high di/dt load transients. With this quicker initial response to load transients, the number of output bulk capacitors can be reduced, helping to reduce cost.

Integrated into the ISL6313B are user programmable current sense resistors, which require only a single external resistor to set their values. No external current sense resistors are required. Another unique feature of the ISL6313B is the addition of a dynamic VID compensation pin that allows optimizing compensation to be added for well controlled dynamic VID response.

Protection features of this controller IC include a set of sophisticated overvoltage, undervoltage, and overcurrent protection. Furthermore, the ISL6313B includes protection against an open circuit on the remote sensing inputs. Combined, these features provide advanced protection for the microprocessor and power system.

## Features

- Integrated Multi-Phase Power Conversion
  - 2-Phase or 1-Phase Operation with Internal Drivers
- Precision Core Voltage Regulation
  - Differential Remote Voltage Sensing
  - ±0.5% System Accuracy Over Temperature
  - Adjustable Reference-Voltage Offset
- Optimal Transient Response
  - Active Pulse Positioning (APP) Modulation
  - Adaptive Phase Alignment (APA)
- Fully Differential, Continuous DCR Current Sensing
  - Integrated Programmable Current Sense Resistors
  - Accurate Load Line Programming
  - Precision Channel Current Balancing
- Variable Gate Drive Bias: 5V to 12V
- Multi-Processor Compatible
  - Intel VR11 Mode of Operation
  - AMD Mode of Operation
- Microprocessor Voltage Identification Inputs
  - 8-Bit DAC
  - Selectable between Intel VR11, AMD 5-bit, and AMD 6-bit DAC tables
  - Dynamic VID Technology
- Dynamic VID Compensation
- Overcurrent Protection
- Multi-tiered Overvoltage Protection
- Digital Soft-Start
- Selectable Operation Frequency up to 1.5MHz Per Phase
- Pb-Free (RoHS Compliant)

## Ordering Information

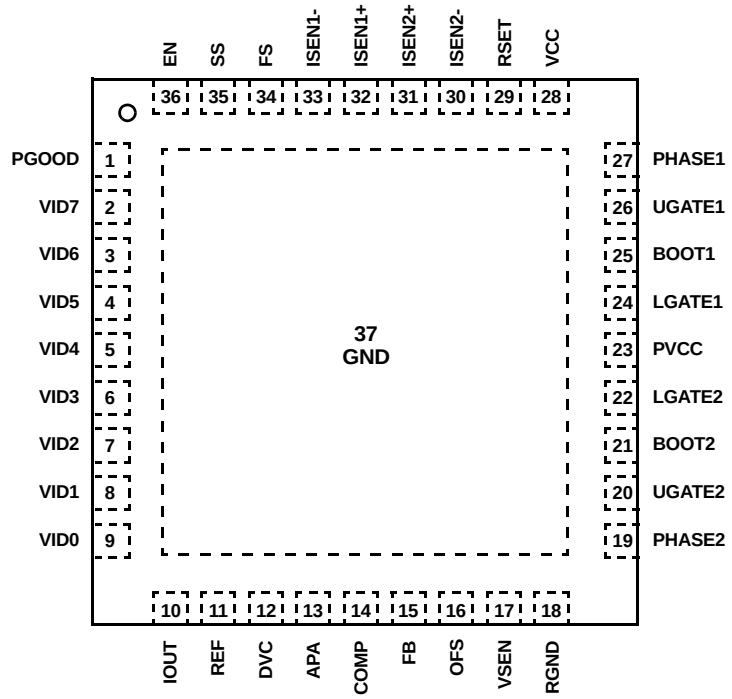
| PART NUMBER (Note) | PART MARKING | TEMP. RANGE (°C) | PACKAGE (Pb-free) | PKG. DWG. # |
|---|---|---|---|---|
| ISL6313BCRZ* | 6313B CRZ | 0 to +70 | 36 Ld 6x6 TQFN | L36.6x6 |
| ISL6313BIRZ* | 6313B IRZ | -40 to +85 | 36 Ld 6x6 TQFN | L36.6x6 |

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

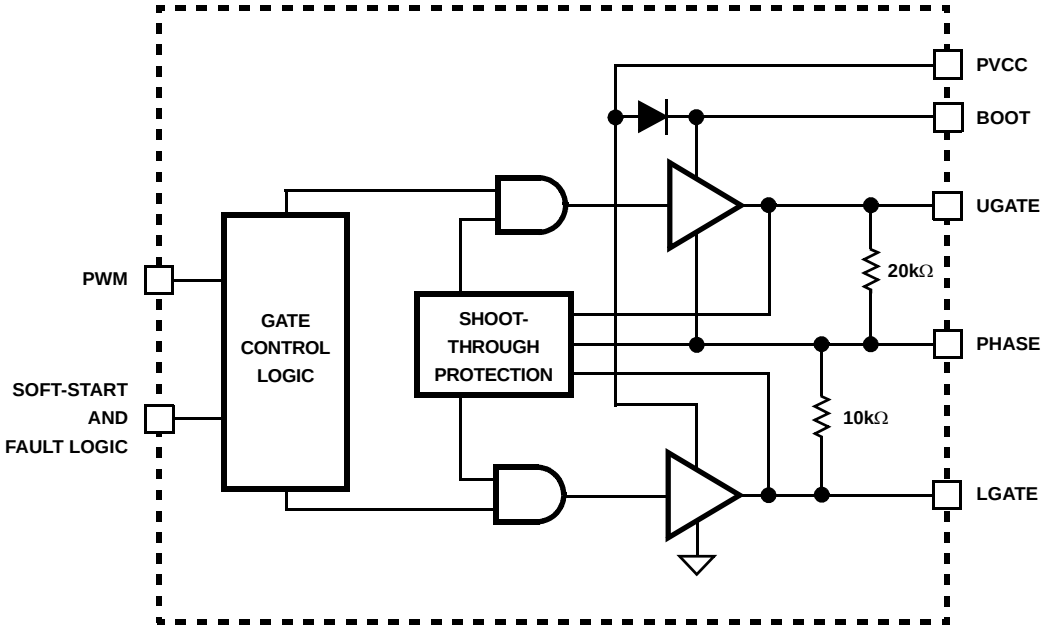
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Pinout

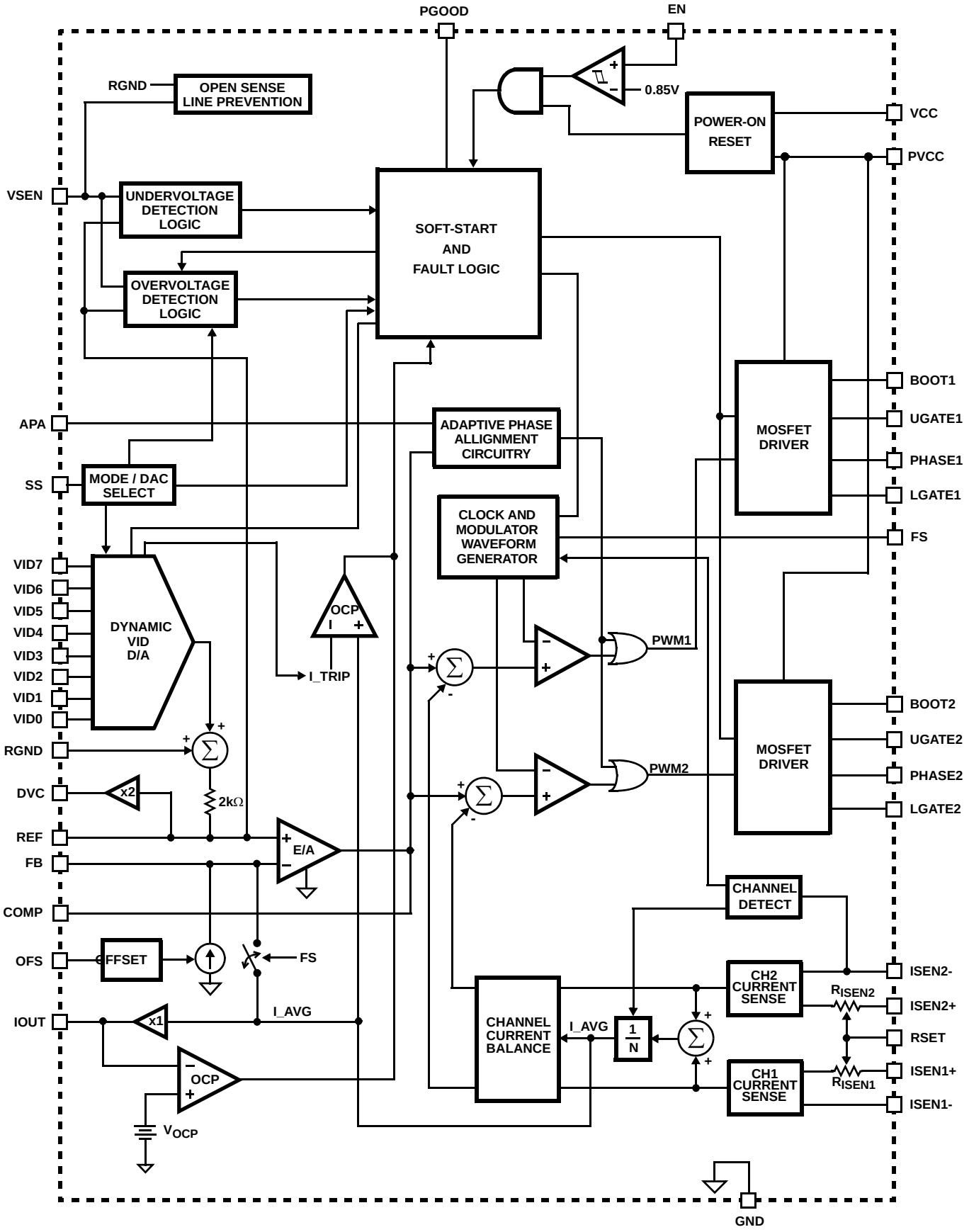
**ISL6313B**
**(36 LD TQFN)**
TOP VIEW



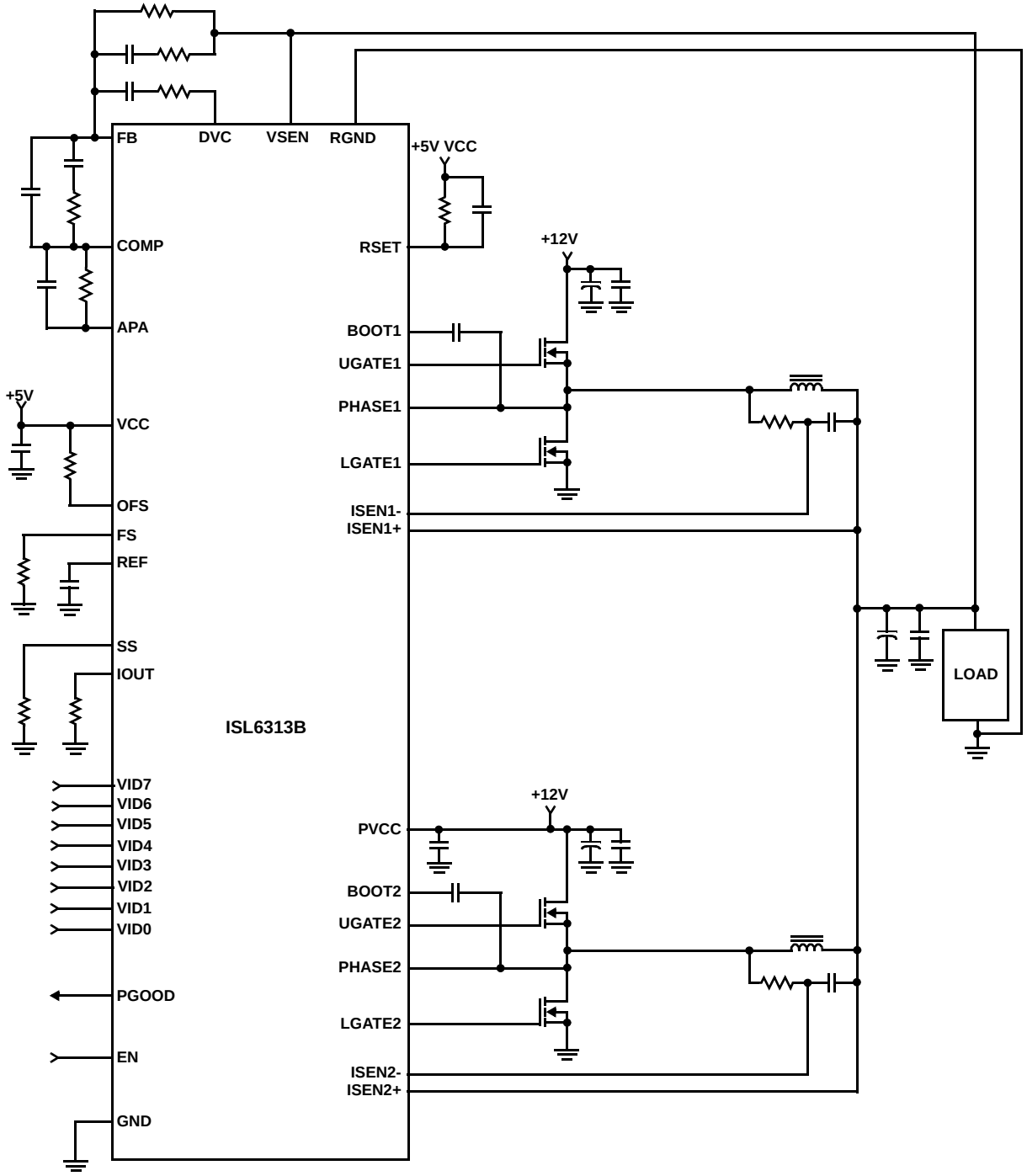

## ISL6313B Integrated Driver Block Diagram



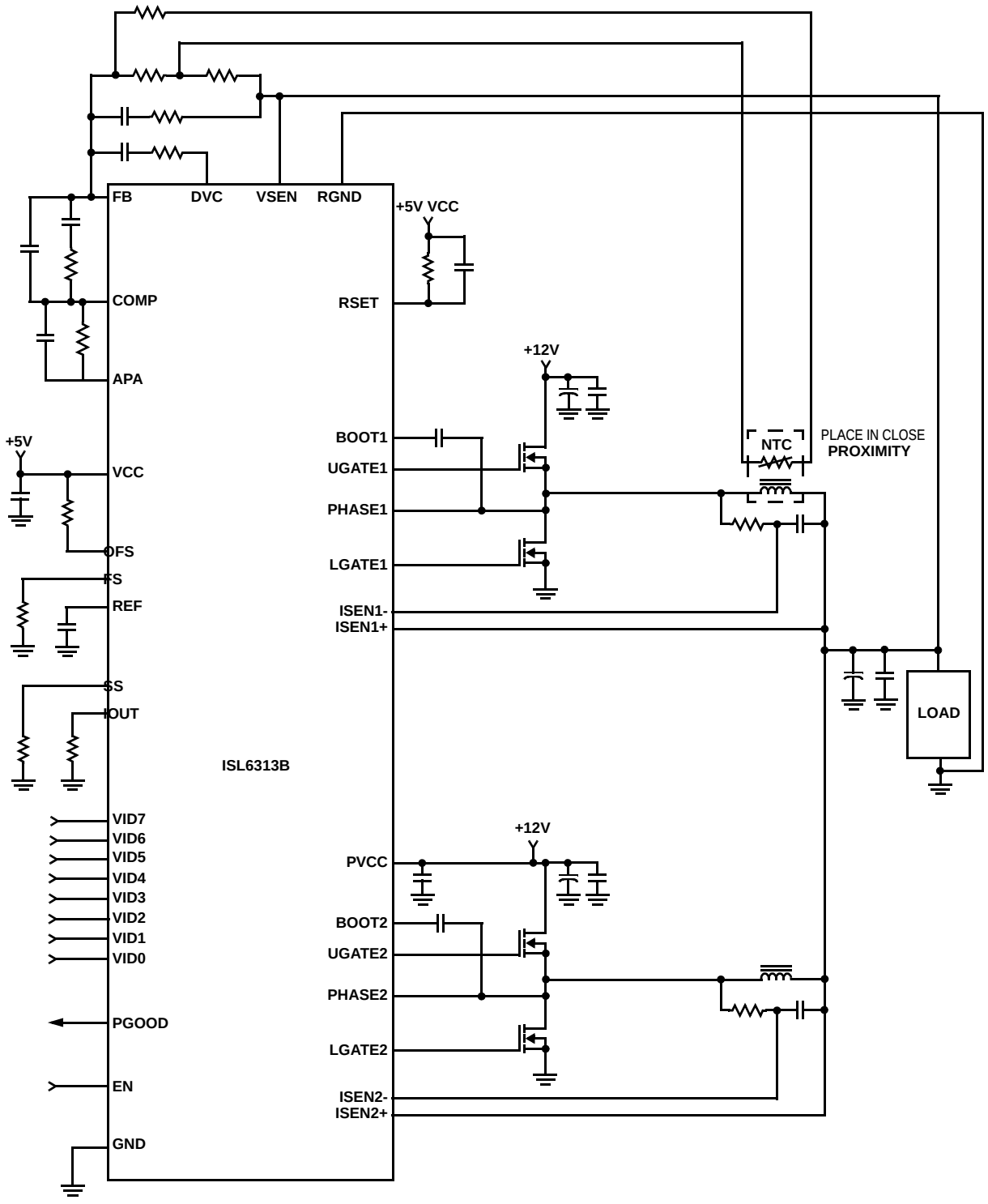
## Block Diagram



## Typical Application - ISL6313B



## Typical Application - ISL6313B with NTC Thermal Compensation



## Absolute Maximum Ratings

Supply Voltage, VCC . . . . . -0.3V to +6V
Supply Voltage, PVCC . . . . . -0.3V to +15V
BOOT Voltage, $V_{BOOT}$ . . . . . GND - 0.3V to GND + 36V
BOOT to PHASE Voltage, $V_{BOOT-PHASE}$ . . . . . -0.3V to 15V (DC)
-0.3V to 16V (<10ns, 10µJ)
PHASE Voltage, $V_{PHASE}$ . . . . . GND - 0.3V to 15V (PVCC = 12)
GND - 8V (<400ns, 20µJ) to 24V (<200ns, $V_{BOOT - PHASE}$ = 12V)
UGATE Voltage, $V_{UGATE}$. . . . . $V_{PHASE}$ - 0.3V to $V_{BOOT}$ + 0.3V
$V_{PHASE}$ - 3.5V (<100ns Pulse Width, 2µJ) to $V_{BOOT}$ + 0.3V
LGATE Voltage, $V_{LGATE}$ . . . . . GND - 0.3V to PVCC + 0.3V
GND - 5V (<100ns Pulse Width, 2µJ) to PVCC + 0.3V
Input, Output, or I/O Voltage . . . . . GND - 0.3V to VCC + 0.3V

## Thermal Information

| Thermal Resistance | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| TQFN Package (Notes 1, 2) . . . . . | 32 | 2.0 |

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## Recommended Operating Conditions

VCC Supply Voltage . . . . . +5V ±5%
PVCC Supply Voltage . . . . . +5V to 12V ±5%
Ambient Temperature
ISL6313BCRZ . . . . . 0°C to +70°C
ISL6313BIRZ . . . . . -40°C to +85°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

1. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For $\theta_{JC}$, the “case temp” location is the center of the exposed metal pad on the package underside.
3. Limits established by characterization and are not production tested.

## Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **BIAS SUPPLIES** | | | | | |
| Input Bias Supply Current | $I_{VCC}$; EN = high | 10 | 14 | 17 | mA |
| Gate Drive Bias Current - PVCC Pin | $I_{PVCC}$; EN = high | 2 | 4.2 | 6 | mA |
| VCC POR (Power-On Reset) Threshold | VCC rising | 4.25 | 4.38 | 4.50 | V |
| | VCC falling | 3.75 | 3.87 | 4.00 | V |
| PVCC POR (Power-On Reset) Threshold | PVCC rising | 4.25 | 4.38 | 4.50 | V |
| | PVCC falling | 3.75 | 3.87 | 4.00 | V |
| **PWM MODULATOR** | | | | | |
| Oscillator Frequency Accuracy, $F_{SW}$ (ISL6313BCRZ) | $R_T$ = 100kΩ (±0.1%) | 225 | 250 | 275 | kHz |
| Oscillator Frequency Accuracy, $F_{SW}$ (ISL6313BIRZ) | $R_T$ = 100kΩ (±0.1%) | 215 | 250 | 280 | kHz |
| Adjustment Range of Switching Frequency | (Note 3) | 0.08 | - | 1.0 | MHz |
| Oscillator Ramp Amplitude, $V_{P-P}$ | (Note 3) | - | 1.50 | - | V |
| **CONTROL THRESHOLDS** | | | | | |
| EN Rising Threshold | | 0.84 | 0.85 | 0.88 | V |
| EN Hysteresis | | - | 100 | - | mV |
| **REFERENCE AND DAC** | | | | | |
| System Accuracy (1.000V to 1.600V) | | -0.5 | - | 0.5 | % |
| System Accuracy (0.600V to 1.000V) | | -1.0 | - | 1.0 | % |
| System Accuracy (0.375V to 0.600V) | | -2.0 | - | 2.0 | % |
| DAC Input Low Voltage (INTEL) | | - | - | 0.4 | V |

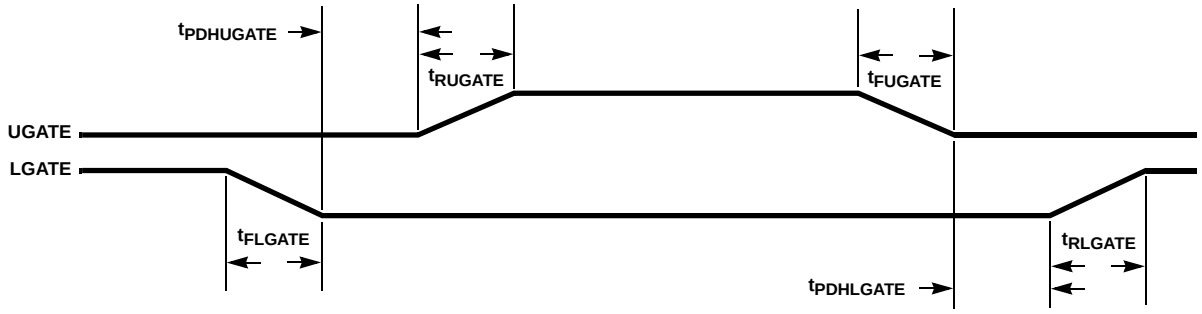
**Electrical Specifications** Recommended Operating Conditions, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| DAC Input High Voltage (INTEL) | | 0.8 | - | - | V |
| DAC Input Low Voltage (AMD) | | - | - | 0.8 | V |
| DAC Input High Voltage (AMD) | | 1.4 | - | - | V |
| **PIN-ADJUSTABLE OFFSET** | | | | | |
| OFS Sink Current Accuracy (Negative Offset) | $R_{OFS}$ = 32.4kΩ from OFS to VCC | 47.0 | 50.0 | 53.0 | µA |
| OFS Source Current Accuracy (Positive Offset) | $R_{OFS}$ = 6.04kΩ from OFS to GND | 47.0 | 50.0 | 53.0 | µA |
| **ERROR AMPLIFIER** | | | | | |
| DC Gain | $R_L$ = 10k to ground, (Note 3) | - | 96 | - | dB |
| Gain-Bandwidth Product | $C_L$ = 100pF, $R_L$ = 10k to ground, (Note 3) | - | 40 | - | MHz |
| Slew Rate | $C_L$ = 100pF, Load = ±400µA, (Note 3) | - | 20 | - | V/µs |
| Maximum Output Voltage | Load = 1mA | 3.90 | 4.20 | - | V |
| Minimum Output Voltage | Load = -1mA | - | 1.30 | 1.52 | V |
| **SOFT-START RAMP** | | | | | |
| Soft-Start Ramp Rate | $R_S$ = 100kΩ | - | 1.26 | - | mV/µs |
| Adjustment Range of Soft-Start Ramp Rate (Note 3) | | 0.156 | - | 6.25 | mV/µs |
| **CURRENT SENSING** | | | | | |
| IOUT Current Sense Offset | $R_{SET}$ = 40.2kΩ, $V_{ISEN1+}$ = $V_{ISEN2+}$ = 0V | -2.5 | 0 | 2.5 | µA |
| IOUT Current Sense Gain (ISL6313BCRZ) | $R_{SET}$ = 40.2kΩ, $V_{ISEN1}$ = $V_{ISEN2}$ = 24mV | 76 | 80 | 84 | µA |
| IOUT Current Sense Gain (ISL6313BIRZ) | $R_{SET}$ = 40.2kΩ, $V_{ISEN1}$ = $V_{ISEN2}$ = 24mV | 73 | 80 | 84 | µA |
| **OVERCURRENT PROTECTION** | | | | | |
| Overcurrent Trip Level - Average Channel | Normal operation (ISL6313BCRZ) | 88 | 100 | 112 | µA |
| | Normal operation (ISL6313BIRZ) | 82 | 100 | 118 | µA |
| | Dynamic VID change | 114 | 140 | 166 | µA |
| Overcurrent Trip Level - Individual Channel | Normal operation | 114 | 140 | 166 | µA |
| | Dynamic VID change | 166 | 196 | 226 | µA |
| IOUT Pin Overcurrent Trip Level | | 1.97 | 2.02 | 2.07 | V |
| **PROTECTION** | | | | | |
| Undervoltage Threshold | VSEN falling | VDAC - 325mV | VDAC - 350mV | VDAC - 375mV | V |
| Undervoltage Hysteresis | VSEN rising | 85 | 100 | 125 | mV |
| Overvoltage Threshold During Soft-Start | VR11 and AMD | 1.220 | 1.260 | 1.300 | V |
| Overvoltage Threshold | VR11, VSEN rising | VDAC + 150mV | VDAC + 175mV | VDAC + 200mV | V |
| | AMD, VSEN rising | VDAC + 200mV | VDAC + 225mV | VDAC + 250mV | V |
| Overvoltage Hysteresis | VSEN falling | - | 100 | - | mV |

**Electrical Specifications** Recommended Operating Conditions, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **SWITCHING TIME (Note 3)** | | | | | |
| UGATE Rise Time | $t_{RUGATE}$; $V_{PVCC}$ = 12V, 3nF load, 10% to 90% | - | 26 | - | ns |
| LGATE Rise Time | $t_{RLGATE}$; $V_{PVCC}$ = 12V, 3nF load, 10% to 90% | - | 18 | - | ns |
| UGATE Fall Time | $t_{FUGATE}$; $V_{PVCC}$ = 12V, 3nF load, 90% to 10% | - | 18 | - | ns |
| LGATE Fall Time | $t_{FLGATE}$; $V_{PVCC}$ = 12V, 3nF load, 90% to 10% | - | 12 | - | ns |
| UGATE Turn-On Non-Overlap | $t_{PDHUGATE}$; $V_{PVCC}$ = 12V, 3nF load, adaptive | - | 10 | - | ns |
| LGATE Turn-On Non-Overlap | $t_{PDHLGATE}$; $V_{PVCC}$ = 12V, 3nF load, adaptive | - | 10 | - | ns |
| **GATE DRIVE RESISTANCE (Note 3)** | | | | | |
| Upper Drive Source Resistance | $V_{PVCC}$ = 12V, 15mA source current | 1.25 | 2.0 | 3.0 | Ω |
| Upper Drive Sink Resistance | $V_{PVCC}$ = 12V, 15mA sink current | 0.9 | 1.65 | 3.0 | Ω |
| Lower Drive Source Resistance | $V_{PVCC}$ = 12V, 15mA source current | 0.85 | 1.25 | 2.2 | Ω |
| Lower Drive Sink Resistance | $V_{PVCC}$ = 12V, 15mA sink current | 0.60 | 0.80 | 1.35 | Ω |
| **OVER-TEMPERATURE SHUTDOWN (Note 3)** | | | | | |
| Thermal Shutdown Setpoint | | - | 160 | - | °C |
| Thermal Recovery Setpoint | | - | 100 | - | °C |

## *Timing Diagram*



## Functional Pin Description

### VCC

VCC is the bias supply for the ICs small-signal circuitry. Connect this pin to a +5V supply and decouple using a quality 0.1µF ceramic capacitor.

### PVCC

This pin is the power supply pin for the channel MOSFET drivers, and can be connected to any voltage from +5V to +12V depending on the desired MOSFET gate-drive level. Decouple this pin with a quality 1.0µF ceramic capacitor.

### GND

GND is the bias and reference ground for the IC.

### EN

This pin is a threshold-sensitive (approximately 0.85V) enable input for the controller. Held low, this pin disables controller operation. Pulled high, the pin enables the controller for operation.

### FS

A resistor, $R_S$, tied to this pin sets the channel switching frequency of the controller. Refer to Equation 47 for proper resistor calculation.

The FS pin also controls whether the internal $I_{AVG}$ current is connected to the FB pin or not. Tieing the $R_S$ resistor to ground connects the $I_{AVG}$ current internally to the FB pin, allowing the converter to incorporate output voltage droop proportional to the output current. Tieing the $R_S$ resistor to VCC, disconnects the $I_{AVG}$ current internally from the FB pin.

### VID0, VID1, VID2, VID3, VID4, VID5, VID6, and VID7

These are the inputs for the internal DAC that provides the reference voltage for output regulation. These pins respond to TTL logic thresholds. These pins are internally pulled high, to approximately 1.2V, by 40µA internal current sources for Intel modes of operation, and pulled low by 20µA internal current sources for AMD modes of operation. The internal pull-up current decreases to 0 as the VID voltage approaches the internal pull-up voltage. All VID pins are compatible with external pull-up voltages not exceeding the IC's bias voltage (VCC).

### VSEN

This pin senses the microprocessor's CORE voltage. Connect this pin to the CORE voltage sense pin or point of the microprocessor.

### RGND

This pin senses the local ground voltage of the microprocessor and offsets the internal DAC by this sensed voltage. Connect this pin to the Ground sense pin or point of the microprocessor.

### FB and COMP

These pins are the internal error amplifier inverting input and output respectively. The FB pin, COMP pin, and the VSEN pins are tied together through external R-C networks to compensate the regulator.

### DVC

A series resistor and capacitor can be connected from the DVC pin to the FB pin to compensate and smooth dynamic VID transitions.

### IOUT

The IOUT pin is the average channel-current sense output. This pin is used as a load current indicator to monitor what the output load current is.

This pin can also be used to set the overcurrent protection trip level if it desired that a lower level be used then the internal trip point. Connecting this pin through a resistor to ground allows the controller to set the alternate overcurrent protection trip level.

### APA

This is the Adaptive Phase Alignment set pin. A 100µA current flows into the APA pin and by tieing a resistor from this pin to COMP the trip level for the Adaptive Phase Alignment circuitry can be set.

### REF

The REF input pin is the positive input of the error amplifier. It is internally connected to the DAC output through a 2kΩ resistor. A capacitor is used between the REF pin and ground to smooth the voltage transition during soft-start and Dynamic VID transitions. This pin can also be bypassed to RGND if desired.

### RSET

Connect this pin to VCC through a resistor to set the effective value of the internal $R_{ISEN}$ current sense resistors. It is recommended a 0.1µF ceramic capacitor be placed in parallel with this resistor for noise immunization.

### OFS

The OFS pin provides a means to program a dc current for generating an offset voltage across the resistor between FB and VSEN. The offset current is generated via an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFS pin should be left unconnected.

### ISEN1-, ISEN1+, ISEN2-, and ISEN2+

These pins are used for differentially sensing the corresponding channel output currents. The sensed currents are used for channel balancing, protection, and load line regulation.

Connect ISEN1- and ISEN2- to the node between the RC sense elements surrounding the inductor of their respective

channel. Tie the ISEN+ pins to the $V_{CORE}$ side of their corresponding channel's sense capacitor.

Tieing ISEN2- to VCC programs the part for single phase operation.

### UGATE1 and UGATE2

Connect these pins to the corresponding upper MOSFET gates. These pins are used to control the upper MOSFETs and are monitored for shoot-through prevention purposes.

### BOOT1 and BOOT2

These pins provide the bias voltage for the corresponding upper MOSFET drives. Connect these pins to appropriately chosen external bootstrap capacitors. Internal bootstrap diodes connected to the PVCC pin provides the necessary bootstrap charge.

### PHASE1 and PHASE2

Connect these pins to the sources of the corresponding upper MOSFETs. These pins are the return path for the upper MOSFET drives.

### LGATE1 and LGATE2

These pins are used to control the lower MOSFETs. Connect these pins to the corresponding lower MOSFETs' gates.

### SS

A resistor, $R_{SS}$, placed from SS to ground or VCC, will set the soft-start ramp slope. Refer to Equations 20 and 21 for proper resistor calculation.

The state of the SS pin also selects which of the available DAC tables will be used to decode the VID inputs and puts the controller into the corresponding mode of operation. For Intel VR11 mode of operation the $R_{SS}$ resistor should be tied to ground. AMD compliance is selected if the $R_{SS}$ resistor is tied to VCC.

### PGOOD

For Intel mode of operation, PGOOD indicates whether VSEN is within specified overvoltage and undervoltage limits after a fixed delay from the end of soft-start. If VSEN exceeds these limits, an overcurrent event occurs, or if the part is disabled, PGOOD is pulled low. PGOOD is always low prior to the end of soft-start.

For AMD modes of operation, PGOOD will always be high as long as VSEN is within the specified undervoltage/overvoltage window and soft-start has ended. PGOOD only goes low if VSEN is outside this window.

## Operation

### Multiphase Power Conversion

Microprocessor load current profiles have changed to the point that using single-phase regulators is no longer a viable solution. Designing a regulator that is cost-effective, thermally sound, and efficient has become a challenge that only multi-phase converters can accomplish. The ISL6313B controller helps simplify implementation by integrating vital functions and requiring minimal external components. The block diagram on page 3 provides a top level view of multi-phase power conversion using the ISL6313B controller.

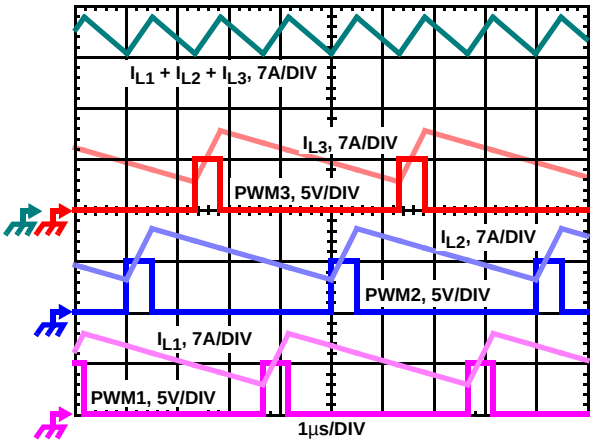



**FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER**

### Interleaving

The switching of each channel in a multi-phase converter is timed to be symmetrically out of phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the three-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 1 and 2). Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

Figure 1 illustrates the multiplicative effect on output ripple frequency. The three channel currents ($I_{L1}$, $I_{L2}$, and $I_{L3}$) combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The peak-to-peak current for each phase is about 7A, and the DC components of the inductor currents combine to feed the load.

To understand the reduction of ripple current amplitude in the multi-phase circuit, examine Equation 1 representing an individual channel peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{L \cdot f_S \cdot V_{IN}} \quad \text{(EQ. 1)}$$

In Equation 1, $V_{IN}$ and $V_{OUT}$ are the input and output voltages respectively, L is the single-channel inductor value, and $f_S$ is the switching frequency.

The output capacitors conduct the ripple component of the inductor current. In the case of multi-phase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{C(PP)} = \frac{(V_{IN} - N \cdot V_{OUT}) \cdot V_{OUT}}{L \cdot f_S \cdot V_{IN}} \quad \text{(EQ. 2)}$$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multiphase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 2 illustrates input currents from a three-phase converter combining to reduce the total input ripple current.

The converter depicted in Figure 2 delivers 1.5V to a 36A load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has $11.9A_{RMS}$ input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

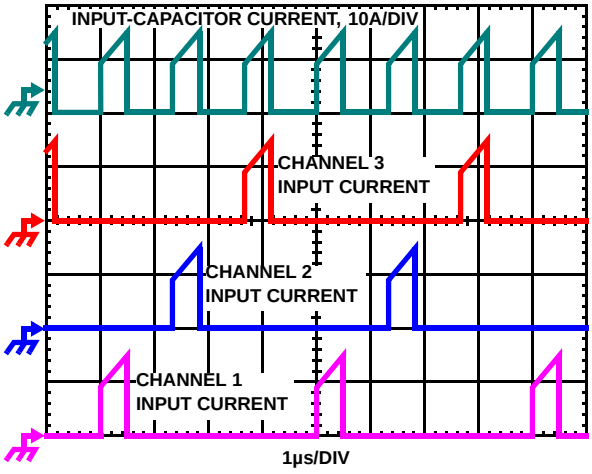



**FIGURE 2. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER**

### *Active Pulse Positioning (APP) Modulated PWM Operation*

The ISL6313B uses a proprietary Active Pulse Positioning (APP) modulation scheme to control the internal PWM signals that command each channel's driver to turn their upper and lower MOSFETs on and off. The time interval in which a PWM signal can occur is generated by an internal clock, whose cycle time is the inverse of the switching frequency set by the resistor connected to the FS pin. The advantage of Intersil's proprietary Active Pulse Positioning (APP) modulator is that the PWM signal has the ability to turn on at any point during this PWM time interval, and turn off immediately after the PWM signal has transitioned high. This is important because is allows the controller to quickly respond to output voltage drops associated with current load spikes, while avoiding the ring back affects associated with other modulation schemes.

The PWM output state is driven by the position of the error amplifier output signal, $V_{COMP}$ minus the current correction signal relative to the proprietary modulator ramp waveform as illustrated in Figure 4. At the beginning of each PWM time interval, this modified $V_{COMP}$ signal is compared to the internal modulator waveform. As long as the modified $V_{COMP}$ voltage is lower then the modulator waveform voltage, the PWM signal is commanded low. The internal MOSFET driver detects the low state of the PWM signal and turns off the upper MOSFET and turns on the lower synchronous MOSFET. When the modified $V_{COMP}$ voltage crosses the modulator ramp, the PWM output transitions high, turning off the synchronous MOSFET and turning on the upper MOSFET. The PWM signal will remain high until the modified $V_{COMP}$ voltage crosses the modulator ramp again. When this occurs the PWM signal will transition low again.

During each PWM time interval the PWM signal can only transition high once. Once PWM transitions high it can not transition high again until the beginning of the next PWM time interval. This prevents the occurrence of double PWM pulses occurring during a single period.

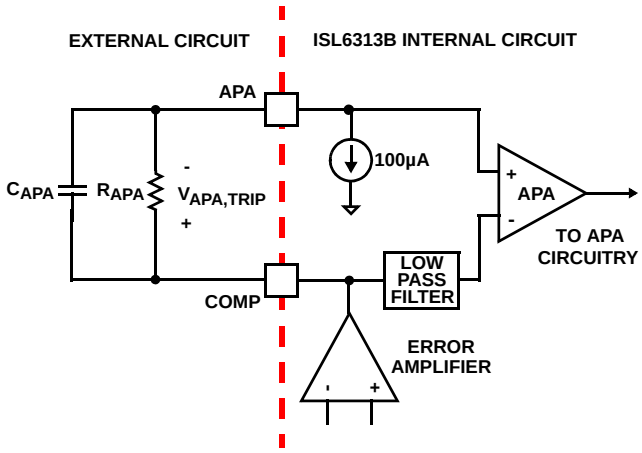



**FIGURE 3. ADAPTIVE PHASE ALIGNMENT DETECTION**

### *Adaptive Phase Alignment (APA)*

To further improve the transient response, the ISL6313B also implements Intersil's proprietary Adaptive Phase Alignment (APA) technique, which turns on all of the channels together at the same time during large current step transient events. As Figure 3 shows, the APA circuitry works by monitoring the voltage on the APA pin and comparing it to

a filtered copy of the voltage on the COMP pin. The voltage on the APA pin is a copy of the COMP pin voltage that has been negatively offset. If the APA pin exceeds the filtered COMP pin voltage an APA event occurs and all of the channels are forced on.

The APA trip level is the amount of DC offset between the COMP pin and the APA pin. This is the voltage excursion that the APA and COMP pin must have during a transient event to activate the Adaptive Phase Alignment circuitry. This APA trip level is set through a resistor, $R_{APA}$, that connects from the APA pin to the COMP pin. A 100µA current flows across $R_{APA}$ into the APA pin to set the APA trip level as described in Equation 3. An APA trip level of 500mV is recommended for most applications. A 1000pF capacitor, $C_{APA}$, should also be placed across the $R_{APA}$ resistor to help with noise immunity.

$$V_{APA(TRIP)} = R_{APA} \cdot 100 \times 10^{-6} \quad \text{(EQ. 3)}$$

### Number of Active Channels

The default number of active channels on the ISL6313B is two for 2-phase operation. If single-phase operation is desired the ISEN2- pin should be tied to the VCC pin. This will disable Channel 2, so only Channel 1 will fire. In single phase operation all of the Channel 2 pins should be left unconnected including the PHASE2, LGATE2, UGATE2, BOOT2, and ISEN2+ pins.

### Channel-Current Balance

One important benefit of multi-phase operation is the thermal advantage gained by distributing the dissipated heat over multiple devices and greater area. By doing this the designer avoids the complexity of driving parallel MOSFETs and the expense of using expensive heat sinks and exotic magnetic materials.

In order to realize the thermal advantage, it is important that each channel in a multi-phase converter be controlled to carry equal amounts of current at any load level. To achieve this, the currents through each channel must be sensed continuously every switching cycle. The sensed currents, $I_n$, from each active channel are summed together and divided by the number of active channels. The resulting cycle average current, $I_{AVG}$, provides a measure of the total load-current demand on the converter during each switching cycle. Channel-current balance is achieved by comparing the sensed current of each channel to the cycle average current, and making the proper adjustment to each channel pulse width based on the error. Intersil's patented current-balance method is illustrated in Figure 4, with error correction for channel 1 represented. In the figure, the cycle average current, $I_{AVG}$, is compared with the Channel 1 sensed current, $I_1$, to create an error signal $I_{ER}$.

The filtered error signal modifies the pulse width commanded by $V_{COMP}$ to correct any unbalance and force $I_{ER}$ toward zero. The same method for error signal correction is applied to each active channel.

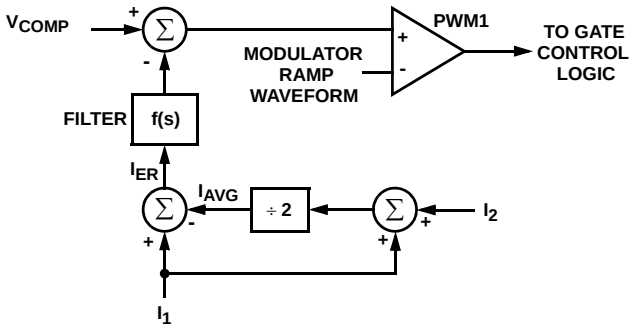



FIGURE 4. CHANNEL-1 PWM FUNCTION AND CURRENT-BALANCE ADJUSTMENT

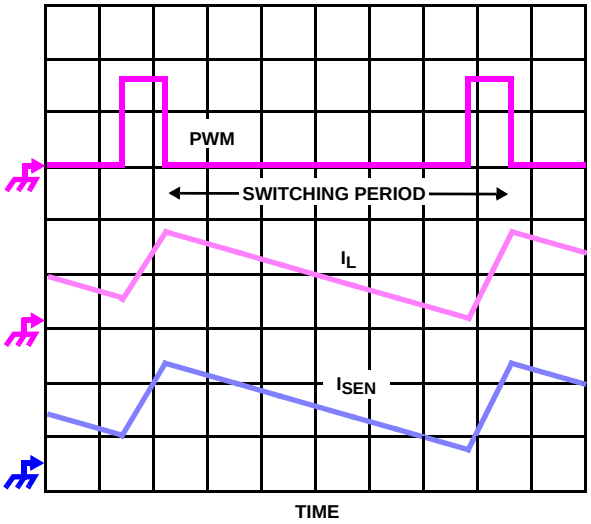



FIGURE 5. CONTINUOUS CURRENT SAMPLING

### Continuous Current Sensing

In order to realize proper current-balance, the currents in each channel are sensed continuously every switching cycle. During this time the current-sense amplifier uses the ISEN inputs to reproduce a signal proportional to the inductor current, $I_L$. This sensed current, $I_{SEN}$, is simply a scaled version of the inductor current.

The ISL6313B supports inductor DCR current sensing to continuously sense each channel's current for channel-current balance. The internal circuitry, shown in Figure 6 represents channel n of an N-Channel converter. This circuitry is repeated for each channel in the converter, but may not be active depending on how many channels are operating.

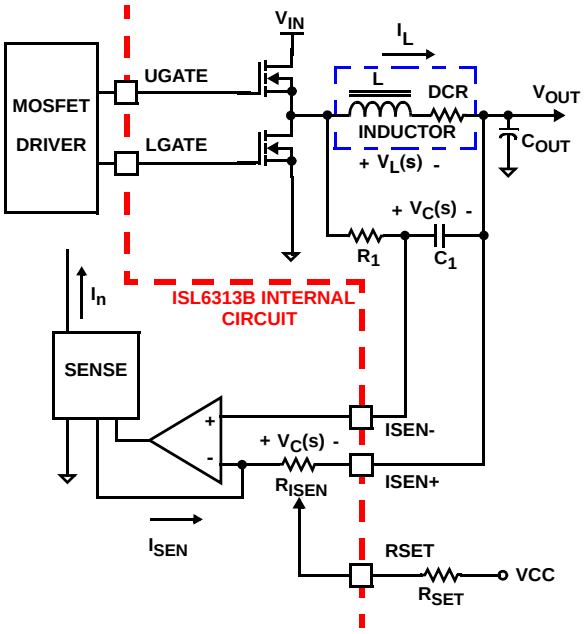



**FIGURE 6. INDUCTOR DCR CURRENT SENSING CONFIGURATION**

Inductor windings have a characteristic distributed resistance or DCR (Direct Current Resistance). For simplicity, the inductor DCR is considered as a separate lumped quantity, as shown in Figure 6. The channel current $I_L$, flowing through the inductor, passes through the DCR. Equation 4 shows the s-domain equivalent voltage, $V_L$, across the inductor.

$$V_L(s) = I_L \cdot (s \cdot L + DCR) \quad \text{(EQ. 4)}$$

A simple R-C network across the inductor ($R_1$ and C) extracts the DCR voltage, as shown in Figure 6. The voltage across the sense capacitor, $V_C$, can be shown to be proportional to the channel current $I_L$, shown in Equation 5.

$$V_C(s) = \frac{\left(\frac{s \cdot L}{DCR} + 1\right)}{(s \cdot R_1 \cdot C_1 + 1)} \cdot DCR \cdot I_L \quad \text{(EQ. 5)}$$

If the $R_1$-$C_1$ network components are selected such that their time constant matches the inductor L/DCR time constant, then $V_C$ is equal to the voltage drop across the DCR.

The capacitor voltage $V_C$, is then replicated across the effective internal sense resistance $R_{ISEN}$. This develops a current through $R_{ISEN}$ which is proportional to the inductor current. This current, $I_{SEN}$, is continuously sensed and is then used by the controller for load-line regulation, channel-current balancing, and overcurrent detection and limiting. Equation 6 shows that the proportion between the channel current, $I_L$, and the sensed current, $I_{SEN}$, is driven by the value of the effective sense resistance, $R_{ISEN}$, and the DCR of the inductor.

$$I_{SEN} = I_L \cdot \frac{DCR}{R_{ISEN}} \quad \text{(EQ. 6)}$$

The effective internal $R_{ISEN}$ resistance is important to the current sensing process because it sets the gain of the load line regulation loop as well as the gain of the channel-current balance loop and the overcurrent trip level. The effective internal $R_{ISEN}$ resistance is user programmable and is set through use of the RSET pin. Placing a single resistor, $R_{SET}$, from the RSET pin to the VCC pin programs the effective internal $R_{ISEN}$ resistance according to Equation 7 below. It is important to note that the $R_{SET}$ resistance value must be between 20kΩ and 80kΩ for Equation 7 to be valid.

$$R_{ISEN} = \frac{3}{400} \cdot R_{SET} \quad \text{(EQ. 7)}$$

***Note: $R_{SET}$ must be between 20kΩ and 80kΩ**

### *Output Voltage Setting*

The ISL6313B uses a digital to analog converter (DAC) to generate a reference voltage based on the logic signals at the VID pins. The DAC decodes the logic signals into one of the discrete voltages shown in Tables 2, 3 or 4. In the Intel VR11 mode of operation, each VID pin is pulled up to an internal 1.2V voltage by a weak current source (40µA), which decreases to 0A as the voltage at the VID pin varies from 0 to the internal 1.2V pull-up voltage. In AMD modes of operation the VID pins are pulled low by a week 20µA current source. External pull-up resistors or active-high output stages can augment the pull-up current sources, up to a voltage of 5V.

The ISL6313B accommodates three different DAC ranges: Intel VR11, AMD K8/K9 5-bit, and AMD 6-bit. The state of the SS and VID7 pins decide which DAC version is active. Refer to Table 1 for a description of how to select the desired DAC version.

**TABLE 1. ISL6313B DAC SELECT TABLE**

| DAC VERSION | SS PIN | VID7 PIN |
|---|---|---|
| INTEL VR11 | $R_{SS}$ resistor tied to GND | - |
| AMD 5-BIT | $R_{SS}$ resistor tied to VCC | high |
| AMD 6-BIT | $R_{SS}$ resistor tied to VCC | low |

**TABLE 2. VR11 VOLTAGE IDENTIFICATION CODES**

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | VDAC |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OFF |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | OFF |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1.60000 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1.59375 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1.58750 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1.58125 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1.57500 |

**TABLE 2. VR11 VOLTAGE IDENTIFICATION CODES (Continued)**

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | VDAC |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1.56875 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1.56250 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1.55625 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1.55000 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1.54375 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1.53750 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1.53125 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1.52500 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1.51875 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1.51250 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1.50625 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1.50000 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1.49375 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1.48750 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1.48125 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1.47500 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1.46875 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1.46250 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1.45625 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1.45000 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1.44375 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1.43750 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1.43125 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1.42500 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1.41875 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1.41250 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1.40625 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1.40000 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1.39375 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1.38750 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1.38125 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1.37500 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1.36875 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1.36250 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1.35625 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1.35000 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1.34375 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1.33750 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1.33125 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1.32500 |

**TABLE 2. VR11 VOLTAGE IDENTIFICATION CODES (Continued)**

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | VDAC |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1.31875 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1.31250 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1.30625 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1.30000 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1.29375 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1.28750 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1.28125 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1.27500 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1.26875 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1.26250 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1.25625 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1.25000 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1.24375 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1.23750 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1.23125 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1.22500 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1.21875 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1.21250 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1.20625 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1.20000 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1.19375 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1.18750 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1.18125 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1.17500 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1.16875 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1.16250 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1.15625 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1.15000 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1.14375 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1.13750 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1.13125 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1.12500 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1.11875 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1.11250 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1.10625 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1.10000 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1.09375 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1.08750 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1.08125 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1.07500 |

**TABLE 2. VR11 VOLTAGE IDENTIFICATION CODES (Continued)**

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | VDAC |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1.06875 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1.06250 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1.05625 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1.05000 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1.04375 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1.03750 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1.03125 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1.02500 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1.01875 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1.01250 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1.00625 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1.00000 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0.99375 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0.98750 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0.98125 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0.97500 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0.96875 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0.96250 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0.95625 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0.95000 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0.94375 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0.93750 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0.93125 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0.92500 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0.91875 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0.91250 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0.90625 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0.90000 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0.89375 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0.88750 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0.88125 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0.87500 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0.86875 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0.86250 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0.85625 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0.85000 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0.84375 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0.83750 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0.83125 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0.82500 |

**TABLE 2. VR11 VOLTAGE IDENTIFICATION CODES (Continued)**

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | VDAC |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.81875 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.81250 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.80625 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0.80000 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0.79375 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0.78750 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0.78125 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0.77500 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0.76875 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0.76250 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0.75625 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0.75000 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0.74375 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0.73750 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0.73125 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0.72500 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0.71875 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0.71250 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0.70625 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0.70000 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0.69375 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0.68750 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0.68125 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0.67500 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0.66875 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0.66250 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0.65625 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0.65000 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0.64375 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0.63750 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0.63125 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0.62500 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0.61875 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0.61250 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0.60625 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0.60000 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0.59375 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0.58750 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0.58125 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0.57500 |

**TABLE 2. VR11 VOLTAGE IDENTIFICATION CODES (Continued)**

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | VDAC |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0.56875 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0.56250 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0.55625 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0.55000 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0.54375 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0.53750 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0.53125 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0.52500 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0.51875 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0.51250 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0.50625 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0.50000 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | OFF |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | OFF |

**TABLE 3. AMD 5-BIT VOLTAGE IDENTIFICATION CODES**

| VID4 | VID3 | VID2 | VID1 | VID0 | VDAC |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | Off |
| 1 | 1 | 1 | 1 | 0 | 0.800 |
| 1 | 1 | 1 | 0 | 1 | 0.825 |
| 1 | 1 | 1 | 0 | 0 | 0.850 |
| 1 | 1 | 0 | 1 | 1 | 0.875 |
| 1 | 1 | 0 | 1 | 0 | 0.900 |
| 1 | 1 | 0 | 0 | 1 | 0.925 |
| 1 | 1 | 0 | 0 | 0 | 0.950 |
| 1 | 0 | 1 | 1 | 1 | 0.975 |
| 1 | 0 | 1 | 1 | 0 | 1.000 |
| 1 | 0 | 1 | 0 | 1 | 1.025 |
| 1 | 0 | 1 | 0 | 0 | 1.050 |
| 1 | 0 | 0 | 1 | 1 | 1.075 |
| 1 | 0 | 0 | 1 | 0 | 1.100 |
| 1 | 0 | 0 | 0 | 1 | 1.125 |
| 1 | 0 | 0 | 0 | 0 | 1.150 |
| 0 | 1 | 1 | 1 | 1 | 1.175 |
| 0 | 1 | 1 | 1 | 0 | 1.200 |
| 0 | 1 | 1 | 0 | 1 | 1.225 |
| 0 | 1 | 1 | 0 | 0 | 1.250 |
| 0 | 1 | 0 | 1 | 1 | 1.275 |
| 0 | 1 | 0 | 1 | 0 | 1.300 |
| 0 | 1 | 0 | 0 | 1 | 1.325 |

**TABLE 3. AMD 5-BIT VOLTAGE IDENTIFICATION CODES**

| VID4 | VID3 | VID2 | VID1 | VID0 | VDAC |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1.350 |
| 0 | 0 | 1 | 1 | 1 | 1.375 |
| 0 | 0 | 1 | 1 | 0 | 1.400 |
| 0 | 0 | 1 | 0 | 1 | 1.425 |
| 0 | 0 | 1 | 0 | 0 | 1.450 |
| 0 | 0 | 0 | 1 | 1 | 1.475 |
| 0 | 0 | 0 | 1 | 0 | 1.500 |
| 0 | 0 | 0 | 0 | 1 | 1.525 |
| 0 | 0 | 0 | 0 | 0 | 1.550 |

**TABLE 4. AMD 6-BIT VOLTAGE IDENTIFICATION CODES**

| VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | VDAC |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1.5500 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1.5250 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1.5000 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1.4750 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1.4500 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1.4250 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1.4000 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1.3750 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1.3500 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1.3250 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1.3000 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1.2750 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1.2500 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1.2250 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1.2000 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1.1750 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1.1500 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1.1250 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1.1000 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1.0750 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1.0500 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1.0250 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1.0000 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0.9750 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0.9500 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0.9250 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0.9000 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0.8750 |

TABLE 4. AMD 6-BIT VOLTAGE IDENTIFICATION CODES

| VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | VDAC |
|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 0 | 0 | 0.8500 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0.8250 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0.8000 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0.7750 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0.7625 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0.7500 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0.7375 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0.7250 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0.7125 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0.7000 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0.6875 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0.6750 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0.6625 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0.6500 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0.6375 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0.6250 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0.6125 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0.6000 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0.5875 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0.5750 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0.5625 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0.5500 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0.5375 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0.5250 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0.5125 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0.5000 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0.4875 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0.4750 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0.4625 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0.4500 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0.4375 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0.4250 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0.4125 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0.4000 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0.3875 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0.3750 |

## Voltage Regulation

The integrating compensation network shown in Figure 7 insures that the steady-state error in the output voltage is limited only to the error in the reference voltage (output of the DAC) and offset errors in the OFS current source, remote-sense and error amplifiers. Intersil specifies the guaranteed tolerance of the ISL6313B to include the combined tolerances of each of these elements.

The output of the error amplifier, $V_{COMP}$, is used by the modulator to generate the PWM signals. The PWM signals control the timing of the Internal MOSFET drivers and regulate the converter output so that the voltage at FB is equal to the voltage at REF. This will regulate the output voltage to be equal to Equation 8. The internal and external circuitry that controls voltage regulation is illustrated in Figure 7.

$$V_{OUT} = V_{REF} - V_{OFS} - V_{DROOP} \quad \text{(EQ. 8)}$$

The ISL6313B incorporates differential remote-sense amplification in the feedback path. The differential sensing removes the voltage error encountered when measuring the output voltage relative to the controller ground reference point resulting in a more accurate means of sensing output voltage.

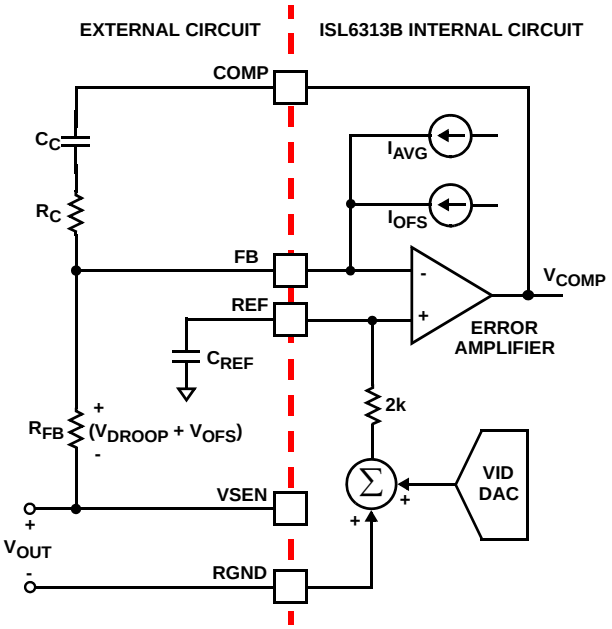



FIGURE 7. OUTPUT VOLTAGE AND LOAD-LINE REGULATION WITH OFFSET ADJUSTMENT

## Load-Line (Droop) Regulation

Some microprocessor manufacturers require a precisely-controlled output resistance. This dependence of output voltage on load current is often termed “droop” or “load line” regulation. By adding a well controlled output impedance, the output voltage can effectively be level shifted in a direction which works to achieve the load-line regulation required by these manufacturers.

In other cases, the designer may determine that a more cost-effective solution can be achieved by adding droop. Droop can help to reduce the output-voltage spike that results from fast load-current demand changes.

The magnitude of the spike is dictated by the ESR and ESL of the output capacitors selected. By positioning the no-load voltage level near the upper specification limit, a larger negative spike can be sustained without crossing the lower limit. By adding a well controlled output impedance, the output voltage under load can effectively be level shifted down so that a larger positive spike can be sustained without crossing the upper specification limit.

As shown in Figure 7, a current proportional to the average current of all active channels, $I_{AVG}$, flows from FB through a load-line regulation resistor $R_{FB}$. The resulting voltage drop across $R_{FB}$ is proportional to the output current, effectively creating an output voltage droop with a steady-state value defined as Equation 9:

$$V_{DROOP} = I_{AVG} \cdot R_{FB} \quad \text{(EQ. 9)}$$

The regulated output voltage is reduced by the droop voltage $V_{DROOP}$. The output voltage as a function of load current is derived by combining Equations 6, 8, and 9.

$$V_{OUT} = V_{REF} - V_{OFS} - \left( \frac{I_{OUT}}{N} \cdot \frac{DCR}{R_{ISEN}} \cdot R_{FB} \right) \quad \text{(EQ. 10)}$$

In Equation 10, $V_{REF}$ is the reference voltage, $V_{OFS}$ is the programmed offset voltage, $I_{OUT}$ is the total output current of the converter, $R_{ISEN}$ is the internal sense resistor connected to the ISEN+ pin, $R_{FB}$ is the feedback resistor, N is the active channel number, and DCR is the Inductor DCR value.

Therefore the equivalent loadline impedance, i.e. droop impedance, is equal to:

$$R_{LL} = \frac{R_{FB}}{N} \cdot \frac{DCR}{R_{ISEN}} \quad \text{(EQ. 11)}$$

### *Output-Voltage Offset Programming*

The ISL6313B allows the designer to accurately adjust the offset voltage by connecting a resistor, $R_{OFS}$, from the OFS pin to VCC or GND. When $R_{OFS}$ is connected between OFS and VCC, the voltage across it is regulated to 1.6V. This causes a proportional current ($I_{OFS}$) to flow into the OFS pin and out of the FB pin, providing a negative offset. If $R_{OFS}$ is connected to ground, the voltage across it is regulated to 0.3V, and $I_{OFS}$ flows into the FB pin and out of the OFS pin, providing a positive offset. The offset current flowing through the resistor between VSEN and FB will generate the desired offset voltage which is equal to the product ($I_{OFS}$ x $R_{FB}$). These functions are shown in Figures 8 and 9.

Once the desired output offset voltage has been determined, use formulas in Equations 12 and 13 to set $R_{OFS}$:

For Negative Offset (connect $R_{OFS}$ to VCC):

$$R_{OFS} = \frac{1.6 \cdot R_{FB}}{V_{OFFSET}} \quad \text{(EQ. 12)}$$

For Positive Offset (connect $R_{OFS}$ to GND):

$$R_{OFS} = \frac{0.3 \cdot R_{FB}}{V_{OFFSET}} \quad \text{(EQ. 13)}$$

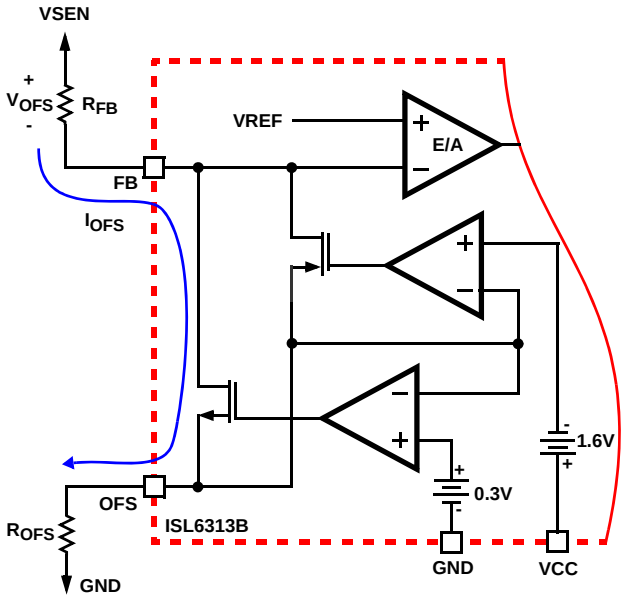



**FIGURE 8. POSITIVE OFFSET OUTPUT VOLTAGE PROGRAMMING**

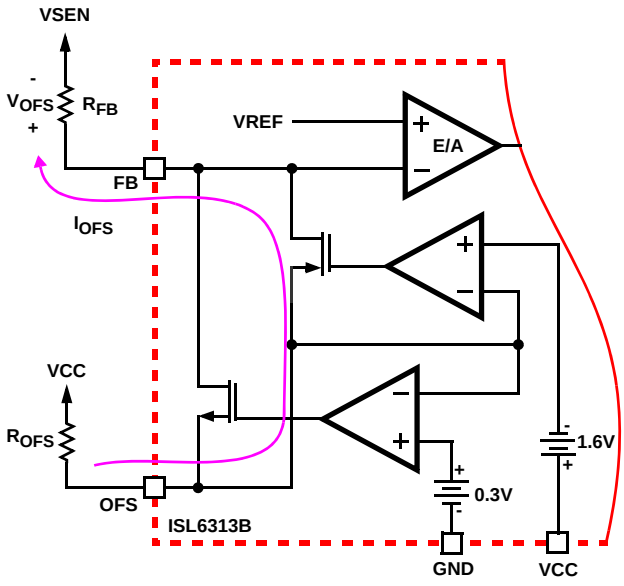



**FIGURE 9. NEGATIVE OFFSET OUTPUT VOLTAGE PROGRAMMING**

### Dynamic VID

Modern microprocessors need to make changes to their core voltage as part of normal operation. They direct the ISL6313B to do this by making changes to the VID inputs. The ISL6313B is required to monitor the DAC inputs and respond to on-the-fly VID changes in a controlled manner, supervising a safe output voltage transition without discontinuity or disruption. The DAC mode the ISL6313B is operating in determines how the controller responds to a dynamic VID change.

#### INTEL DYNAMIC VID TRANSITIONS

When in Intel VR11 mode the ISL6313B checks the VID inputs on the positive edge of an internal 5.5MHz clock. If a new code is established and it remains stable for 3 consecutive readings (0.36µs to 0.54µs), the ISL6313B recognizes the new code and changes the internal DAC reference directly to the new level. The Intel processor controls the VID transitions and is responsible for incrementing or decrementing one VID step at a time. In VR11 mode, the ISL6313B will immediately change the internal DAC reference to the new requested value as soon as the request is validated, which means the fastest recommended rate at which a bit change can occur is once every 1µs. If the VID code is changed by more then one step at a time, the DAC will try to track it at a 5.5MHz step rate. This will likely cause an overcurrent or overvoltage fault.

#### AMD DYNAMIC VID TRANSITIONS

When running in AMD 5-bit or 6-bit modes of operation, the ISL6313B responds differently to a dynamic VID change then when in Intel VR11 mode. In the AMD modes the ISL6313B still checks the VID inputs on the positive edge of an internal 5.5MHz clock. In these modes the VID code can be changed by more than a 1-bit step at a time. If a new code is established and it remains stable for 3 consecutive readings (0.36µs to 0.54µs), the ISL6313B recognizes the change and begins slewing the DAC in 6.25mV steps at a stepping frequency of 345kHz until the VID and DAC are equal. Thus, the total time required for a VID change, $t_{DVID}$, is dependent only on the size of the VID change ($\Delta V_{VID}$).

The time required for a ISL6313B-based converter in AMD 5-bit DAC configuration to make a 1.1V to 1.5V reference voltage change is about 186µs, as calculated using Equation 14.

$$t_{DVID} = \frac{1}{345 \times 10^3} \cdot \left(\frac{\Delta V_{VID}}{0.00625}\right) \quad \text{(EQ. 14)}$$

#### VID "OFF" DAC CODES

Both the Intel VR11 and the AMD 5-bit VID tables include "Off" DAC codes, which indicate to the controller to disable all regulation. Recognition of these codes is slightly different in that they must be stable for 4 consecutive readings of a 5.5MHz clock (0.54µs to 0.72µs) to be recognized. Once an "Off" code is recognized the ISL6313B latches off, and must be reset by dropping the EN pin.

### Compensating Dynamic VID Transitions

During a VID transition, the resulting change in voltage on the FB pin and the COMP pin causes an AC current to flow through the error amplifier compensation components from the FB to the COMP pin. This current then flows through the feedback resistor, $R_{FB}$, and can cause the output voltage to overshoot or undershoot at the end of the VID transition. In order to ensure the smooth transition of the output voltage during a VID change, a VID-on-the-fly compensation network is required. This network is composed of a resistor and capacitor in series, $R_{DVC}$ and $C_{DVC}$, between the DVC and the FB pin.

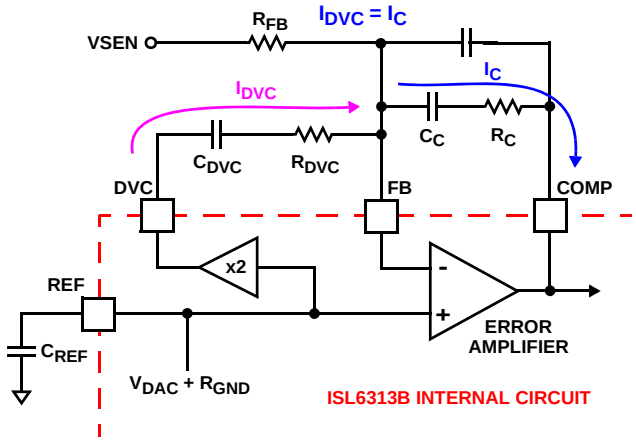



FIGURE 10. DYNAMIC VID COMPENSATION NETWORK

This VID-on-the-fly compensation network works by sourcing AC current into the FB node to offset the effects of the AC current flowing from the FB to the COMP pin during a VID transition. To create this compensation current the ISL6313B sets the voltage on the DVC pin to be 2x the voltage on the REF pin. Since the error amplifier forces the voltage on the FB pin and the REF pin to be equal, the resulting voltage across the series RC between DVC and FB is equal to the REF pin voltage. The RC compensation components, $R_{DVC}$ and $C_{DVC}$, can then be selected to create the desired amount of compensation current.

The amount of compensation current required is dependant on the modulator gain of the system, K1, and the error amplifier R-C components, $R_C$ and $C_C$, that are in series between the FB and COMP pins. Use Equations 15, 16 and 17 to calculate the RC component values, $R_{DVC}$ and $C_{DVC}$, for the VID-on-the-fly compensation network. For these equations: $V_{IN}$ is the input voltage for the power train; $V_{PP}$ is the oscillator ramp amplitude (1.5V); and $R_C$ and $C_C$ are the error amplifier R-C components between the FB and COMP pins.

$$K1 = \frac{V_{IN}}{V_{PP}} \qquad A = \frac{K1}{K1 - 1} \quad \text{(EQ. 15)}$$

$$R_{DVC} = A \times R_C \quad \text{(EQ. 16)}$$

$$C_{DVC} = \frac{C_C}{A} \quad \text{(EQ. 17)}$$

### Advanced Adaptive Zero Shoot-Through Deadtime Control (Patent Pending)

The integrated drivers incorporate a unique adaptive deadtime control technique to minimize deadtime, resulting in high efficiency from the reduced freewheeling time of the lower MOSFET body-diode conduction, and to prevent the upper and lower MOSFETs from conducting simultaneously. This is accomplished by ensuring either rising gate turns on its MOSFET with minimum and sufficient delay after the other has turned off.

During turn-off of the lower MOSFET, the PHASE voltage is monitored until it reaches a -0.3V/+0.8V (forward/reverse inductor current). At this time the UGATE is released to rise. An auto-zero comparator is used to correct the $r_{DS(ON)}$ drop in the phase voltage preventing false detection of the -0.3V phase level during $r_{DS(ON)}$ conduction period. In the case of zero current, the UGATE is released after 35ns delay of the LGATE dropping below 0.5V. When LGATE first begins to transition low, this quick transition can disturb the PHASE node and cause a false trip, so there is 20ns of blanking time once LGATE falls until PHASE is monitored.

Once the PHASE is high, the advanced adaptive shoot-through circuitry monitors the PHASE and UGATE voltages during a PWM falling edge and the subsequent UGATE turn-off. If either the UGATE falls to less than 1.75V above the PHASE or the PHASE falls to less than +0.8V, the LGATE is released to turn-on.

### Internal Bootstrap Device

Both integrated upper drivers feature an internal bootstrap Schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the PHASE node. This reduces voltage stress on the boot to phase pins.

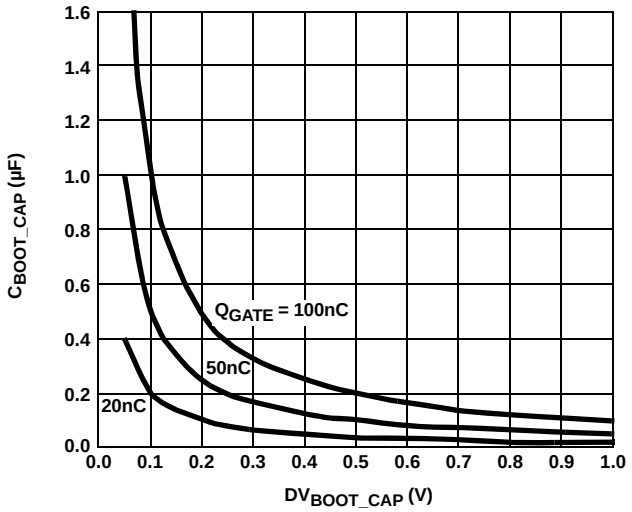



**FIGURE 11. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE**

The bootstrap capacitor must have a maximum voltage rating above PVCC + 4V and its capacitance value can be chosen from Equation 18:

$$C_{BOOT\_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT\_CAP}} \qquad \text{(EQ. 18)}$$

$$Q_{GATE} = \frac{Q_{G1} \cdot PVCC}{V_{GS1}} \cdot N_{Q1}$$

where $Q_{G1}$ is the amount of gate charge per upper MOSFET at $V_{GS1}$ gate-source voltage and $N_{Q1}$ is the number of control MOSFETs. The $\Delta V_{BOOT\_CAP}$ term is defined as the allowable droop in the rail of the upper gate drive.

### Gate Drive Voltage Versatility

The ISL6313B provides the user flexibility in choosing the gate drive voltage for efficiency optimization. The controller ties the upper and lower drive rails together. Simply applying a voltage from 5V up to 12V on PVCC sets both gate drive rail voltages simultaneously.

## Initialization

Prior to initialization, proper conditions must exist on the EN, VCC, PVCC and the VID pins. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, the controller asserts PGOOD.

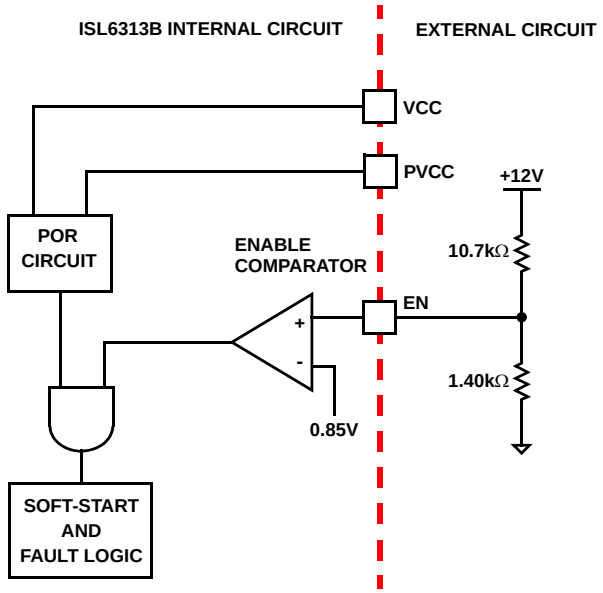



**FIGURE 12. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (EN) FUNCTION**

### Enable and Disable

While in shutdown mode, the LGATE and UGATE signals are held low to assure the MOSFETs remain off. The following input conditions must be met, for both Intel and AMD modes of operation, before the ISL6313B is released

from shutdown mode to begin the soft-start start-up sequence:

1. The bias voltage applied at VCC must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, proper operation of all aspects of the ISL6313B is guaranteed. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL6313B will not inadvertently turn off unless the bias voltage drops substantially (see Electrical Specifications on page 6).
2. The voltage on EN must be above 0.85V. The EN input allows for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the ISL6313B in shutdown until the voltage at EN rises above 0.85V. The enable comparator has 110mV of hysteresis to prevent bounce.
3. The driver bias voltage applied at the PVCC pin must reach the internal power-on reset (POR) rising threshold. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL6313B will not inadvertently turn off unless the PVCC bias voltage drops substantially (see Electrical Specifications on page 6).

For Intel VR11 and AMD 6-bit modes of operation these are the only conditions that must be met for the controller to immediately begin the soft-start sequence. If running in AMD 5-bit mode of operation there is one more condition that must be met:

4. The VID code must not be 11111 in AMD 5-bit mode. This code signals the controller that no load is present. The controller will not allow soft-start to begin if this VID code is present on the VID pins.

Once all of these conditions are met the controller will begin the soft-start sequence and will ramp the output voltage up to the user designated level.

### *Intel Soft-Start*

The soft-start function allows the converter to bring up the output voltage in a controlled fashion, resulting in a linear ramp-up. The soft-start sequence for the Intel modes of operation is slightly different then the AMD soft-start sequence.

For the Intel VR11 mode of operation, the soft-start sequence if composed of four periods, as shown in Figure 21. Once the ISL6313B is released from shutdown and soft-start begins (as described in “Enable and Disable” on page 20), the controller will have a fixed delay period $T_{d1}$ of typically 1.10ms. After this delay period, the VR will begin first soft-start ramp until the output voltage reaches 1.1V VBOOT voltage. Then, the controller will regulate the VR voltage at 1.1V for another fixed delay period $t_{d3}$, of typically 93µs. At the end of $t_{d3}$, period, ISL6313B will read the VID signals. It is recommended that the VID codes be set no later then 50µs into period $t_{d3}$,. If the VID code is valid, ISL6313B will initiate the second soft-start ramp until the output voltage reaches the VID voltage plus/minus any offset or droop voltage.

The soft-start time is the sum of the 4 periods as shown in Equation 19.

$$t_{SS} = t_{d1} + t_{d2} + t_{d3} + t_{d4} \quad \text{(EQ. 19)}$$

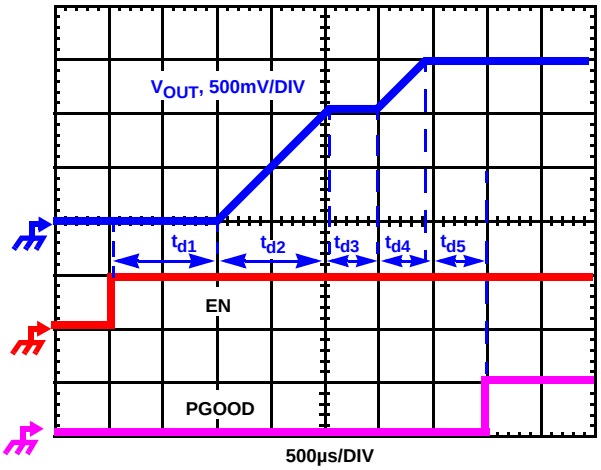



**FIGURE 13. SOFT-START WAVEFORMS**

During $t_{d2}$ and $t_{d4}$, ISL6313B digitally controls the DAC voltage change at 6.25mV per step. The time for each step is determined by the frequency of the soft-start oscillator which is defined by the resistor $R_{SS}$ on the SS pin. The second soft-start ramp time $t_{d2}$ and $t_{d4}$ can be calculated based on Equations 20 and 21:

$$t_{d2} = 1.1 \cdot R_{SS} \cdot 8 \cdot 10^{-3} (\mu s) \quad \text{(EQ. 20)}$$

$$t_{d4} = \left|V_{VID} - 1.1\right| \cdot R_{SS} \cdot 8 \cdot 10^{-3} (\mu s) \quad \text{(EQ. 21)}$$

For example, when VID is set to 1.5V and the $R_{SS}$ is set at 100kΩ, the first soft-start ramp time $t_{d2}$ will be 880µs and the second soft-start ramp time $t_{d4}$ will be 320µs.

After the DAC voltage reaches the final VID setting, PGOOD will be set to high with the fixed delay $t_{d5}$. The typical value for $t_{d5}$ is 93µs.

### *AMD Soft-Start*

For the AMD 5-bit and 6-bit modes of operation, the soft-start sequence is composed of two periods, as shown in Figure 14. At the beginning of soft-start, the VID code is immediately obtained from the VID pins, followed by a fixed delay period $t_{dA}$ of typically 1.10ms. After this delay period the ISL6313B will begin ramping the output voltage to the desired DAC level at a fixed rate of 6.25mV per step. The time for each step is determined by the frequency of the soft-start oscillator which is defined by the resistor $R_{SS}$ on the SS pin. The amount of time required to ramp the output

voltage to the final DAC voltage is referred to as tDB, and can be calculated as shown in Equation 22:

$$tDB = V_{VID} \cdot R_{SS} \cdot 8 \cdot 10^{-3} (\mu s) \quad \text{(EQ. 22)}$$

At the end of soft-start, PGOOD will immediately go high if the VSEN voltage is within the undervoltage and overvoltage limits.

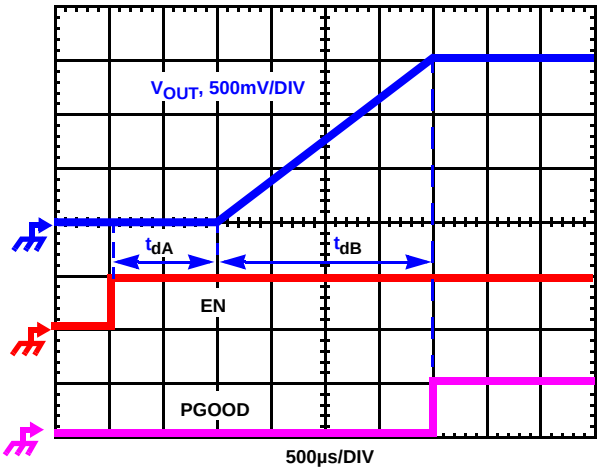



FIGURE 14. SOFT-START WAVEFORMS

### Pre-Biased Soft-Start

The ISL6313B also has the ability to start up into a pre-charged output, without causing any unnecessary disturbance. The FB pin is monitored during soft-start, and should it be higher than the equivalent internal ramping reference voltage, the output drives hold both MOSFETs off.

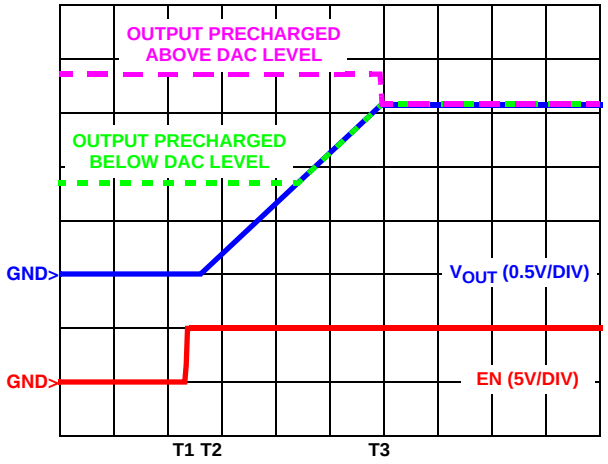



FIGURE 15. SOFT-START WAVEFORMS FOR ISL6313B-BASED MULTI-PHASE CONVERTER

Once the internal ramping reference exceeds the FB pin potential, the output drives are enabled, allowing the output to ramp from the pre-charged level to the final level dictated by the DAC setting. Should the output be pre-charged to a level exceeding the DAC setting, the output drives are enabled at the end of the soft-start period, leading to an abrupt correction in the output voltage down to the DAC-set level.

## Fault Monitoring and Protection

The ISL6313B actively monitors output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to a microprocessor load. One common power good indicator is provided for linking to external system monitors. The schematic in Figure 16 outlines the interaction between the fault monitors and the power-good signal.

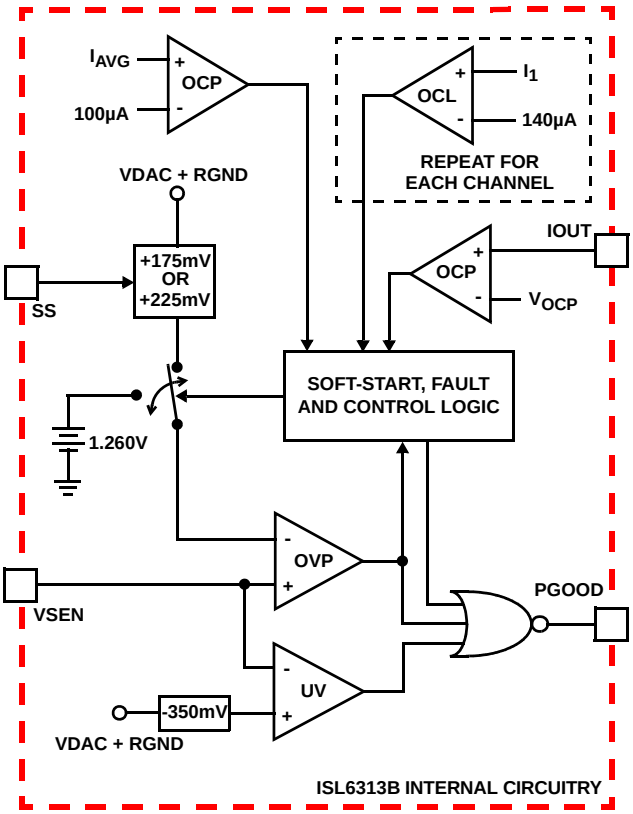



FIGURE 16. POWER GOOD AND PROTECTION CIRCUITRY

### Power-Good Signal

The power-good pin (PGOOD) is an open-drain logic output that signals whether or not the ISL6313B is regulating the output voltage within the proper levels, and whether any fault conditions exist. This pin should be tied through a resistor to a voltage source that's equal to or less then VCC.

For Intel mode of operation, PGOOD indicates whether VSEN is within specified overvoltage and undervoltage limits after a fixed delay from the end of soft-start. PGOOD transitions low when an undervoltage, overvoltage, or overcurrent condition is detected or when the controller is disabled by a reset from EN, POR, or one of the no-CPU VID codes. In the event of an overvoltage or overcurrent condition, or a no-CPU VID code, the controller latches off and PGOOD will not return high until EN is toggled and a successful soft-start is

completed. In the case of an undervoltage event, PGOOD will return high when the output voltage rises above the undervoltage hysteresis level. PGOOD is always low prior to the end of soft-start.

For AMD modes of operation, PGOOD will always be high as long as VSEN is within the specified undervoltage/ overvoltage window and soft-start has ended. PGOOD only goes low if VSEN is outside this window. Even if the controller is shut down the PGOOD signal will still stay high until VSEN falls below the undervoltage threshold.

### Overvoltage Protection

The ISL6313B constantly monitors the difference between the $V_{SEN}$ and $R_{GND}$ voltages to detect if an overvoltage event occurs. During soft-start, while the DAC is ramping up, the overvoltage trip level is the higher of a fixed voltage 1.260V or DAC + 175mV for Intel modes of operation and DAC + 225mV for AMD modes of operation. Upon successful soft-start, the overvoltage trip level is only DAC + 175mV or DAC + 225mV depending on whether the controller is running in Intel or AMD mode. When the output voltage rises above the OVP trip level actions are taken by the ISL6313B to protect the microprocessor load.

At the inception of an overvoltage event, $L_{GATE1}$ and $L_{GATE2}$ are commanded high and the PGOOD signal is driven low. This turns on the all of the lower MOSFETs and pulls the output voltage below a level that might cause damage to the load. The $L_{GATE}$ outputs remain high until $V_{SEN}$ falls 100mV below the OVP threshold that tripped the overvoltage protection circuitry. The ISL6313B will continue to protect the load in this fashion as long as the overvoltage condition recurs. Once an overvoltage condition ends the ISL6313B latches off, and must be reset by toggling EN, or through POR, before a soft-start can be reinitiated.

There is an OVP condition that exists that will not latch off the ISL6313B. During a soft-start sequence, if the $V_{SEN}$ voltage is above the OVP threshold an overvoltage event will occur, but will be released once $V_{SEN}$ falls 100mV below the OVP threshold. If $V_{SEN}$ then rises above the OVP trip threshold a second time, the ISL6313B will be latched off and cannot be restarted until the controller is reset.

### Pre-POR Overvoltage Protection

Prior to $P_{VCC}$ and VCC exceeding their POR levels, the ISL6313B is designed to protect the load from any overvoltage events that may occur. This is accomplished by means of an internal 10kΩ resistor tied from PHASE to LGATE, which turns on the lower MOSFET to control the output voltage until the overvoltage event ceases or the input power supply cuts off. For complete protection, the low side MOSFET should have a gate threshold well below the maximum voltage rating of the load/microprocessor.

In the event that during normal operation the $P_{VCC}$ or VCC voltage falls back below the POR threshold, the pre-POR overvoltage protection circuitry reactivates to protect from any more pre-POR overvoltage events.

### Undervoltage Detection

The undervoltage threshold is set at DAC - 350mV of the VID code. When the output voltage ($V_{SEN}$ - $R_{GND}$) is below the undervoltage threshold, PGOOD gets pulled low. No other action is taken by the controller. PGOOD will return high if the output voltage rises above DAC - 250mV.

### Open Sense Line Prevention

In the case that either of the remote sense lines, VSEN or GND, become open, the ISL6313B is designed to prevent the controller from regulating. This is accomplished by means of a small 5µA pull-up current on VSEN, and a pull-down current on RGND. If the sense lines are opened at any time, the voltage difference between $V_{SEN}$ and $R_{GND}$ will increase until an overvoltage event occurs, at which point overvoltage protection activates and the controller stops regulating. The ISL6313B will be latched off and cannot be restarted until the controller is reset.

### Overcurrent Protection

The ISL6313B takes advantage of the proportionality between the load current and the average current, $I_{AVG}$, to detect an overcurrent condition. Two different methods of detecting overcurrent events are available on the ISL6313B. The first method continually compares the average sense current with a constant 100µA OCP reference current as shown in Figure 16. Once the average sense current exceeds the OCP reference current, a comparator triggers the converter to begin overcurrent protection procedures.

For this first method the overcurrent trip threshold is dictated by the DCR of the inductors, the number of active channels, and the RSET pin resistor, $R_{SET}$. To calculate the overcurrent trip level, $I_{OCP}$, using this method use Equation 23, where N is the number of active channels, DCR is the individual inductor's DCR, and $R_{SET}$ is the RSET pin resistor value.

$$I_{OCP} = \frac{100 \cdot 10^{-6} \cdot R_{SET} \cdot N \cdot 3}{DCR \cdot 400} \quad \text{(EQ. 23)}$$

During VID-on-the-fly transitions the overcurrent trip level for this method is boosted to prevent false overcurrent trip events that can occur. Starting from the beginning of a dynamic VID transition, the overcurrent trip level is boosted to 140µA. The OCP level will stay at this boosted level until 50µs after the end of the dynamic VID transition, at which point it will return to the typical 100µA trip level.

The second method for detecting overcurrent events continuously compares the voltage on the IOUT pin, $V_{IOUT}$, to the overcurrent protection voltage, $V_{OCP}$, as shown in Figure 16. The average channel sense current flows out the IOUT pin and through $R_{IOUT}$, creating the IOUT pin voltage which is proportional to the output current. When the IOUT

pin voltage exceeds the $V_{OCP}$ voltage of 2.0V, the overcurrent protection circuitry activates. Since the IOUT pin voltage is proportional to the output current, the overcurrent trip level, $I_{OCP}$, can be set by selecting the proper value for $R_{IOUT}$, as shown in Equation 24.

$$I_{OCP} = \frac{6 \cdot R_{SET} \cdot N}{DCR \cdot R_{IOUT} \cdot 400} \quad \text{(EQ. 24)}$$

Once the output current exceeds the overcurrent trip level, $V_{IOUT}$ will exceed $V_{OCP}$ and a comparator will trigger the converter to begin overcurrent protection procedures.

At the beginning of an overcurrent shutdown, the controller turns off both upper and lower MOSFETs and lowers PGOOD. The controller will then immediately attempt to soft-start. If the overcurrent fault remains, the trip-retry cycles will continue until either the controller is disabled or the fault is cleared. If five overcurrent events occur without successfully completing soft-start, the controller will latch off after the fifth try and must be reset by toggling EN before a soft-start can be reinitiated. Note that the energy delivered during trip-retry cycling is much less than during full-load operation, so there is no thermal hazard.

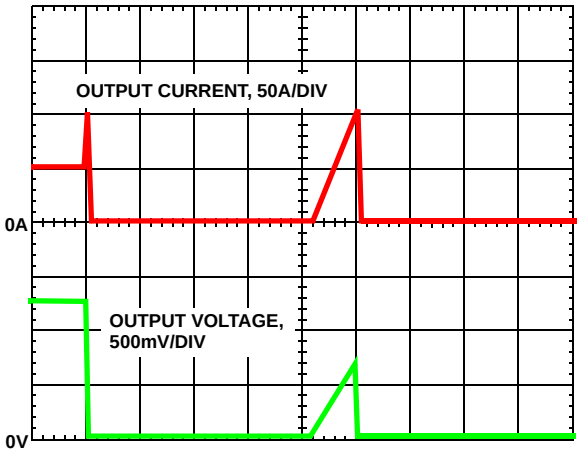



**FIGURE 17. OVERCURRENT BEHAVIOR IN HICCUP MODE**

### *Individual Channel Overcurrent Limiting*

The ISL6313B has the ability to limit the current in each individual channel without shutting down the entire regulator. This is accomplished by continuously comparing the sensed currents of each channel with a constant 140µA OCL reference current as shown in Figure 16. If a channel's individual sensed current exceeds this OCL limit, the UGATE signal of that channel is immediately forced low, and the LGATE signal is forced high. This turns off the upper MOSFET(s), turns on the lower MOSFET(s), and stops the rise of current in that channel, forcing the current in the channel to decrease. That channel's UGATE signal will not be able to return high until the sensed channel current falls back below the 140µA reference.

During VID-on-the-fly transitions the OCL trip level is boosted to prevent false overcurrent limiting events that can occur. Starting from the beginning of a dynamic VID transition, the overcurrent trip level is boosted to 196µA. The OCL level will stay at this boosted level until 50µs after the end of the dynamic VID transition, at which point it will return to the typical 140µA trip level.

## *General Design Guide*

This design guide is intended to provide a high-level explanation of the steps necessary to create a multi-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced below. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts for all common microprocessor applications.

### *Power Stages*

The first step in designing a multi-phase converter is to determine the number of phases. This determination depends heavily on the cost analysis which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board, whether through-hole components are permitted, the total board space available for power-supply circuitry, and the maximum amount of load current. Generally speaking, the most economical solutions are those in which each phase handles between 25A and 30A. All surface-mount designs will tend toward the lower end of this current range. If through-hole MOSFETs and inductors can be used, higher per-phase currents are possible. In cases where board space is the limiting constraint, current can be pushed as high as 40A per phase, but these designs require heat sinks and forced air to cool the MOSFETs, inductors and heat-dissipating surfaces.

#### MOSFETS

The choice of MOSFETs depends on the current each MOSFET will be required to conduct, the switching frequency, the capability of the MOSFETs to dissipate heat, and the availability and nature of heat sinking and air flow.

#### LOWER MOSFET POWER CALCULATION

The calculation for power loss in the lower MOSFET is simple, since virtually all of the loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$). In Equation 25, $I_M$ is the maximum continuous output current, $I_{PP}$ is the peak-to-peak inductor current (see Equation 1 on page 10), and d is the duty cycle ($V_{OUT}/V_{IN}$).

$$P_{LOW(1)} = r_{DS(ON)} \cdot \left[\left(\frac{I_M}{N}\right)^2 \cdot (1-d) + \frac{I_{L(PP)}^2 \cdot (1-d)}{12}\right] \quad \text{(EQ. 25)}$$

An additional term can be added to the lower-MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the

lower-MOSFET body diode. This term is dependent on the diode forward voltage at $I_M$, $V_{D(ON)}$, the switching frequency, $f_S$, and the length of dead times, $t_{d1}$ and $t_{d2}$, at the beginning and the end of the lower-MOSFET conduction interval respectively.

$$P_{LOW(2)} = V_{D(ON)} \cdot f_S \cdot \left[ \left( \frac{I_M}{N} + \frac{I_{PP}}{2} \right) \cdot t_{d1} + \left( \frac{I_M}{N} - \frac{I_{PP}}{2} \right) \cdot t_{d2} \right] \quad \text{(EQ. 26)}$$

The total maximum power dissipated in each lower MOSFET is approximated by the summation of $P_{LOW(1)}$ and $P_{LOW(2)}$.

**UPPER MOSFET POWER CALCULATION**

In addition to $r_{DS(ON)}$ losses, a large portion of the upper-MOSFET losses are due to currents conducted across the input voltage ($V_{IN}$) during switching. Since a substantially higher portion of the upper-MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses can be divided into separate components involving the upper-MOSFET switching times, the lower-MOSFET body-diode reverse-recovery charge, $Q_{rr}$, and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 27, the required time for this commutation is $t_1$ and the approximated associated power loss is $P_{UP(1)}$.

$$P_{UP(1)} \approx V_{IN} \cdot \left( \frac{I_M}{N} + \frac{I_{PP}}{2} \right) \cdot \left( \frac{t_1}{2} \right) \cdot f_S \quad \text{(EQ. 27)}$$

At turn on, the upper MOSFET begins to conduct and this transition occurs over a time $t_2$. In Equation 28, the approximate power loss is $P_{UP(2)}$.

$$P_{UP(2)} \approx V_{IN} \cdot \left( \frac{I_M}{N} - \frac{I_{PP}}{2} \right) \cdot \left( \frac{t_2}{2} \right) \cdot f_S \quad \text{(EQ. 28)}$$

A third component involves the lower MOSFET reverse-recovery charge, $Q_{rr}$. Since the inductor current has fully commutated to the upper MOSFET before the lower-MOSFET body diode can recover all of $Q_{rr}$, it is conducted through the upper MOSFET across VIN. The power dissipated as a result is $P_{UP(3)}$.

$$P_{UP(3)} = V_{IN} \cdot Q_{rr} \cdot f_S \quad \text{(EQ. 29)}$$

Finally, the resistive part of the upper MOSFET is given in Equation 30 as $P_{UP(4)}$.

$$P_{UP(4)} \approx r_{DS(ON)} \cdot d \cdot \left[ \left( \frac{I_M}{N} \right)^2 + \frac{I_{PP}^2}{12} \right] \quad \text{(EQ. 30)}$$

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 27, 28, 29 and 30. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies.

### *Package Power Dissipation*

When choosing MOSFETs it is important to consider the amount of power being dissipated in the integrated drivers located in the controller. Since there are a total of three drivers in the controller package, the total power dissipated by all three drivers must be less than the maximum allowable power dissipation for the TQFN package.

Calculating the power dissipation in the drivers for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of +125°C. The maximum allowable IC power dissipation for the 6x6 TQFN package is approximately 3.5W at room temperature. See “Layout Considerations” on page 31 for thermal transfer improvement suggestions.

When designing the ISL6313B into an application, it is recommended that the following calculation is used to ensure safe operation at the desired frequency for the selected MOSFETs. The total gate drive power losses, $P_{Qg\_TOT}$, due to the gate charge of MOSFETs and the integrated driver’s internal circuitry and their corresponding average driver current can be estimated with Equations 31 and 32, respectively.

$$P_{Qg\_TOT} = P_{Qg\_Q1} + P_{Qg\_Q2} + I_Q \cdot VCC \quad \text{(EQ. 31)}$$

$$P_{Qg\_Q1} = \frac{3}{2} \cdot Q_{G1} \cdot PVCC \cdot F_{SW} \cdot N_{Q1} \cdot N_{PHASE}$$

$$P_{Qg\_Q2} = Q_{G2} \cdot PVCC \cdot F_{SW} \cdot N_{Q2} \cdot N_{PHASE}$$

$$I_{DR} = \left( \frac{3}{2} \cdot Q_{G1} \cdot N_{Q1} + Q_{G2} \cdot N_{Q2} \right) \cdot N_{PHASE} \cdot F_{SW} + I_Q \quad \text{(EQ. 32)}$$

In Equations 31 and 32, $P_{Qg\_Q1}$ is the total upper gate drive power loss and $P_{Qg\_Q2}$ is the total lower gate drive power loss; the gate charge ($Q_{G1}$ and $Q_{G2}$) is defined at the particular gate to source drive voltage PVCC in the corresponding MOSFET data sheet; $I_Q$ is the driver total quiescent current with no load at both drive outputs; $N_{Q1}$ and $N_{Q2}$ are the number of upper and lower MOSFETs per phase, respectively; $N_{PHASE}$ is the number of active phases. The $I_Q$*VCC product is the quiescent power of the controller without capacitive load and is typically 75mW at 300kHz.

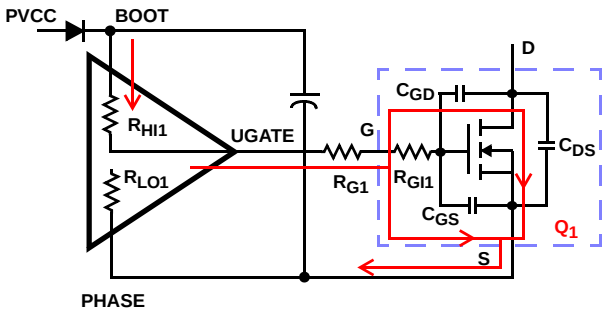



**FIGURE 18. TYPICAL UPPER-GATE DRIVE TURN-ON PATH**

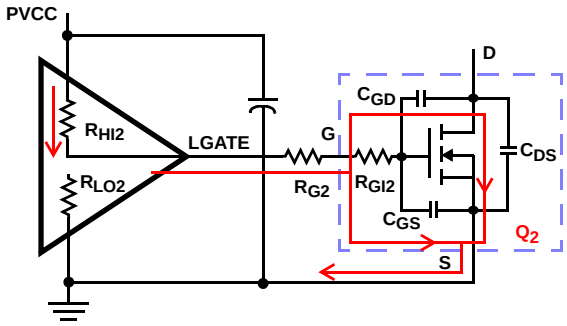



**FIGURE 19. TYPICAL LOWER-GATE DRIVE TURN-ON PATH**

The total gate drive power losses are dissipated among the resistive components along the transition path and in the bootstrap diode. The portion of the total power dissipated in the controller itself is the power dissipated in the upper drive path resistance, $P_{DR\_UP}$, the lower drive path resistance, $P_{DR\_UP}$, and in the boot strap diode, $P_{BOOT}$. The rest of the power will be dissipated by the external gate resistors ($R_{G1}$ and $R_{G2}$) and the internal gate resistors ($R_{GI1}$ and $R_{GI2}$) of the MOSFETs. Figures 18 and 19 show the typical upper and lower gate drives turn-on transition path. The total power dissipation in the controller itself, $P_{DR}$, can be roughly estimated as:

$$P_{DR} = P_{DR\_UP} + P_{DR\_LOW} + P_{BOOT} + (I_Q \cdot VCC) \qquad \text{(EQ. 33)}$$

$$P_{BOOT} = \frac{P_{Qg\_Q1}}{3}$$

$$P_{DR\_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right) \cdot \frac{P_{Qg\_Q1}}{3}$$

$$P_{DR\_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right) \cdot \frac{P_{Qg\_Q2}}{2}$$

$$R_{EXT1} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

## *Inductor DCR Current Sensing Component Selection*

The ISL6313B senses each individual channel's inductor current by detecting the voltage across the output inductor DCR of that channel (As described in "Continuous Current Sensing" on page 12). As Figure 20 illustrates, an R-C network is required to accurately sense the inductor DCR voltage and convert this information into a current, which is proportional to the total output current. The time constant of this R-C network must match the time constant of the inductor L/DCR.

Follow the steps below to choose the component values for this RC network.

1. Choose an arbitrary value for $C_1$. The recommended value is 0.1µF.
2. Plug the inductor L and DCR component values, and the value for $C_1$ chosen in step 1, into Equation 34 to calculate the value for $R_1$.

$$R_1 = \frac{L}{DCR \cdot C_1} \qquad \text{(EQ. 34)}$$

Once the R-C network components have been chosen, the effective internal $R_{ISEN}$ resistance must then be set. The $R_{ISEN}$ resistance sets the gain of the load line regulation loop as well as the gain of the channel-current balance loop and the overcurrent trip level. The effective internal $R_{ISEN}$ resistance is set through a single resistor on the RSET pin, $R_{SET}$.

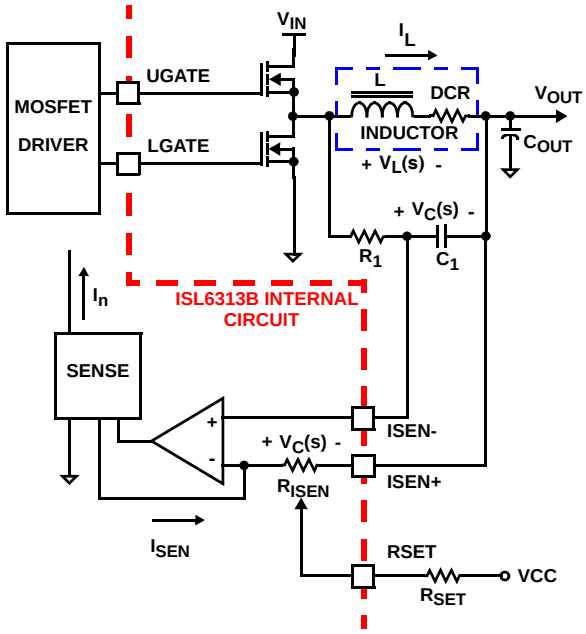



**FIGURE 20. DCR SENSING CONFIGURATION**

Use Equation 35 to calculate the value of $R_{SET}$. In Equation 35, DCR is the DCR of the output inductor at room temperature, $I_{OCP}$ is the desired overcurrent trip level, and N is the number of phases. It is recommended that the

desired overcurrent trip level, $I_{OCP}$, be chosen so that it's 30% larger then the maximum load current expected.

$$R_{SET} = \frac{DCR}{100 \times 10^{-6}} \cdot \frac{I_{OCP}}{N} \cdot \frac{400}{3} \quad \text{(EQ. 35)}$$

***Note: $R_{SET}$ must be between 20kΩ and 80kΩ**

Due to errors in the inductance or DCR it may be necessary to adjust the value of $R_1$ to match the time constants correctly. The effects of time constant mismatch can be seen in the form of droop overshoot or undershoot during the initial load transient spike, as shown in Figure 21. Follow the steps below to ensure the R-C and inductor L/DCR time constants are matched accurately.

1. Capture a transient event with the oscilloscope set to about L/DCR/2 (sec/div). For example, with L = 1µH and DCR = 1mΩ, set the oscilloscope to 500µs/div.
2. Record ΔV1 and ΔV2 as shown in Figure 21.
3. Select new values, $R_{1(NEW)}$, for the time constant resistor based on the original value, $R_{1(OLD)}$, using Equation 36.

$$R_{1(NEW)} = R_{1(OLD)} \cdot \frac{\Delta V_1}{\Delta V_2} \quad \text{(EQ. 36)}$$

4. Replace $R_1$ with the new value and check to see that the error is corrected. Repeat the procedure if necessary.

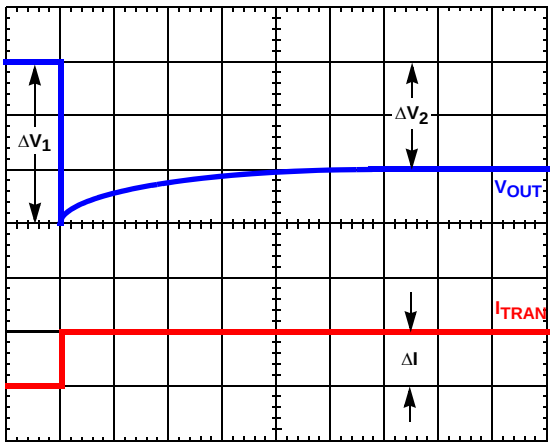



**FIGURE 21. TIME CONSTANT MISMATCH BEHAVIOR**

### Loadline Regulation Resistor

If loadline regulation is desired, the resistor on the FS pin, $R_T$, should be connected to Ground in order for the internal average sense current to flow out across the loadline regulation resistor, labeled $R_{FB}$ in Figure 7. This resistor's value sets the desired loadline required for the application. The desired loadline, $R_{LL}$, can be calculated by Equation 37 where $V_{DROOP}$ is the desired droop voltage at the full load current $I_{FL}$.

$$R_{LL} = \frac{V_{DROOP}}{I_{FL}} \quad \text{(EQ. 37)}$$

Based on the desired loadline, the loadline regulation resistor, $R_{FB}$, can be calculated from Equation 38.

$$R_{FB} = \frac{R_{LL} \cdot N \cdot R_{SET}}{DCR} \cdot \frac{3}{400} \quad \text{(EQ. 38)}$$

In Equation 38, $R_{LL}$ is the loadline resistance; N is the number of active channels; DCR is the DCR of the individual output inductors; and $R_{SET}$ is the RSET pin resistor.

If no loadline regulation is required, the resistor on the FS pin, $R_T$, should be connected to the VCC pin. To choose the value for $R_{FB}$ in this situation, please refer to "Compensation without load-line regulation" on page 28.

### IOUT Pin Resistor

A copy of the average sense current flows out of the IOUT pin, and a resistor, $R_{IOUT}$, placed from this pin to ground can be used to set the overcurrent protection trip level. Based on the desired overcurrent trip threshold, $I_{OCP}$, the IOUT pin resistor, $R_{IOUT}$, can be calculated from Equation 39.

$$R_{IOUT} = \frac{R_{SET} \cdot N}{DCR \cdot I_{OCP}} \cdot \frac{6}{400} \quad \text{(EQ. 39)}$$

### APA Pin Component Selection

A 100µA current flows into the APA pin and across $R_{APA}$ to set the APA trip level. A 1000pF capacitor, $C_{APA}$, should also be placed across the $R_{APA}$ resistor to help with noise immunity. Use Equation 40 to set $R_{APA}$ to get the desired APA trip level. An APA trip level of 500mV is recommended for most applications.

$$R_{APA} = \frac{V_{APA(TRIP)}}{100 \times 10^{-6}} = \frac{500mV}{100 \times 10^{-6}} = 5k\Omega \quad \text{(EQ. 40)}$$

### Compensation

The two opposing goals of compensating the voltage regulator are stability and speed. Depending on whether the regulator employs the optional load-line regulation as described in Load-Line Regulation, there are two distinct methods for achieving these goals.

#### COMPENSATION WITH LOAD-LINE REGULATION

The load-line regulated converter behaves in a similar manner to a peak current mode controller because the two poles at the output filter L-C resonant frequency split with the introduction of current information into the control loop. The final location of these poles is determined by the system function, the gain of the current signal, and the value of the compensation components, $R_C$ and $C_C$.

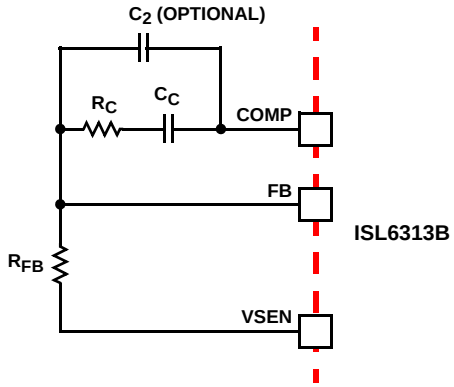



**FIGURE 22. COMPENSATION CONFIGURATION FOR LOAD-LINE REGULATED ISL6313B CIRCUIT**

Since the system poles and zero are affected by the values of the components that are meant to compensate them, the solution to the system equation becomes fairly complicated. Fortunately, there is a simple approximation that comes very close to an optimal solution. Treating the system as though it were a voltage-mode regulator, by compensating the L-C poles and the ESR zero of the voltage mode approximation, yields a solution that is always stable with very close to ideal transient performance.

Select a target bandwidth for the compensated system, $f_0$. The target bandwidth must be large enough to assure adequate transient performance, but smaller than 1/3 of the per-channel switching frequency. The values of the compensation components depend on the relationships of $f_0$ to the L-C pole frequency and the ESR zero frequency. For each of the following three, there is a separate set of equations for the compensation components.

In Equation 41, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent series resistance of the bulk output filter capacitance; and $V_{PP}$ is the peak-to-peak sawtooth signal amplitude as described in the Electrical Specifications on page 6.

Once selected, the compensation values in Equation 41 assure a stable converter with reasonable transient performance. In most cases, transient performance can be improved by making adjustments to $R_C$. Slowly increase the value of $R_C$ while observing the transient performance on an oscilloscope until no further improvement is noted. Normally, $C_C$ will not need adjustment. Keep the value of $C_C$ from Equation 41 unless some performance issue is noted

The optional capacitor $C_2$, is sometimes needed to bypass noise away from the PWM comparator (see Figure 22). Keep a position available for $C_2$, and be prepared to install a high-frequency capacitor of between 22pF and 150pF in case any leading edge jitter problem is noted.

Case 1:

$$\frac{1}{2\cdot\pi\cdot\sqrt{L\cdot C}} > f_0$$

$$R_C = R_{FB}\cdot\frac{2\cdot\pi\cdot f_0\cdot V_{pp}\cdot\sqrt{L\cdot C}}{V_{IN}}$$

$$C_C = \frac{V_{IN}}{2\cdot\pi\cdot V_{PP}\cdot R_{FB}\cdot f_0}$$

Case 2:

$$\frac{1}{2\cdot\pi\cdot\sqrt{L\cdot C}} \le f_0 < \frac{1}{2\cdot\pi\cdot C\cdot ESR}$$

$$R_C = R_{FB}\cdot\frac{V_{PP}\cdot(2\cdot\pi)^2\cdot f_0^2\cdot L\cdot C}{V_{IN}} \qquad \text{(EQ. 41)}$$

$$C_C = \frac{V_{IN}}{(2\cdot\pi)^2\cdot f_0^2\cdot V_{PP}\cdot R_{FB}\cdot\sqrt{L\cdot C}}$$

Case 3:

$$f_0 > \frac{1}{2\cdot\pi\cdot C\cdot ESR}$$

$$R_C = R_{FB}\cdot\frac{2\cdot\pi\cdot f_0\cdot V_{pp}\cdot L}{V_{IN}\cdot ESR}$$

$$C_C = \frac{V_{IN}\cdot ESR\cdot\sqrt{C}}{2\cdot\pi\cdot V_{PP}\cdot R_{FB}\cdot f_0\cdot\sqrt{L}}$$

## COMPENSATION WITHOUT LOAD-LINE REGULATION

The non load-line regulated converter is accurately modeled as a voltage-mode regulator with two poles at the L-C resonant frequency and a zero at the ESR frequency. A type III controller, as shown in Figure 23, provides the necessary compensation.

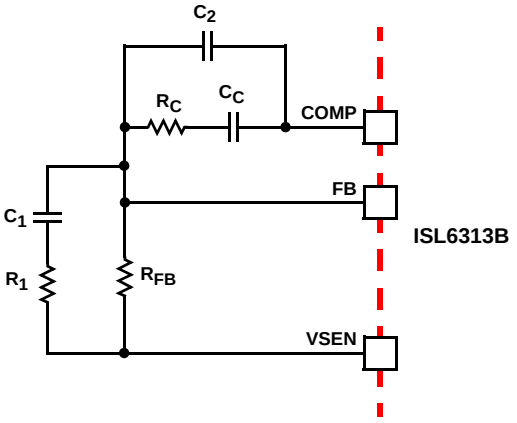



**FIGURE 23. COMPENSATION CIRCUIT WITHOUT LOAD-LINE REGULATION**

The first step is to choose the desired bandwidth, $f_0$, of the compensated system. Choose a frequency high enough to assure adequate transient performance but not higher than 1/3 of the switching frequency. The type-III compensator has an extra high-frequency pole, $f_{HF}$. This pole can be used for added noise rejection or to assure adequate attenuation at the error-amplifier high-order pole and zero frequencies. A

good general rule is to choose $f_{HF} = 10f_0$, but it can be higher if desired. Choosing $f_{HF}$ to be lower than $10f_0$ can cause problems with too much phase shift below the system bandwidth.

$$R_1 = R_{FB} \cdot \frac{C \cdot ESR}{\sqrt{L \cdot C} - C \cdot ESR}$$

$$C_1 = \frac{\sqrt{L \cdot C} - C \cdot ESR}{R_{FB}}$$

$$C_2 = \frac{V_{IN}}{(2 \cdot \pi)^2 \cdot f_0 \cdot f_{HF} \cdot (\sqrt{L \cdot C}) \cdot R_{FB} \cdot V_{PP}} \quad \text{(EQ. 42)}$$

$$R_C = \frac{V_{PP} \cdot \left(2\pi\right)^2 \cdot f_0 \cdot f_{HF} \cdot L \cdot C \cdot R_{FB}}{V_{IN} \cdot (2 \cdot \pi \cdot f_{HF} \cdot \sqrt{L \cdot C} - 1)}$$

$$C_C = \frac{V_{IN} \cdot (2 \cdot \pi \cdot f_{HF} \cdot \sqrt{L \cdot C} - 1)}{(2 \cdot \pi)^2 \cdot f_0 \cdot f_{HF} \cdot (\sqrt{L \cdot C}) \cdot R_{FB} \cdot V_{PP}}$$

In the solutions to the compensation equations, there is a single degree of freedom. For the solutions presented in Equation 42, $R_{FB}$ is selected arbitrarily. The remaining compensation components are then selected according to Equation 42.

In Equation 42, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent-series resistance of the bulk output-filter capacitance; and $V_{PP}$ is the peak-to-peak sawtooth signal amplitude as described in the Electrical Specifications on page 6.

### *Output Filter Design*

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter limits the system transient response. The output capacitors must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, $\Delta I$, the load-current slew rate, di/dt, and the maximum allowable output-voltage deviation under transient loading, $\Delta V_{MAX}$. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output-voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount

$$\Delta V \approx ESL \cdot \frac{di}{dt} + ESR \cdot \Delta I \quad \text{(EQ. 43)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current (see “Interleaving” on page 10 and Equation 2), a voltage develops across the bulk capacitor ESR equal to $I_{C(P-P)}(ESR)$. Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{PP(MAX)}$, determines the lower limit on the inductance.

$$L \geq ESR \cdot \frac{\left(V_{IN} - N \cdot V_{OUT}\right) \cdot V_{OUT}}{f_S \cdot V_{IN} \cdot V_{PP(MAX)}} \quad \text{(EQ. 44)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than $\Delta V_{MAX}$. This places an upper limit on inductance.

Equation 45 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output-voltage deviation than the leading edge. Equation 46 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation, L is the per-channel inductance, C is the total output capacitance, and N is the number of active channels.

$$L \leq \frac{2 \cdot N \cdot C \cdot V_O}{(\Delta I)^2} \cdot \left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right] \quad \text{(EQ. 45)}$$

$$L \leq \frac{1.25 \cdot N \cdot C}{(\Delta I)^2} \cdot \left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right] \cdot \left(V_{IN} - V_O\right) \quad \text{(EQ. 46)}$$

### Switching Frequency

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper MOSFET loss calculation. These effects are outlined in “MOSFETs” on page 24, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output-voltage ripple. Choose the lowest switching frequency that allows the regulator to meet the transient-response requirements.

Switching frequency is determined by the selection of the frequency-setting resistor, $R_T$. Figure 24 and Equation 47 are provided to assist in selecting the correct value for $R_T$.

$$R_T = 10^{[10.61 - (1.035 \cdot \log(f_S))]} \quad \text{(EQ. 47)}$$

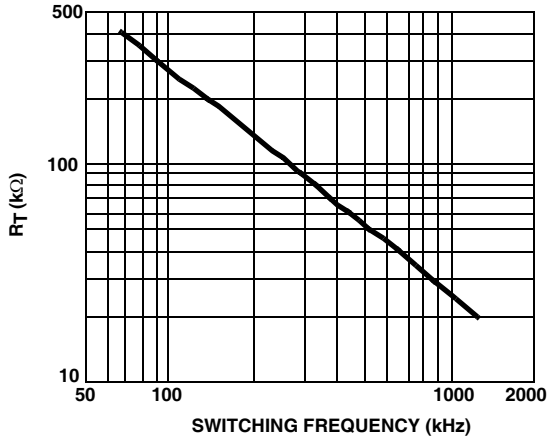



FIGURE 24. $R_T$ vs SWITCHING FREQUENCY

### Input Capacitor Selection

The input capacitors are responsible for sourcing the AC component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the ac component of the current drawn by the upper MOSFETs which is related to duty cycle and the number of active phases.

For a two-phase design, use Figure 25 to determine the input-capacitor RMS current requirement set by the duty cycle, maximum sustained output current ($I_O$), and the ratio of the peak-to-peak inductor current ($I_{L(P-P)}$) to $I_O$.

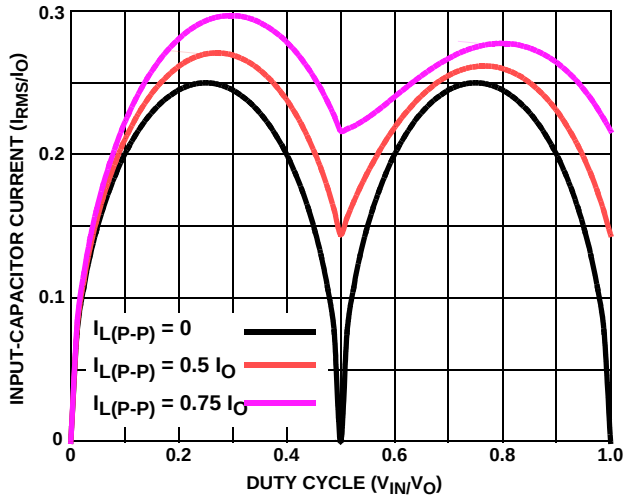



FIGURE 25. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR 2-PHASE CONVERTER

Select a bulk capacitor with a ripple current rating which will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25x greater than the maximum input voltage. Figure 26 provides the same input RMS current information for single-phase designs. Use the same approach for selecting the bulk capacitor type and number.

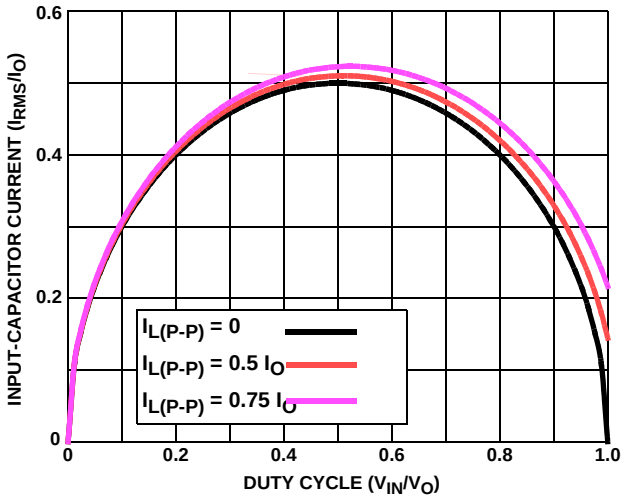



FIGURE 26. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR SINGLE-PHASE CONVERTER

Low capacitance, high-frequency ceramic capacitors are needed in addition to the input bulk capacitors to suppress leading and falling edge voltage spikes. The spikes result from the high current slew rate produced by the upper MOSFET turn on and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitics and maximize suppression.

## Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device overvoltage stress. Careful component selection, layout, and placement minimizes these voltage spikes. Consider, as an example, the turnoff transition of the upper PWM MOSFET. Prior to turnoff, the upper MOSFET was carrying channel current. During the turnoff, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes.

There are two sets of critical components in a DC/DC converter using a ISL6313B controller. The power components are the most critical because they switch large amounts of energy. Next are small signal components that connect to sensitive nodes or supply critical bypassing current and signal coupling.

The power components should be placed first, which include the MOSFETs, input and output capacitors, and the inductors. It is important to have a symmetrical layout for each power train, preferably with the controller located equidistant from each. Symmetrical layout allows heat to be dissipated equally across all power trains. Equidistant placement of the controller to the power trains it controls through the integrated drivers helps keep the gate drive traces equally short, resulting in equal trace impedances and similar drive capability of all sets of MOSFETs.

When placing the MOSFETs try to keep the source of the upper FETs and the drain of the lower FETs as close as thermally possible. Input Bulk capacitors should be placed close to the drain of the upper FETs and the source of the lower FETs. Locate the output inductors and output capacitors between the MOSFETs and the load. The high-frequency input and output decoupling capacitors (ceramic) should be placed as close as practicable to the decoupling target, making use of the shortest connection paths to any internal planes, such as vias to GND next or on the capacitor solder pad.

The critical small components include the bypass capacitors for VCC and PVCC, and many of the components surrounding the controller including the feedback network and current sense components. Locate the VCC/PVCC bypass capacitors as close to the ISL6313B as possible. It is especially important to locate the components associated with the feedback circuit close to their respective controller pins, since they belong to a high-impedance circuit loop, sensitive to EMI pick-up.

A multi-layer printed circuit board is recommended. Figure 27 shows the connections of the critical components for the converter. Note that capacitors $C_{XX(IN)}$ and $C_{XX(OUT)}$ could each represent numerous physical capacitors. Dedicate one solid layer, usually the one underneath the component side of the board, for a ground plane and make all critical component ground connections with vias to this layer.

Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminal to output inductors short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring.

### Routing UGATE, LGATE, and PHASE Traces

Great attention should be paid to routing the UGATE, LGATE, and PHASE traces since they drive the power train MOSFETs using short, high current pulses. It is important to size them as large and as short as possible to reduce their overall impedance and inductance. They should be sized to carry at least one ampere of current (0.02” to 0.05”). Going between layers with vias should also be avoided, but if so, use two vias for interconnection when possible.

Extra care should be given to the LGATE traces in particular since keeping their impedance and inductance low helps to significantly reduce the possibility of shoot-through. It is also important to route each channels UGATE and PHASE traces in as close proximity as possible to reduce their inductances.

### Current Sense Component Placement and Trace Routing

One of the most critical aspects of the ISL6313B regulator layout is the placement of the inductor DCR current sense components and traces. The R-C current sense components must be placed as close to their respective ISEN+ and ISEN- pins on the ISL6313B as possible.

The sense traces that connect the R-C sense components to each side of the output inductors should be routed on the bottom of the board, away from the noisy switching components located on the top of the board. These traces should be routed side by side, and they should be very thin traces. It’s important to route these traces as far away from any other noisy traces or planes as possible. These traces should pick up as little noise as possible.

### Thermal Management

For maximum thermal performance in high current, high switching frequency applications, connecting the thermal GND pad of the ISL6313B to the ground plane with multiple vias is recommended. This heat spreading allows the part to achieve its full thermal potential. It is also recommended that the controller be placed in a direct path of airflow if possible to help thermally manage the part.

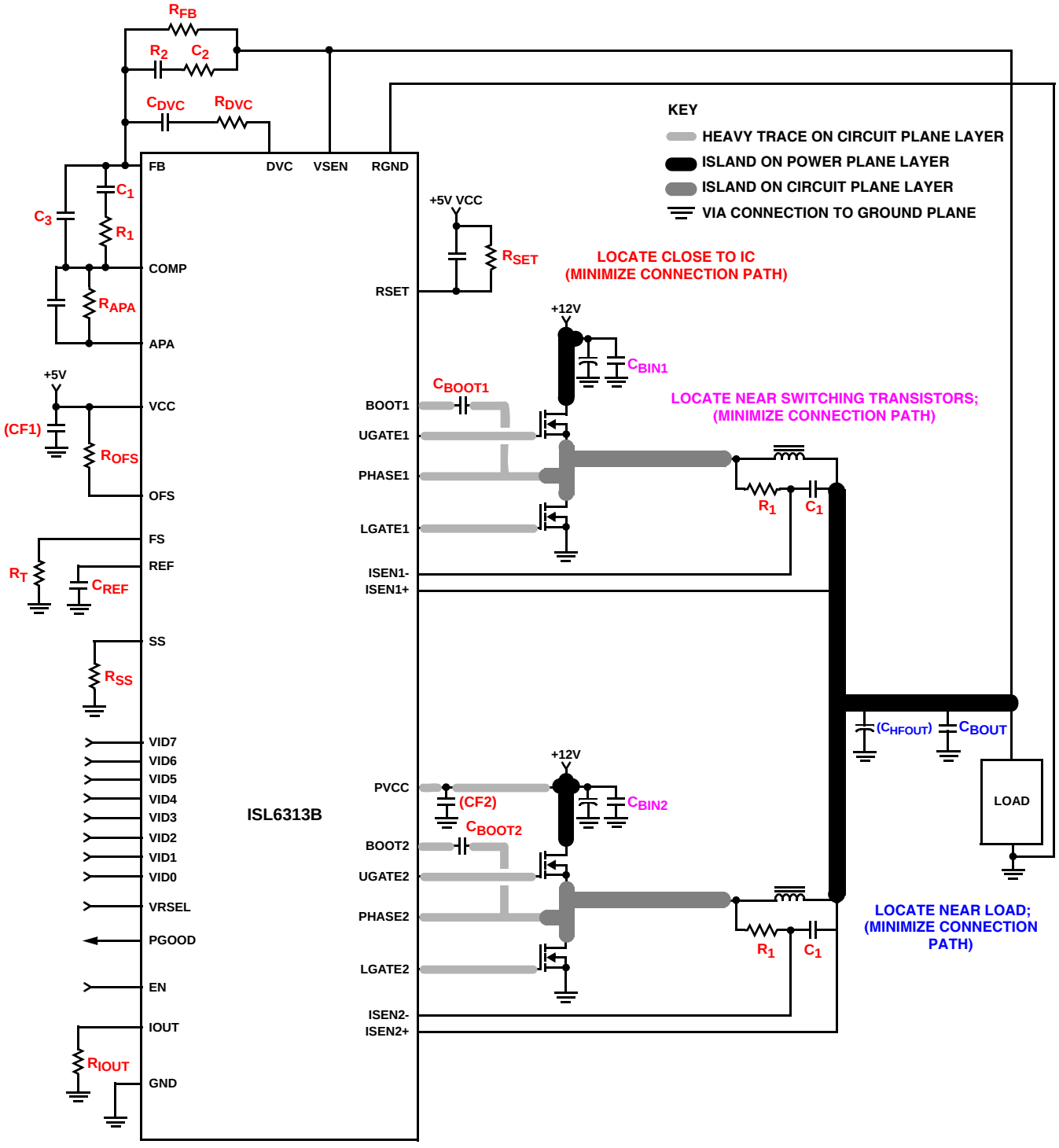


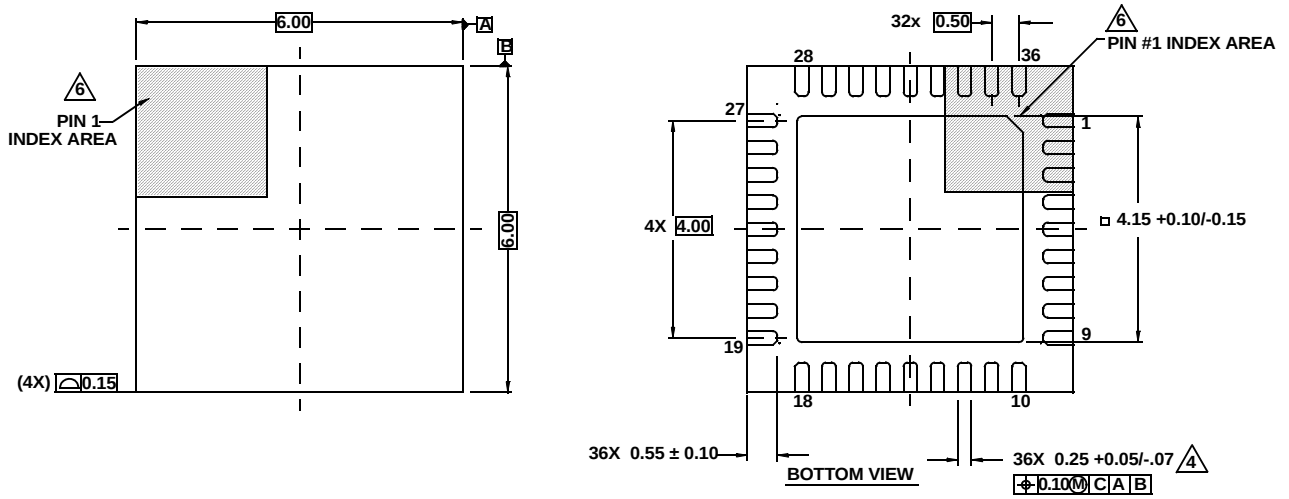

FIGURE 27. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

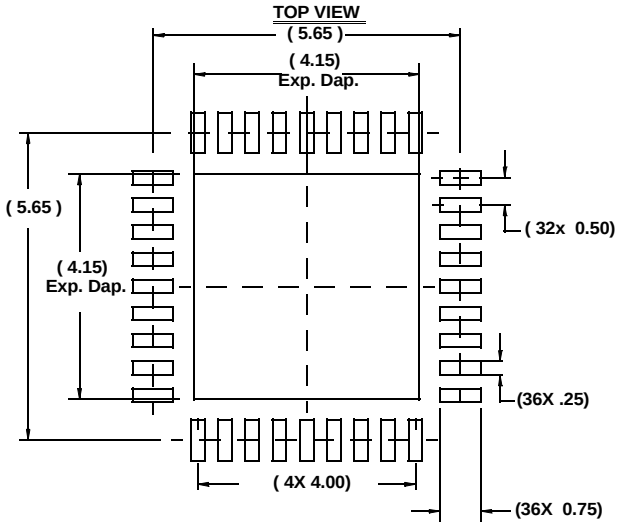
All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

# Package Outline Drawing

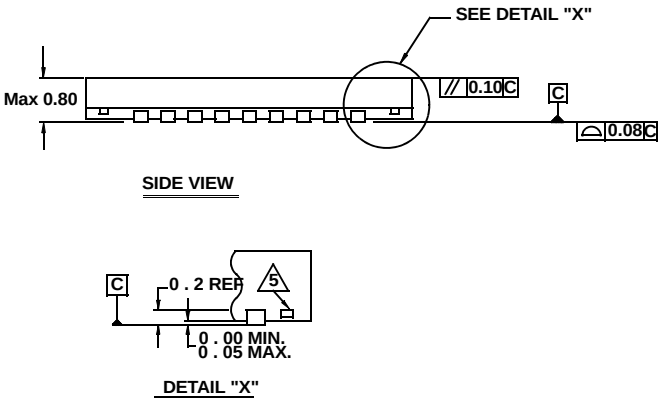
## L36.6x6

**36 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE**
**Rev 5, 08/08**




TYPICAL RECOMMENDED LAND PATTERN




1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.