

# HD74SSTV16857

## 1:1 14-bit SSTL\_2 Registered Buffer

REJ03D0830-0700  
 (Previous: ADE-205-336F)  
 Rev.7.00  
 Apr 07, 2006

### Description

The HD74SSTV16857 is a 14-bit registered buffer designed for 2.3 V to 2.7 V Vcc operation and LVCMOS reset ( $\overline{\text{RESET}}$ ) input / SSTL\_2 data (D) inputs and CLK input.

Data flow from D to Q is controlled by differential clock pins (CLK,  $\overline{\text{CLK}}$ ) and the  $\overline{\text{RESET}}$ . Data is triggered on the positive edge of the positive clock (CLK), and the negative clock ( $\overline{\text{CLK}}$ ) must be used to maintain noise margins. When  $\overline{\text{RESET}}$  is low, all registers are reset and all outputs are low.

To ensure defined outputs from the register before a stable clock has been supplied,  $\overline{\text{RESET}}$  must be held in the low state during power up.

### Features

- Supports LVCMOS reset ( $\overline{\text{RESET}}$ ) input / SSTL\_2 data (D) inputs and CLK input
- Differential SSTL\_2 (Stub series terminated logic) CLK signal
- Flow through architecture optimizes PCB layout
- Ordering Information

Part Name	Package Type	Package Code (Previous code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74SSTV16857TEL	TSSOP-48 pin	PTSP0048KA-A (TTP-48DBV)	T	EL (1,000 pcs / Reel)
HD74SSTV16857NEL	TVSOP-48 pin	PTSP0048LA-A (TTP-48DEV)	N	EL (1,000 pcs / Reel)

Note: Please consult the sales office for the above package availability.

### Function Table

Inputs				Output Q
$\overline{\text{RESET}}$	$\overline{\text{CLK}}$	CLK	D	
L	X	X	X	L
H	↓	↑	H	H
H	↓	↑	L	L
H	L or H	H or L	X	$Q_0^{*1}$

H : High level

L : Low level

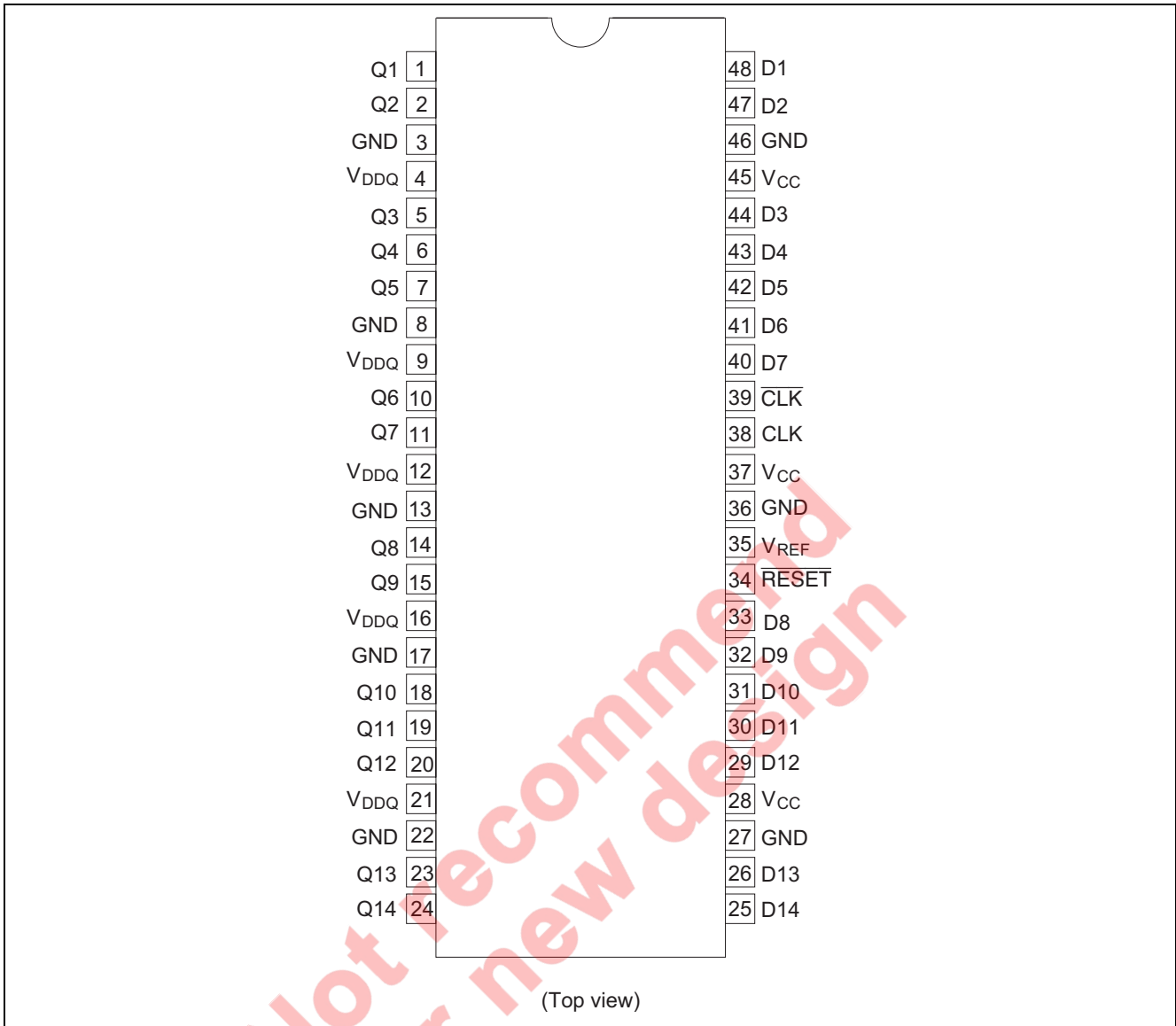
X : Immaterial

↑ : Low to high transition

↓ : High to low transition

Note: 1. Output level before the indicated steady state input conditions were established.

Pin Arrangement



## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$ or $V_{DDQ}$	-0.5 to 3.6	V	
Input voltage <sup>*1</sup>	$V_I$	-0.5 to $V_{DDQ}+0.5$	V	
Output voltage <sup>*1,2</sup>	$V_O$	-0.5 to $V_{DDQ}+0.5$	V	
Input clamp current	$I_{IK}$	±50	mA	$V_I < 0$ or $V_I > V_{CC}$
Output clamp current	$I_{OK}$	±50	mA	$V_O < 0$ or $V_O > V_{DDQ}$
Continuous output current	$I_O$	±50	mA	$V_O = 0$ to $V_{DDQ}$
$V_{CC}$ , $V_{DDQ}$ or GND current / pin	$I_{CC}$ , $I_{DDQ}$ or $I_{GND}$	±100	mA	
Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air)	$P_T$	115	$^\circ\text{C} / \text{W}$	TSSOP
Storage temperature	$T_{stg}$	-65 to +150	$^\circ\text{C}$	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

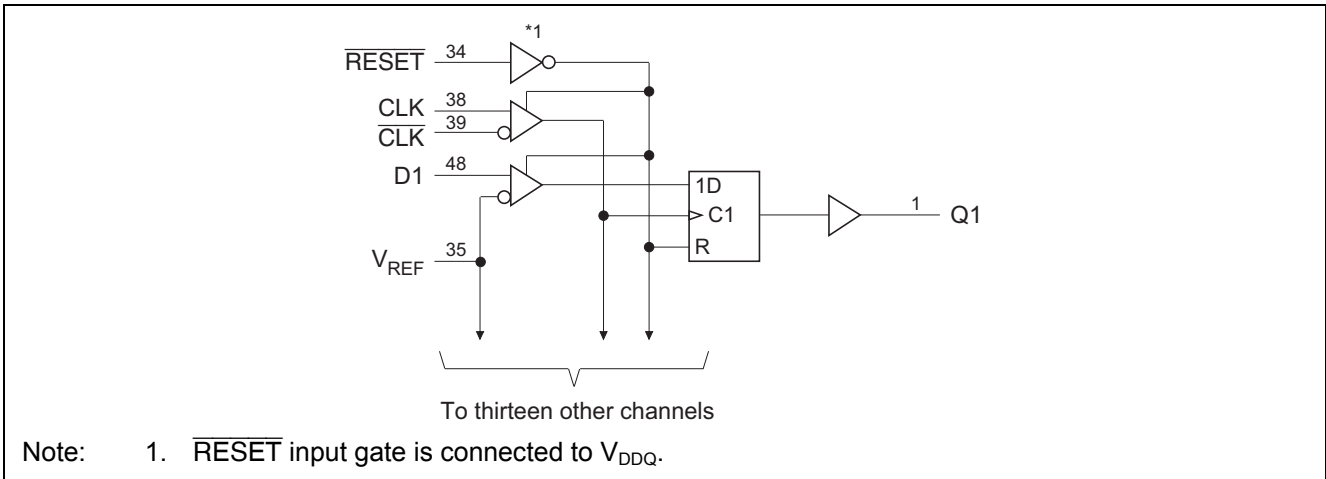
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This current will flow only when the output is in the high state and  $V_O > V_{DDQ}$ .

## Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions	
Supply voltage	$V_{CC}$	$V_{DDQ}$	2.5	2.7	V		
Output supply voltage	$V_{DDQ}$	2.3	2.5	2.7	V		
Reference voltage	$V_{REF}$	1.15	1.25	1.35	V	$V_{REF} = 0.5 \times V_{DDQ}$	
Termination voltage	$V_{TT}$	$V_{REF}-40$ mV	$V_{REF}$	$V_{REF}+40$ mV	V		
Input voltage	$V_I$	0	—	$V_{CC}$	V		
AC high level input voltage	$V_{IH}$	$V_{REF}+310$ mV	—	—	V	D	
AC low level input voltage	$V_{IL}$	—	—	$V_{REF}-310$ mV	V	D	
DC high level input voltage	$V_{IH}$	$V_{REF}+150$ mV	—	—	V	D	
DC low level input voltage	$V_{IL}$	—	—	$V_{REF}-150$ mV	V	D	
High level input voltage	$V_{IH}$	1.7	—	$V_{DDQ}+0.3$	V	$\overline{\text{RESET}}$	
Low level input voltage	$V_{IL}$	-0.3	—	0.7	V	$\overline{\text{RESET}}$	
Differential input voltage	(Common mode range)	$V_{CMR}$	0.97	—	1.53	V	CLK, $\overline{\text{CLK}}$
	(Minimum peak to peak input)	$V_{PP}$	360	—	—	mV	CLK, $\overline{\text{CLK}}$
High level output current	$I_{OH}$	—	—	-20	mA		
Low level output current	$I_{OL}$	—	—	20	mA		
Operating temperature	$T_a$	0	—	70	$^\circ\text{C}$		

Note: The  $\overline{\text{RESET}}$  input of the device must be held at  $V_{DDQ}$  or GND to ensure proper device operation. The differential inputs must not be floating, unless  $\overline{\text{RESET}}$  is low.

Logic Diagram



Electrical Characteristics

Item	Symbol	$V_{CC}$ (V)	Min	Typ	Max	Unit	Test Conditions
Input diode voltage	$V_{IK}$	2.3	—	—	-1.2	V	$I_{IN} = -18 \text{ mA}$
Output voltage	$V_{OH}$	2.3 to 2.7	$V_{CC}-0.2$	—	—	V	$I_{OH} = -100 \mu\text{A}$
		2.3	1.95	—	$V_{DDQ}$	$I_{OH} = -16 \text{ mA}$	
	$V_{OL}$	2.3 to 2.7	—	—	0.2		$I_{OL} = 100 \mu\text{A}$
		2.3	0	—	0.35		$I_{OL} = 16 \text{ mA}$
Input current (All inputs)	$I_{IN}$	2.7	—	—	$\pm 5$	$\mu\text{A}$	$V_{IN} = 2.7 \text{ V or } 0$
Quiescent supply current	$I_{CC}^{*2}$	2.7	—	—	45	mA	$V_{IN} = V_{IH(AC)} \text{ or } V_{IL(AC)}, I_O = 0$
Standby current	$I_{CC}(\text{stdy})$	2.7	—	—	10	$\mu\text{A}$	$\overline{\text{RESET}} = \text{GND}$
Dynamic operating clock only	$I_{CCD}^{*2}$	2.7	—	—	90	$\mu\text{A}/$ clock MHz	$\overline{\text{RESET}} = V_{CC}$ , $V_I = V_{IH(AC)} \text{ or } V_{IL(AC)}$ , CLK and $\overline{\text{CLK}}$ switching 50% duty cycle
Dynamic operating per each data input	$I_{CCD}^{*2}$	2.7	—	—	15	$\mu\text{A}/$ clock MHz/ data input	$\overline{\text{RESET}} = V_{CC}$ , $V_I = V_{IH(AC)} \text{ or } V_{IL(AC)}$ , CLK and $\overline{\text{CLK}}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.
Output high <sup>*3</sup>	$r_{OH}$	2.3 to 2.7	7	—	$22^{*4}$	$\Omega$	$I_{OH} = -20 \text{ mA}$
Output low <sup>*3</sup>	$r_{OL}$	2.3 to 2.7	7	—	$22^{*4}$	$\Omega$	$I_{OL} = 20 \text{ mA}$
$ r_{OH} - r_{OL} $ each separate bit <sup>*3</sup>	$r_{O(\Delta)}$	2.5	—	—	4	$\Omega$	$I_O = 20 \text{ mA}, T_a = 25^\circ\text{C}$
Input capacitance	Data inputs	$C_{IN}$	2.5 <sup>*1</sup>	—	3.5	pF	$V_I = V_{REF} \pm 310 \text{ mV}$
	CLK and $\overline{\text{CLK}}$			—	3.5		$V_{CMR} = 1.25 \text{ V}, V_{PP} = 360 \text{ mV}$
	$\overline{\text{RESET}}$			3.0	—		$V_I = V_{CC} \text{ or } \text{GND}$

- Notes: 1. All typical values are at  $V_{CC} = 2.5 \text{ V}, T_a = 25^\circ\text{C}$ .  
 2. Total  $I_{CC}(\text{max}) = I_{CC} + \{I_{CCD}(\text{clock}) \times f(\text{clock})\} + \{I_{CCD}(\text{Data}) \times 1/2f(\text{clock}) \times 14\}$   
 3. This is effective in the case that it did terminate by resistance.  
 4. See figure. 1, 2

### Switching Characteristics

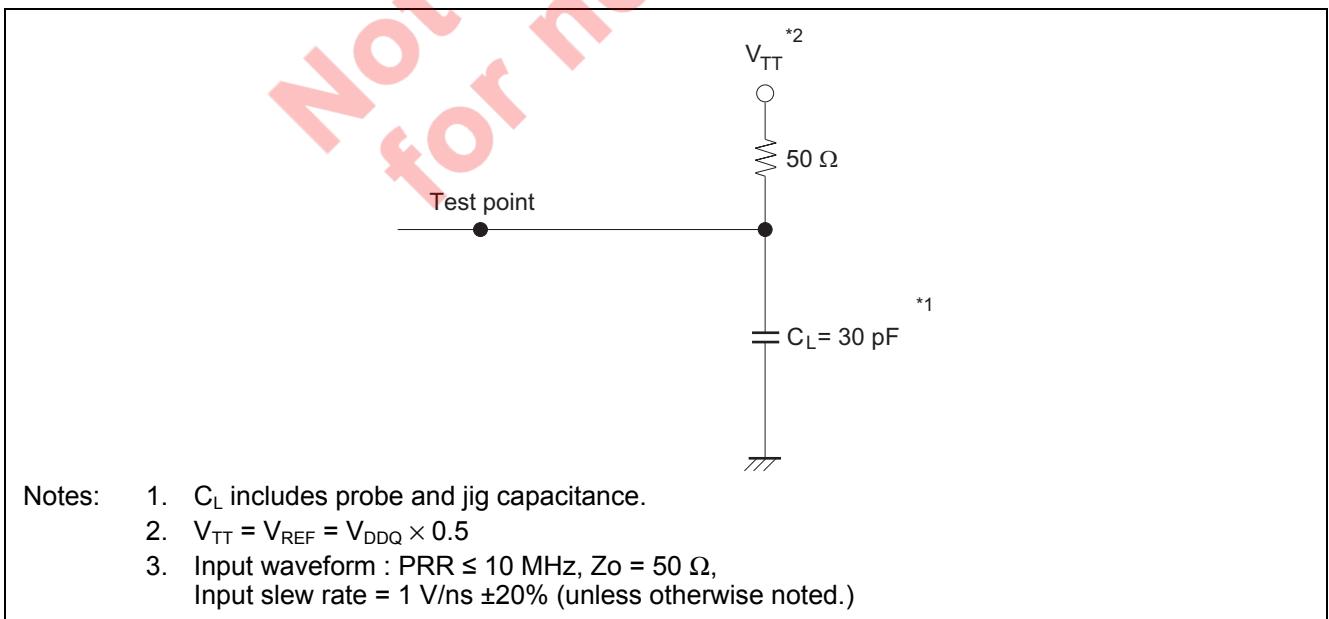
Item	Symbol	V <sub>CC</sub> = 2.5 ± 0.2 V		Unit	Test Condition	
		Min	Max			
Clock frequency <sup>*1</sup>	f <sub>clock</sub>	—	200	MHz		
Setup time	Fast slew rate <sup>*4, 6</sup>	t <sub>su</sub>	0.75	—	ns	Data before CLK↑, $\overline{\text{CLK}}\downarrow$
	Slow slew rate <sup>*5, 6</sup>		0.9	—		
Hold time	Fast slew rate <sup>*4, 6</sup>	t <sub>h</sub>	0.75	—	ns	Data after CLK↑, $\overline{\text{CLK}}\downarrow$
	Slow slew rate <sup>*5, 6</sup>		0.9	—		
Differential inputs active time	t <sub>act</sub>	22	—	ns	Data inputs must be low after $\overline{\text{RESET}}$ high.	
Differential inputs inactive time	t <sub>inact</sub>	22	—	ns	Data and clock inputs must be held at valid levels (not floating) after $\overline{\text{RESET}}$ low.	
Pulse width	t <sub>w</sub>	2.5	—	ns	CLK, $\overline{\text{CLK}}$ "H" or "L"	
Output slew <sup>*3</sup>	t <sub>SL</sub>	1	4	volt/ns		

(C<sub>L</sub> = 30 pF, R<sub>L</sub> = 50 Ω, V<sub>REF</sub> = V<sub>TT</sub> = V<sub>DDQ</sub> × 0.5)

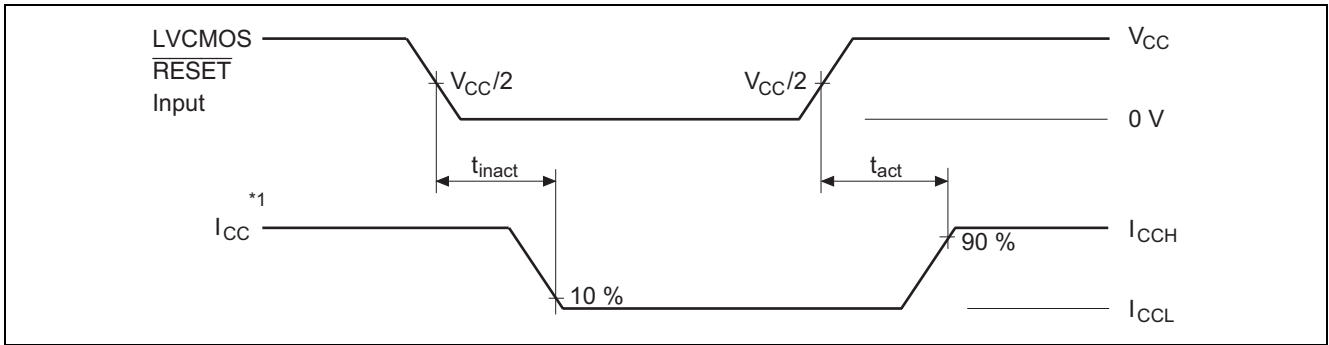
Item	Symbol	V <sub>CC</sub> = 2.5 ± 0.2 V			Unit	FROM (Input)	TO (Output)
		Min	Typ	Max			
Maximum clock frequency	f <sub>max</sub>	200	—	—	MHz		
Propagation delay time <sup>*2</sup>	t <sub>PLH</sub> , t <sub>PHL</sub>	1.1	—	2.8	ns	CLK, $\overline{\text{CLK}}$	Q
	t <sub>PHL</sub>	—	—	5.0		$\overline{\text{RESET}}$	Q

- Notes:
1. Although the clock is differential, all timing is relative to CLK going high and  $\overline{\text{CLK}}$  going low.
  2. This timing relationship is specified into test load (see waveforms – 3, 4) with all of the outputs switching.
  3. Assumes into an equivalent, distributed load to the address net structure defined in the application information provided in this specification.
  4. For data signal input slew rate ≥ 1 V/ns.
  5. For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns.
  6. CLK,  $\overline{\text{CLK}}$  signals input slew rates are ≥ 1 V/ns.

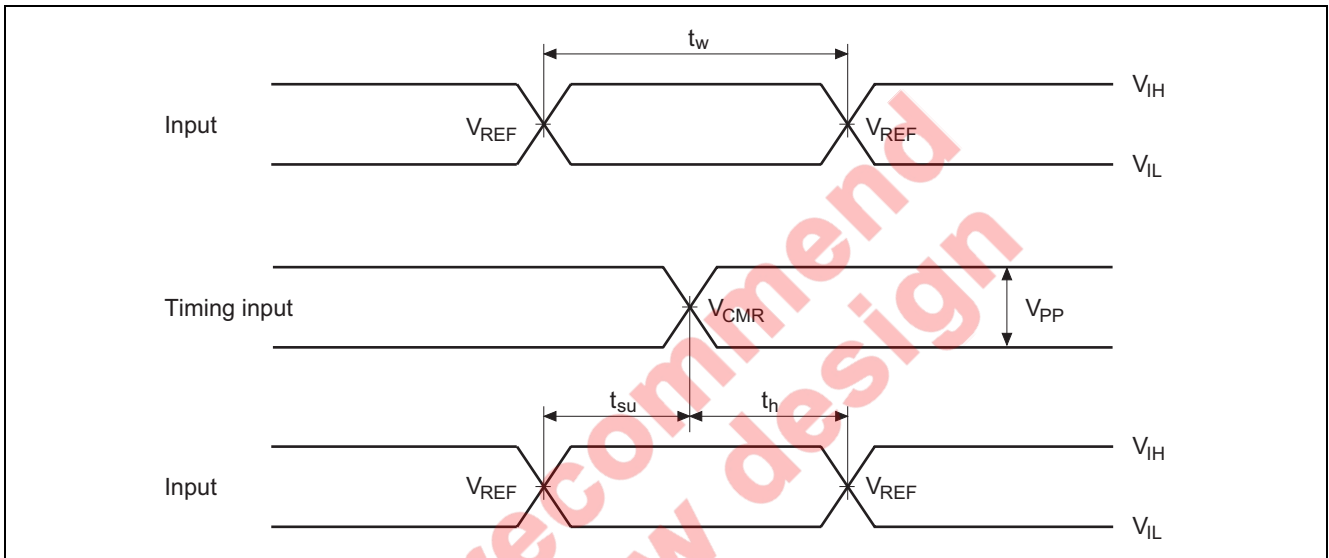
### Test Circuit



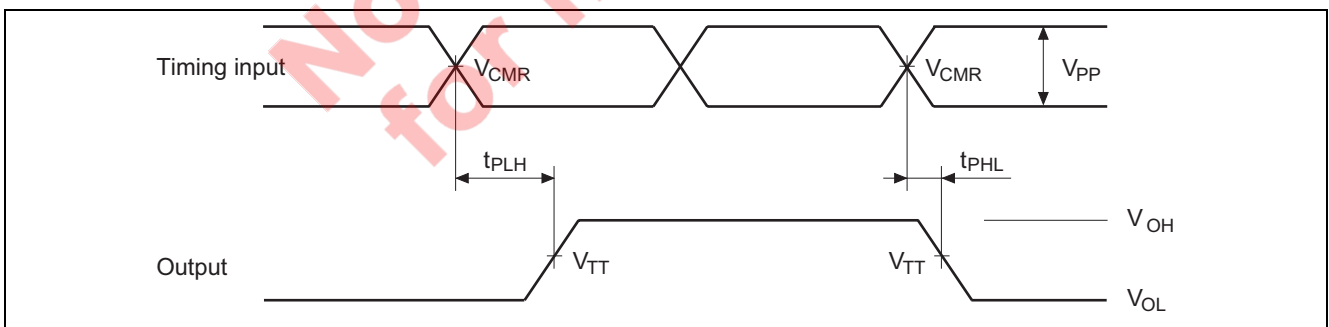
Waveforms – 1



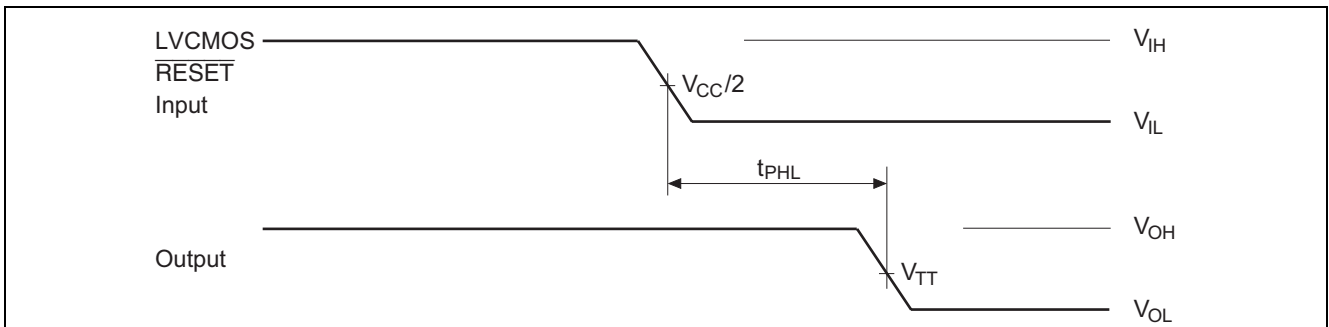
Waveforms – 2



Waveforms – 3



Waveforms – 4



- Notes:
1.  $I_{CC}$  tested with clock and data inputs held at  $V_{CC}$  or GND, and  $I_O = 0$  mA.
  2. All input pulses are supplied by generators having the following characteristics :  
 $PRR \leq 10$  MHz,  $Z_o = 50 \Omega$ , input slew rate =  $1$  V/ns  $\pm 20\%$  (unless otherwise specified).
  3. The outputs are measured one at a time with one transition per measurement.
  4.  $V_{TT} = V_{REF} = V_{DDQ}/2$
  5.  $V_{IH} = V_{REF} + 310$  mV (AC voltage levels) for differential inputs.  $V_{IH} = V_{CC}$  for LVC MOS input.
  6.  $V_{IL} = V_{REF} - 310$  mV (AC voltage levels) for differential inputs.  $V_{IL} = GND$  for LVC MOS input.
  7.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$

Not recommended  
for new design

Application Data

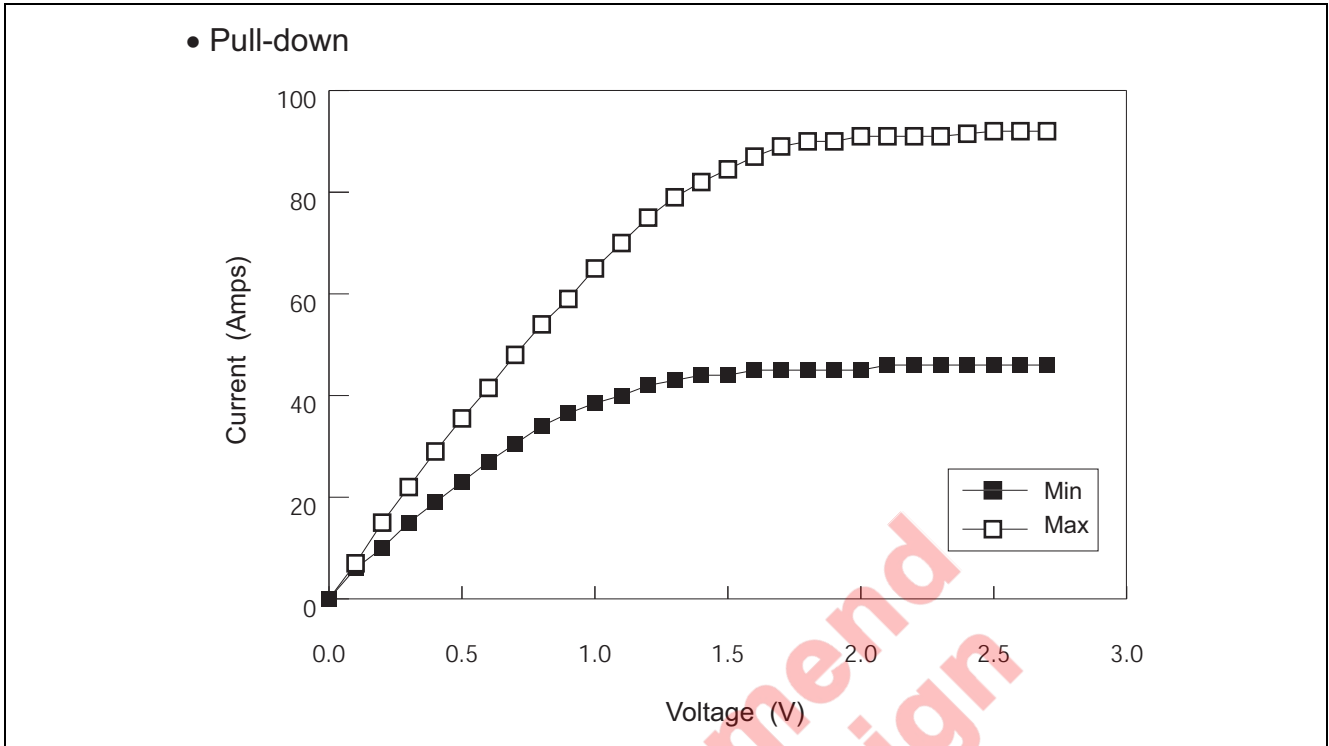


Figure . 1

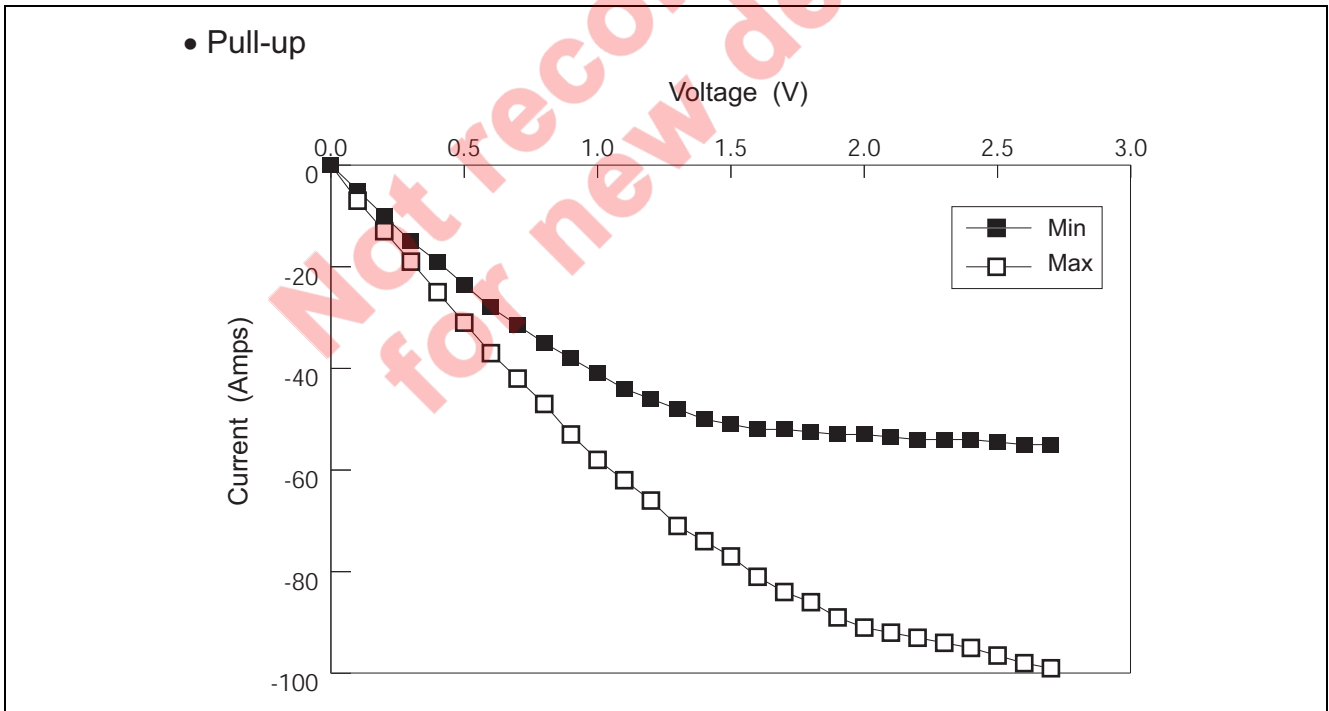


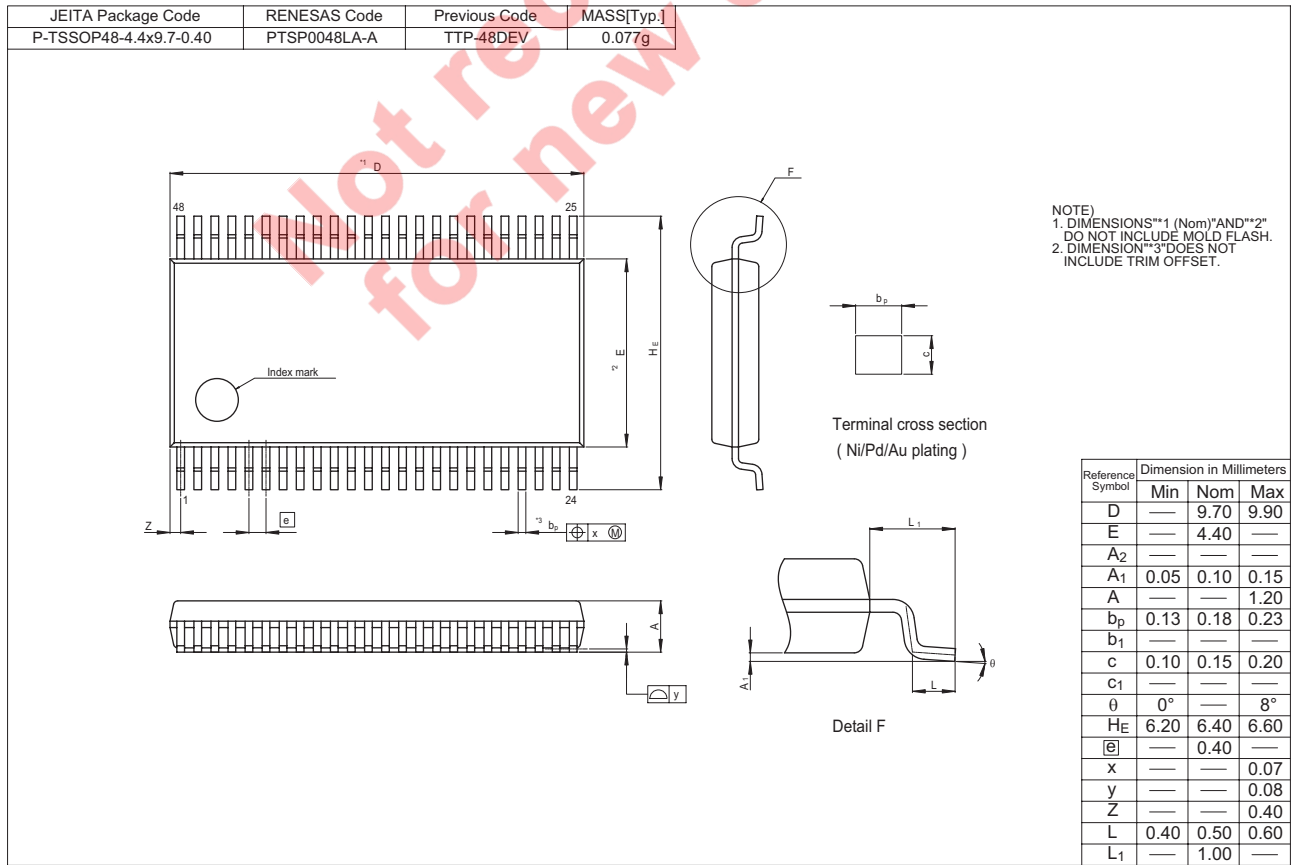
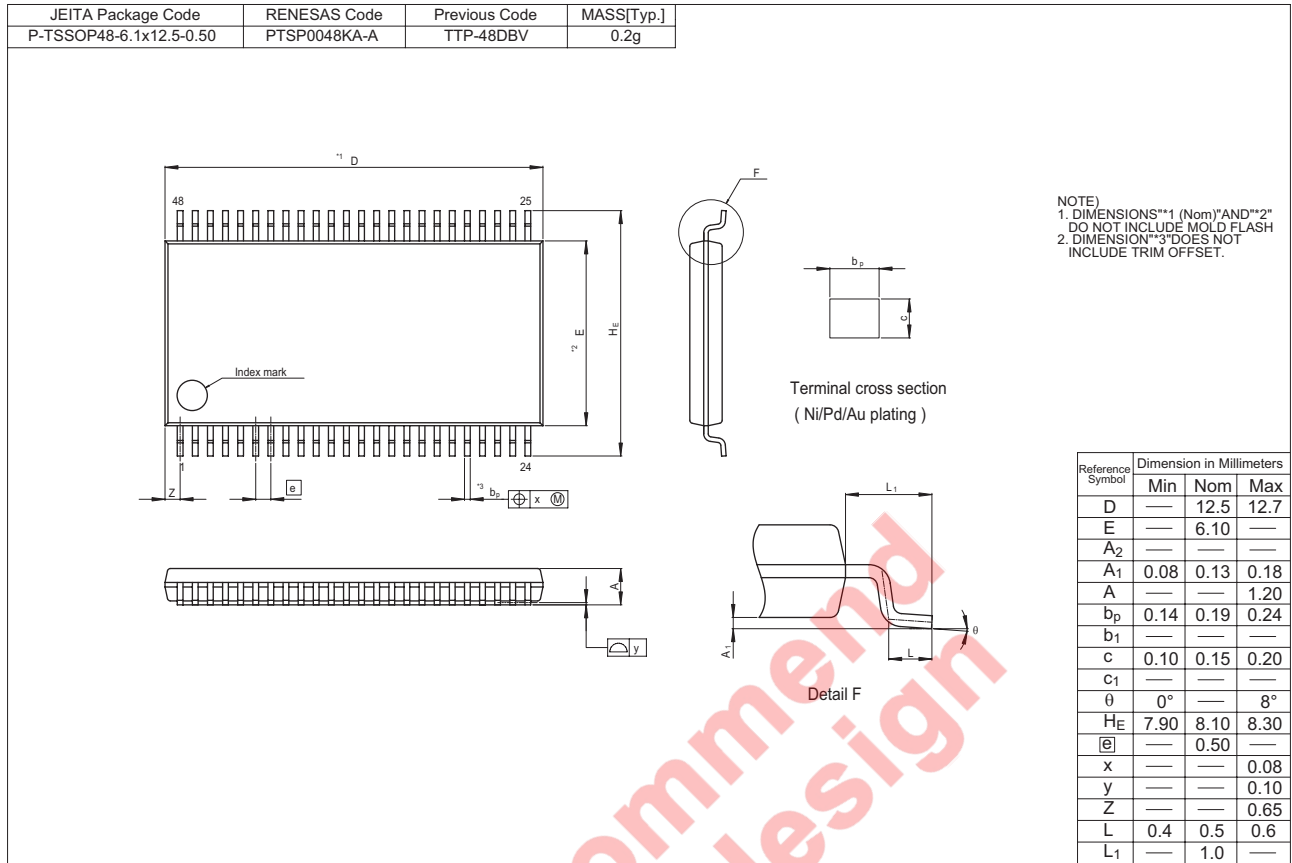
Figure . 2



## Curve Data

Voltage (V)	Pull-down		Pull-up	
	I (mA)	I (mA)	I (mA)	I (mA)
	Min	Max	Min	Max
0.0	0	0	0	0
0.1	6	7	-5	-7
0.2	10	15	-10	-13
0.3	15	22	-15	-19
0.4	19	29	-19	-25
0.5	23	35.5	-23.5	-31
0.6	27	41.5	-28	-37
0.7	30.5	48	-31.5	-42
0.8	34	54	-35	-47
0.9	36.5	59	-38	-53
1.0	38.5	65	-41	-58
1.1	40	70	-44	-62
1.2	42	75	-46	-66
1.3	43	79	-48	-71
1.4	44	82	-50	-74
1.5	44	84.5	-51	-77
1.6	45	87	-52	-81
1.7	45	89	-52	-84
1.8	45	90	-52.5	-86
1.9	45	90	-53	-89
2.0	45	91	-53	-91
2.1	46	91	-53.5	-92
2.2	46	91	-54	-93
2.3	46	91	-54	-94
2.4	46	91.5	-54	-95
2.5	46	92	-54.5	-96.5
2.6	46	92	-55	-98
2.7	46	92	-55	-99

Package Dimensions



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