Isolated Sigma-Delta Modulator

AD7401A

FEATURES

20 MHz maximum external clock rate
Second-order modulator
16 bits, no missing codes
±2 LSB INL typical at 16 bits
1 µV/°C typical offset drift
On-board digital isolator
On-board reference
±250 mV analog input range
Low power operation: 17 mA typical at 5.5 V
–40°C to +125°C operating range
16-lead SOIC package
Internal clock version: AD7400A
Safety and regulatory approvals
- **UL recognition**
  - **3750 V rms for 1 minute per UL 1577**
- **CSA Component Acceptance Notice #5A**
- **VDE Certificate of Conformity**
  - **DIN V VDE V 0884-10 (VDE V 0884-10):2006-12**
  - **V_{IORM} = 891 V peak**

APPLICATIONS

AC motor controls
Shunt current monitoring
Data acquisition systems
Analog-to-digital and opto-isolator replacements

GENERAL DESCRIPTION

The AD7401A[1] is a second-order, sigma-delta (Σ-Δ) modulator that converts an analog input signal into a high speed, 1-bit data stream with on-chip digital isolation based on Analog Devices, Inc., *i*Coupler® technology. The AD7401A operates from a 5 V power supply and accepts a differential input signal of ±250 mV (±320 mV full scale). The analog input is continuously sampled by the analog modulator, eliminating the need for external sample-and-hold circuitry. The input information is contained in the output stream as a density of ones with a data rate up to 20 MHz. The original information can be reconstructed with an appropriate digital filter. The serial I/O can use a 5 V or a 3 V supply (V_{DD2}).

The serial interface is digitally isolated. High speed CMOS, combined with monolithic air core transformer technology, means the on-chip isolation provides outstanding performance characteristics, superior to alternatives such as optocoupler devices. The part contains an on-chip reference. The AD7401A is offered in a 16-lead SOIC and has an operating temperature range of –40°C to +125°C.

FUNCTIONAL BLOCK DIAGRAM

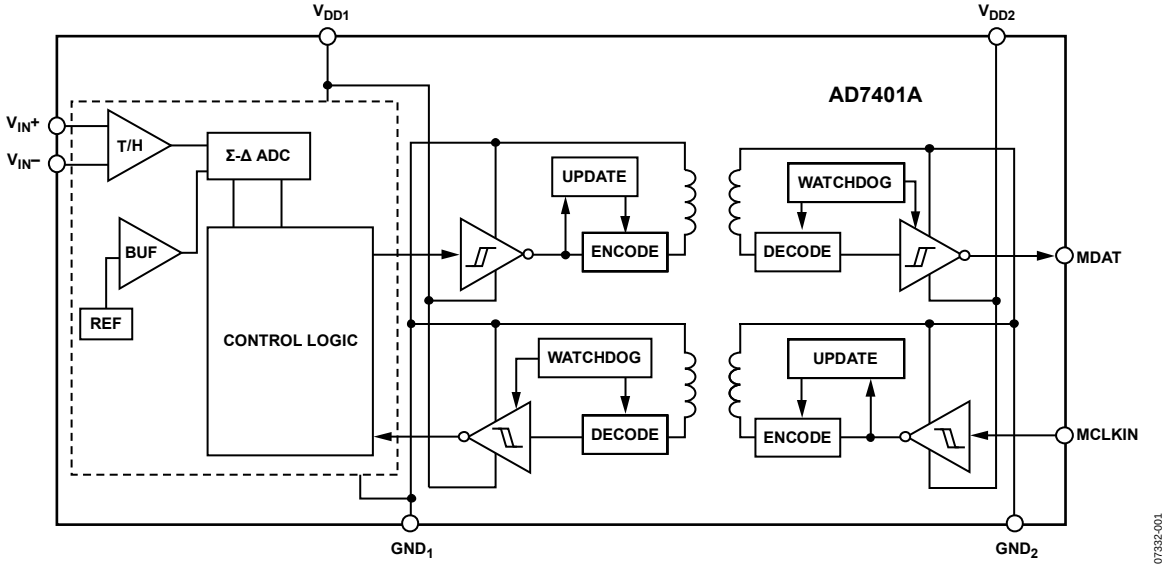

Figure 1.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329. Other patents pending.

Rev. 0

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REVISION HISTORY

7/08—Revision 0: Initial Version

SPECIFICATIONS

V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 3 V to 5.5 V, $V_{IN}+$ = −200 mV to +200 mV, and $V_{IN}-$ = 0 V (single-ended); T_A = −40°C to +125°C, f_{MCLKIN} = 16 MHz maximum,[1] tested with sinc3 filter, 256 decimation rate, as defined by Verilog code, unless otherwise noted.

Table 1.

	Y Version[1, 2]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
STATIC PERFORMANCE					
Resolution	16			Bits	Filter output truncated to 16 bits
Integral Nonlinearity (INL)[3]		±1.5	±7	LSB	$V_{IN}+$ = ±200 V, T_A = −40°C to +85°C, f_{MCLKIN} = 20 MHz max[1]
		±2	±13	LSB	$V_{IN}+$ = ±250 V, T_A = −40°C to +85°C, f_{MCLKIN} = 20 MHz max[1]
		±1.5	±11	LSB	$V_{IN}+$ = ±200 V, T_A = −40°C to +125°C, f_{MCLKIN} = 20 MHz max[1]
		±2	±46	LSB	$V_{IN}+$ = ±250 V, T_A = −40°C to +125°C, f_{MCLKIN} = 20 MHz max[1]
Differential Nonlinearity (DNL)[3]			±0.9	LSB	Guaranteed no missed codes to 16 bits, f_{MCLKIN} = 20 MHz max,[1] $V_{IN}+$ = −250 mV to +250 mV
Offset Error[3]		±.025	±0.5	mV	f_{MCLKIN} = 20 MHz max,[1] $V_{IN}+$ = −250 mV to +250 mV
Offset Drift vs. Temperature[3]		1	3.5	µV/°C	
Offset Drift vs. V_{DD1}[3]		120		µV/V	
Gain Error[3]		0.07	±1.5	mV	
		±1		mV	f_{MCLKIN} = 20 MHz max,[1] $V_{IN}+$ = −250 mV to +250 mV
Gain Error Drift vs. Temperature[3]		23		µV/°C	
Gain Error Drift vs. V_{DD1}[3]		110		µV/V	
ANALOG INPUT					
Input Voltage Range		±200	±250	mV	For specified performance; full range ±320 mV
Dynamic Input Current		±13	±18	µA	$V_{IN}+$ = 500 mV, $V_{IN}-$ = 0 V, f_{MCLKIN} = 20 MHz max[1]
		±10	±15	µA	$V_{IN}+$ = 400 mV, $V_{IN}-$ = 0 V, f_{MCLKIN} = 20 MHz max[1]
		0.08		µA	$V_{IN}+$ = 0 V, $V_{IN}-$ = 0 V, f_{MCLKIN} = 20 MHz max[1]
DC Leakage Current		±0.01	±0.6	µA	
Input Capacitance		10		pF	
DYNAMIC SPECIFICATIONS					$V_{IN}+$ = 5 kHz
Signal-to-(Noise + Distortion) Ratio (SINAD)[3]	76	82		dB	$V_{IN}+$ = ±200 V, T_A = −40°C to +85°C, f_{MCLKIN} = 5 MHz to 20 MHz[1]
	71	82		dB	$V_{IN}+$ = ±250 V, T_A = −40°C to +85°C, f_{MCLKIN} = 5 MHz to 20 MHz[1]
	72	82		dB	$V_{IN}+$ = ±200 V, T_A = −40°C to +125°C, f_{MCLKIN} = 5 MHz to 20 MHz[1]
		82		dB	$V_{IN}+$ = ±250 V, T_A = −40°C to +125°C, f_{MCLKIN} = 5 MHz to 20 MHz[1]
Signal-to-Noise Ratio (SNR)[3]	81	83		dB	$V_{IN}+$ = ±250 V, T_A = −40°C to +125°C, f_{MCLKIN} = 5 MHz to 20 MHz[1]
	80	82		dB	$V_{IN}+$ = ±200 V, T_A = −40°C to +125°C, f_{MCLKIN} = 5 MHz to 20 MHz[1]
Total Harmonic Distortion (THD)[3]		−90		dB	f_{MCLKIN} = 20 MHz max[1], $V_{IN}+$ = −250 mV to +250 mV
Peak Harmonic or Spurious Noise (SFDR)[3]		−92		dB	
Effective Number of Bits (ENOB)[3]		13.3	12.3	Bits	
Isolation Transient Immunity[3]	25	30		kV/µs	
LOGIC INPUTS					
Input High Voltage, V_{IH}	0.8 × V_{DD2}			V	
Input Low Voltage, V_{IL}			0.2 × V_{DD2}	V	
Input Current, I_{IN}			±0.5	µA	
Floating State Leakage Current			1	µA	
Input Capacitance, C_{IN}[4]			10	pF	

Parameter	Y Version[1, 2] Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DD2} − 0.1			V	I_O = −200 μA
Output Low Voltage, V_{OL}			0.4	V	I_O = +200 μA
POWER REQUIREMENTS					
V_{DD1}	4.5		5.5	V	
V_{DD2}	3		5.5	V	
I_{DD1}[5]		10	12	mA	V_{DD1} = 5.5 V
I_{DD2}[6]		7	9	mA	V_{DD2} = 5.5 V
		3	4	mA	V_{DD2} = 3.3 V
Power Dissipation		93.5		mW	V_{DD1} = V_{DD2} = 5.5 V

[1] For f_{MCLK} > 16 MHz to 20 MHz, mark space ratio is 48/52 to 52/48, V_{DD1} = V_{DD2} = 5 V ± 5%, and T_A = −40°C to +85°C.
[2] All voltages are relative to their respective ground.
[3] See the Terminology section.
[4] Sample tested during initial release to ensure compliance.
[5] See Figure 15.
[6] See Figure 17.

TIMING SPECIFICATIONS

V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 3 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter[1]	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{MCLKIN}[2, 3]	20	MHz max	Master clock input frequency
	5	MHz min	Master clock input frequency
t_1[4]	25	ns max	Data access time after MCLKIN rising edge
t_2[4]	15	ns min	Data hold time after MCLKIN rising edge
t_3	0.4 × t_{MCLKIN}	ns min	Master clock low time
t_4	0.4 × t_{MCLKIN}	ns min	Master clock high time

[1] Sample tested during initial release to ensure compliance.
[2] Mark space ratio for clock input is 40/60 to 60/40 for f_{MCLKIN} ≤ 16 MHz and 48/52 to 52/48 for 16 MHz < f_{MCLKIN} < 20 MHz.
[3] V_{DD1} = V_{DD2} = 5 V ± 5% for f_{MCLKIN} > 16 MHz to 20 MHz.
[4] Measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.8 V or 2.0 V.

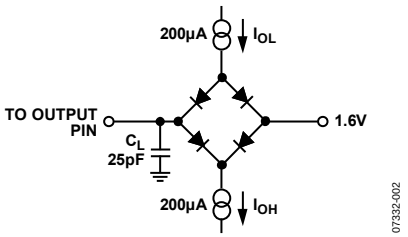

Figure 2. Load Circuit for Digital Output Timing Specifications

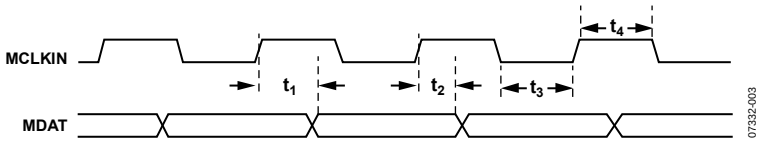

Figure 3. Data Timing

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 3.

Parameter	Symbol	Value	Unit	Conditions
Input-to-Output Momentary Withstand Voltage	V_{ISO}	3750 min	V	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.46 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.1 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table I)

REGULATORY INFORMATION

Table 4.

UL[1]	CSA	VDE[2]
Recognized Under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
3750 V rms Isolation Voltage	Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 630 V rms maximum working voltage	Reinforced insulation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12, 891 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each AD7401A is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 second (current leakage detection limit = 7.5 µA).
[2] In accordance with DIN V VDE V 0884-10, each AD7400A is proof tested by applying an insulation test voltage ≥1671V peak for 1 sec (partial discharge detection limit = 5 pC).

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits.

Table 5.

Description	Symbol	Characteristic	Unit
INSTALLATION CLASSIFICATION PER DIN VDE 0110			
For Rated Mains Voltage ≤ 300 V rms		I to IV	
For Rated Mains Voltage ≤ 450 V rms		I to II	
For Rated Mains Voltage ≤ 600 V rms		I to II	
CLIMATIC CLASSIFICATION		40/105/21	
POLLUTION DEGREE (DIN VDE 0110, TABLE 1)		2	
MAXIMUM WORKING INSULATION VOLTAGE	V_{IORM}	891	V peak
INPUT-TO-OUTPUT TEST VOLTAGE, METHOD B1			
$V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1671	V peak
INPUT-TO-OUTPUT TEST VOLTAGE, METHOD A	V_{PR}		
After Environmental Test Subgroup 1		1426	V peak
$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, Partial Discharge < 5 pC			
After Input and/or Safety Test Subgroup 2/ Safety Test Subgroup 3		1069	V peak
$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, Partial Discharge < 5 pC			
HIGHEST ALLOWABLE OVERVOLTAGE (TRANSIENT OVERVOLTAGE, t_{TR} = 10 sec)	V_{TR}	6000	V peak
SAFETY-LIMITING VALUES (MAXIMUM VALUE ALLOWED IN THE EVENT OF A FAILURE, SEE Figure 4)			
Case Temperature	T_S	150	°C
Side 1 Current	I_{S1}	265	mA
Side 2 Current	I_{S2}	335	mA
INSULATION RESISTANCE AT T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

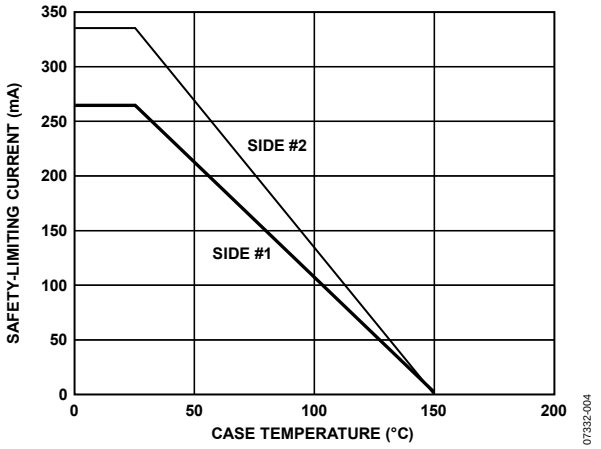

Figure 4. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN V VDE V 0884-10

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. All voltages are relative to their respective ground.

Table 6.

Parameter	Rating
V_{DD1} to GND_1	−0.3 V to +6.5 V
V_{DD2} to GND_2	−0.3 V to +6.5 V
Analog Input Voltage to GND_1	−0.3 V to V_{DD1} + 0.3 V
Digital Input Voltage to GND_2	−0.3 V to V_{DD1} + 0.5 V
Output Voltage to GND_2	−0.3 V to V_{DD2} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
SOIC Package	
θ_{JA} Thermal Impedance[2]	89.2°C/W
θ_{JC} Thermal Impedance[2]	55.6°C/W
Resistance (Input to Output), R_{I-O}	10^{12} Ω
Capacitance (Input to Output), C_{I-O}[3]	1.7 pF typ
Pb-Free Temperature, Soldering	
Reflow	260°C
ESD	1.5 kV

[1] Transient currents of up to 100 mA do not cause SCR to latch up.
[2] EDEC 2S2P standard board.
[3] f = 1 MHz.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform	891	V peak	Maximum CSA/VDE approved working voltage
DC Voltage	891	V	Maximum CSA/VDE approved working voltage

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

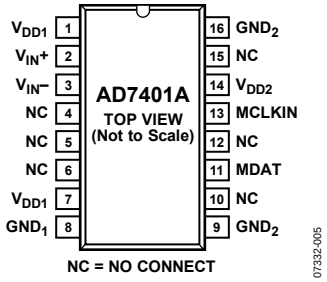

Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7	V_{DD1}	Supply Voltage, 4.5 V to 5.5 V. This is the supply voltage for the isolated side of the AD7401A and is relative to GND_1.
2	$V_{IN}+$	Positive Analog Input. Specified range of ±250 mV.
3	$V_{IN}-$	Negative Analog Input. Normally connected to GND_1.
4 to 6, 10, 12, 15	NC	No Connect.
8	GND_1	Ground 1. This is the ground reference point for all circuitry on the isolated side.
9, 16	GND_2	Ground 2. This is the ground reference point for all circuitry on the nonisolated side.
11	MDAT	Serial Data Output. The single bit modulator output is supplied to this pin as a serial data stream. The bits are clocked out on the rising edge of the MCLKIN input and valid on the following MCLKIN rising edge.
13	MCLKIN	Master Clock Logic Input. 20 MHz maximum. The bit stream from the modulator is valid on the rising edge of MCLKIN.
14	V_{DD2}	Supply Voltage. 3 V to 5.5 V. This is the supply voltage for the nonisolated side and is relative to GND_2.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, using 25 kHz brick-wall filter, unless otherwise noted.

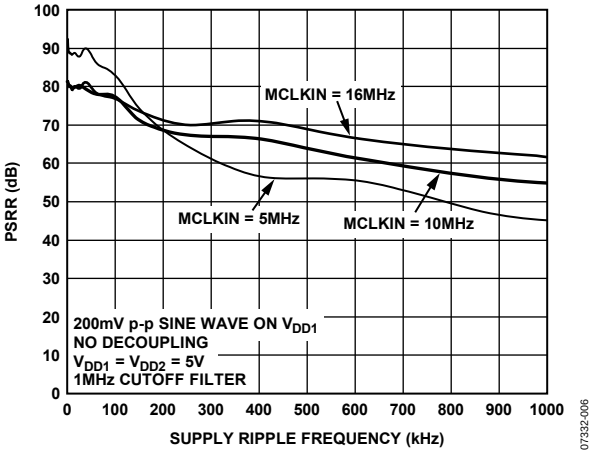

Figure 6. PSRR vs. Supply Ripple Frequency Without Supply Decoupling

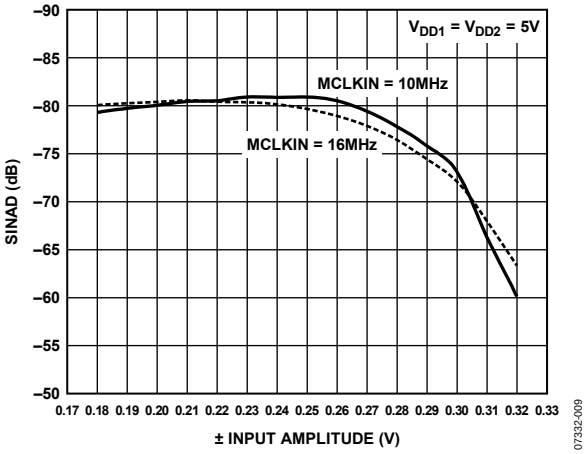

Figure 9. SINAD vs. V_{IN}

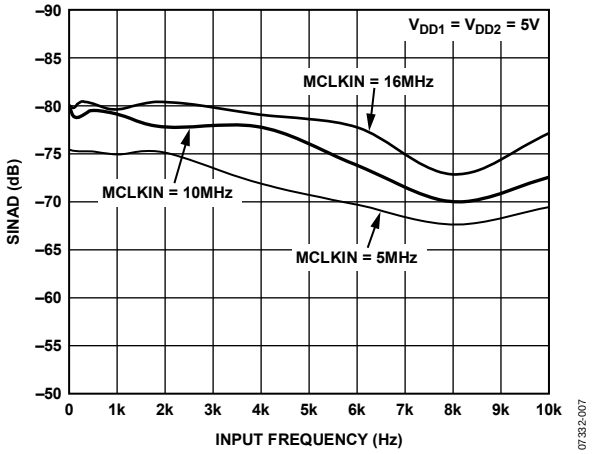

Figure 7. SINAD vs. Analog Input Frequency

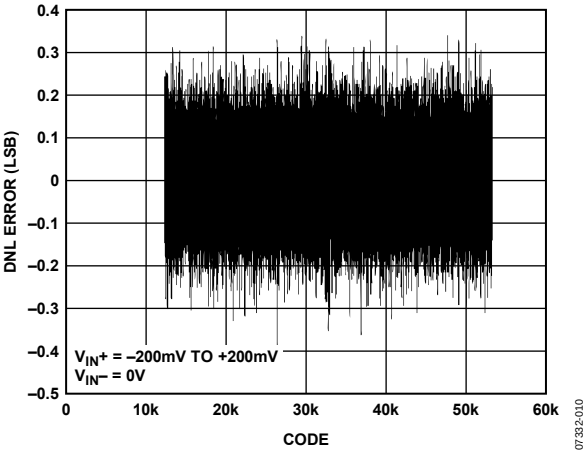

Figure 10. Typical DNL (±200 mV Range)

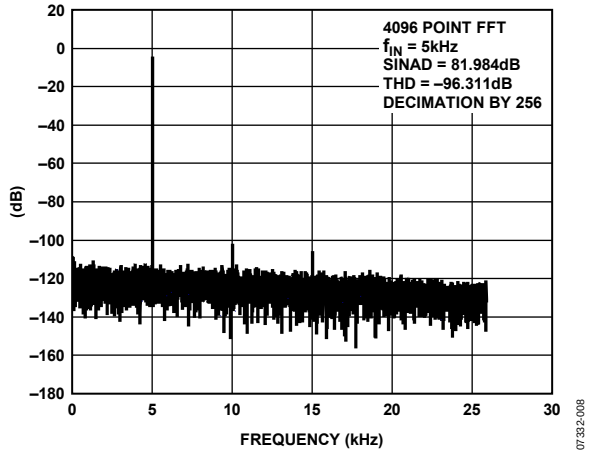

Figure 8. Typical FFT (±200 mV Range)

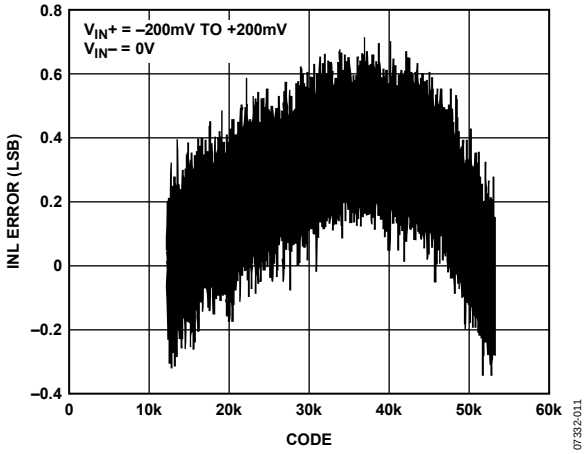

Figure 11. Typical INL (±200 mV Range)

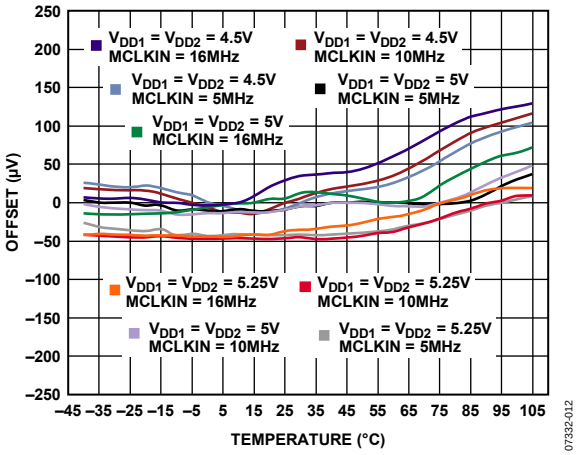

Figure 12. Offset Drift vs. Temperature for Various Supply Voltages

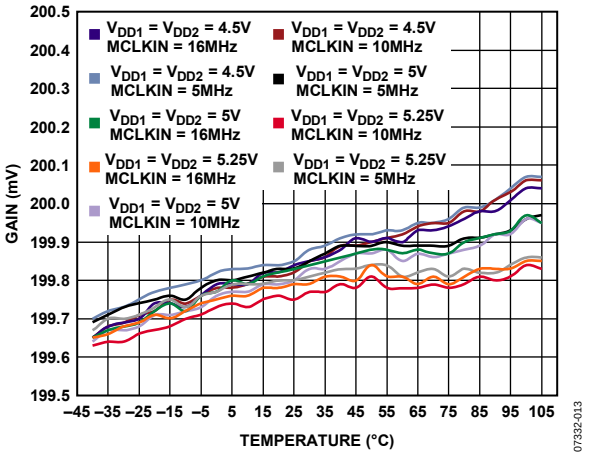

Figure 13. Gain Error Drift vs. Temperature for Various Supply Voltages

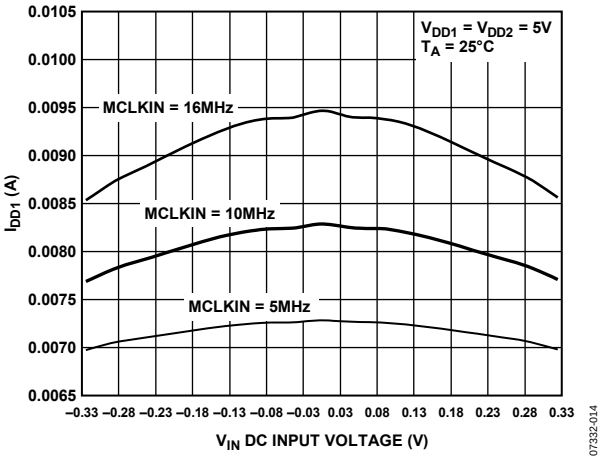

Figure 14. I_{DD1} vs. V_{IN} DC Input Voltage

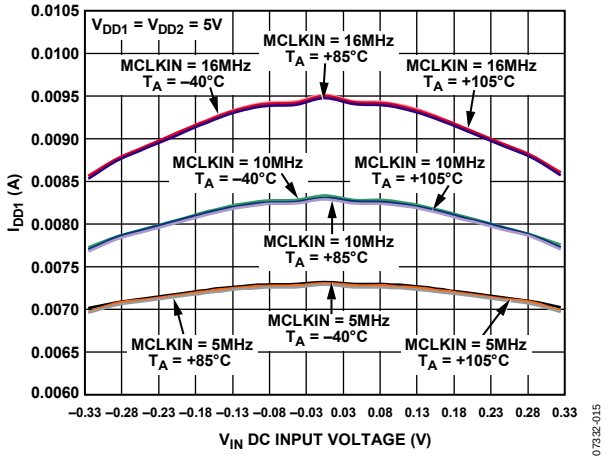

Figure 15. I_{DD1} vs. V_{IN} at Various Temperatures

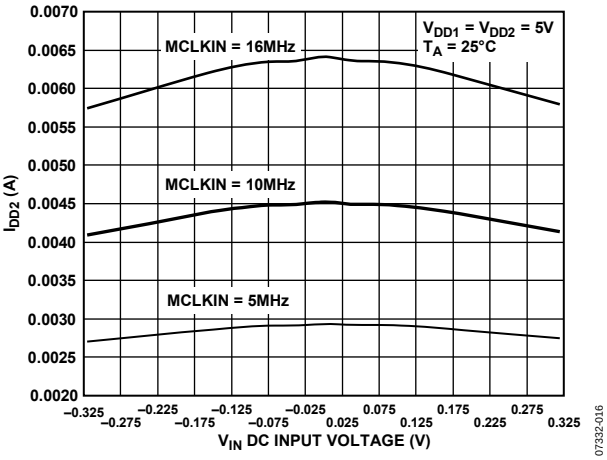

Figure 16. I_{DD2} vs. V_{IN} DC Input Voltage

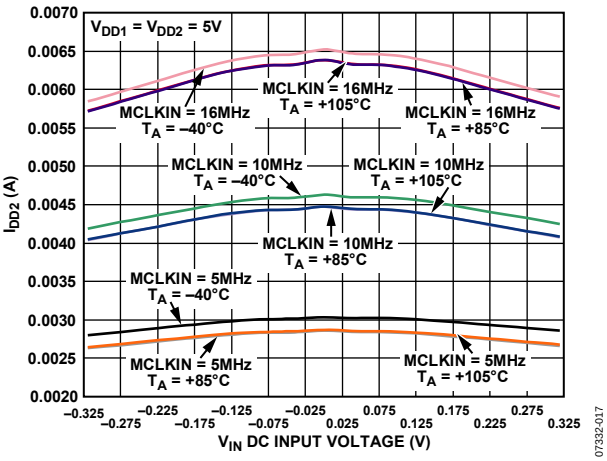

Figure 17. I_{DD2} vs. V_{IN} at Various Temperatures

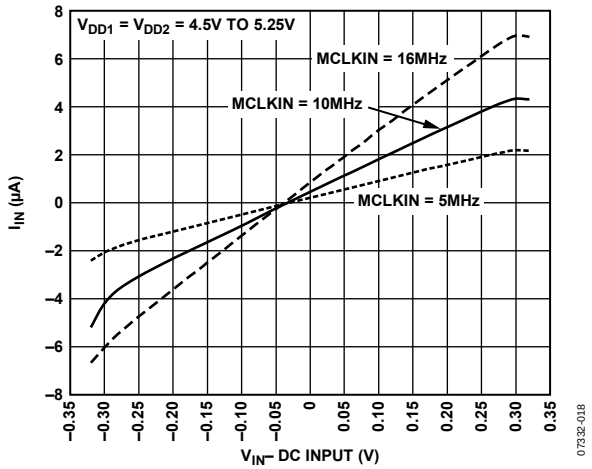

Figure 18. I_{IN} vs. V_{IN}– DC Input

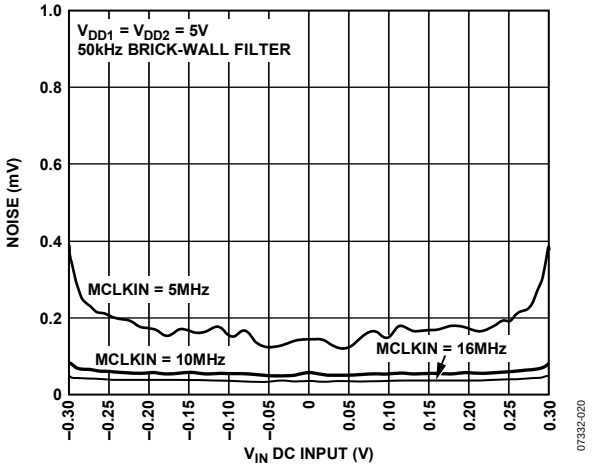

Figure 20. RMS Noise Voltage vs. V_{IN} DC Input

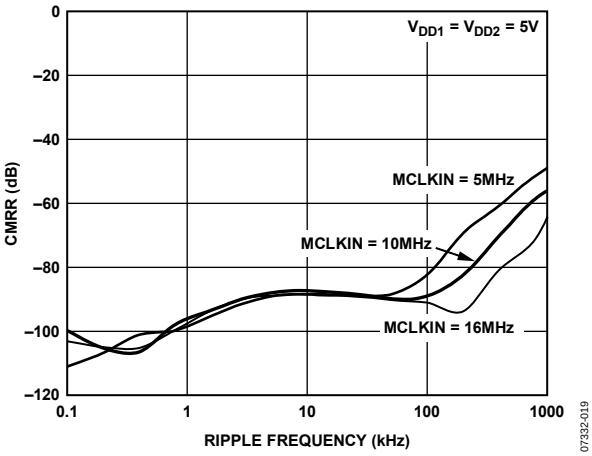

Figure 19. CMRR vs. Common-Mode Ripple Frequency

TERMINOLOGY

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are specified negative full scale, −250 mV ($V_{IN}+ - V_{IN}-$), Code 7169 for the 16-bit level, and specified positive full scale, +250 mV ($V_{IN}+ - V_{IN}-$), Code 58366 for the 16-bit level.

Offset Error
Offset error is the deviation of the midscale code (32768 for the 16-bit level) from the ideal $V_{IN}+ - V_{IN}-$ (that is, 0 V).

Gain Error
The gain error includes both positive full-scale gain error and negative full-scale gain error. Positive full-scale gain error is the deviation of the specified positive full-scale code (58366 for the 16-bit level) from the ideal $V_{IN}+ - V_{IN}-$ (+250 mV) after the offset error is adjusted out. Negative full-scale gain error is the deviation of the specified negative full-scale code (7169 for the 16-bit level) from the ideal $V_{IN}+ - V_{IN}-$ (−250 mV) after the offset error is adjusted out. Gain error includes reference error.

Signal-to-(Noise and Distortion) Ratio (SINAD)
SINAD is the measured ratio of signal-to-noise and distortion at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise and distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}(Noise\ and\ Distortion) = (6.02N + 1.76)\ \text{dB}$$

Therefore, for a 12-bit converter, this is 74 dB.

Effective Number of Bits (ENOB)
ENOB is defined by

$$ENOB = (SINAD - 1.76)/6.02\ \text{bits}$$

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7401A, it is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Common-Mode Rejection Ratio (CMRR)
CMRR is defined as the ratio of the power in the ADC output at ±250 mV frequency, f, to the power of a 250 mV p-p sine wave applied to the common-mode voltage of $V_{IN}+$ and $V_{IN}-$ of frequency, f_S, as

$$CMRR\ (\text{dB}) = 10\ .\log(Pf/Pf_S)$$

where:
Pf is the power at frequency, f, in the ADC output.
Pf_S is the power at frequency, f_S, in the ADC output.

Power Supply Rejection Ratio (PSRR)
Variations in power supply affect the full-scale transition but not the converter's linearity. PSRR is the maximum change in the specified full-scale (±250 mV) transition point due to a change in power supply voltage from the nominal value (see Figure 6).

Isolation Transient Immunity
The isolation transient immunity specifies the rate of rise/fall of a transient pulse applied across the isolation boundary beyond which clock or data is corrupted. The AD7401A was tested using a transient pulse frequency of 100 kHz.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7401A isolated Σ-Δ modulator converts an analog input signal into a high speed (20 MHz maximum), single-bit data stream; the time average single-bit data from the modulators is directly proportional to the input signal. Figure 23 shows a typical application circuit where the AD7401A is used to provide isolation between the analog input, a current sensing resistor, and the digital output, which is then processed by a digital filter to provide an N-bit word.

ANALOG INPUT

The differential analog input of the AD7401A is implemented with a switched capacitor circuit. This circuit implements a second-order modulator stage that digitizes the input signal into a 1-bit output stream. The sample clock (MCLKIN) provides the clock signal for the conversion process as well as the output data-framing clock. This clock source is external on the AD7401A. The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. A digital stream that accurately represents the analog input over time appears at the output of the converter (see Figure 21).

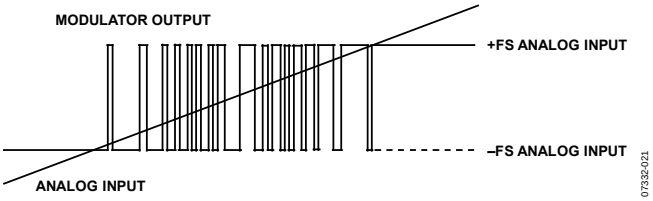

Figure 21. Analog Input vs. Modulator Output

A differential signal of 0 V results (ideally) in a stream of alternating 1s and 0s at the MDAT output pin. This output is high 50% of the time and low 50% of the time. A differential input of 200 mV produces a stream of 1s and 0s that are high 81.25% of the time (for a +250 mV input, the output stream is high 89.06% of the time). A differential input of −200 mV produces a stream of 1s and 0s that are high 18.75% of the time (for a −250 mV input, the output stream is high 10.94% of the time).

A differential input of 320 mV results in a stream of, ideally, all 1s. This is the absolute full-scale range of the AD7401A, and 200 mV is the specified full-scale range, as shown in Table 9.

Table 9. Analog Input Range

Analog Input	Voltage Input
Full-Scale Range	+640 mV
Positive Full Scale	+320 mV
Positive Typical Input Range	+250 mV
Positive Specified Input Range	+200 mV
Zero	0 mV
Negative Specified Input Range	−200 mV
Negative Typical Input Range	−250 mV
Negative Full Scale	−320 mV

To reconstruct the original information, this output needs to be digitally filtered and decimated. A sinc3 filter is recommended because this is one order higher than that of the AD7401A modulator. If a 256 decimation rate is used, the resulting 16-bit word rate is 62.5 kHz, assuming a 16 MHz external clock frequency. Figure 22 shows the transfer function of the AD7401A relative to the 16-bit output.

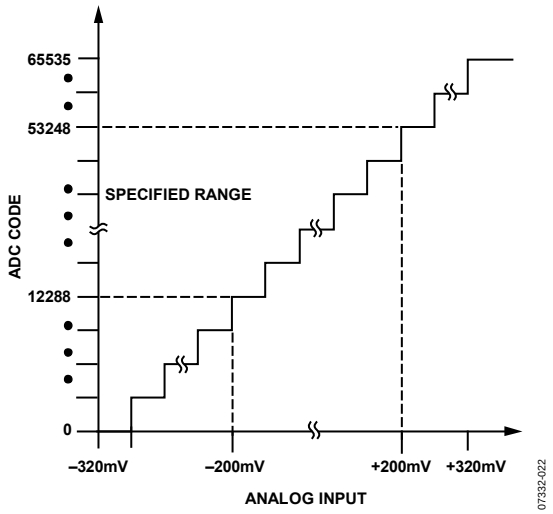

Figure 22. Filtered and Decimated 16-Bit Transfer Characteristic

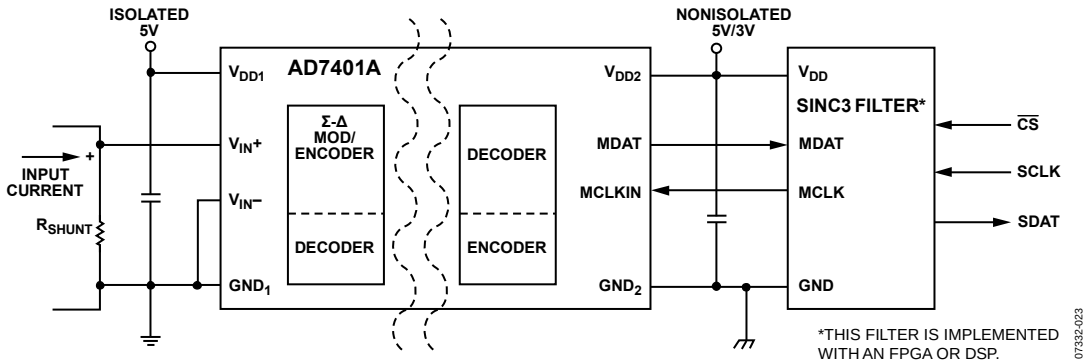

Figure 23. Typical Application Circuit

DIFFERENTIAL INPUTS

The analog input to the modulator is a switched capacitor design. The analog signal is converted into charge by highly linear sampling capacitors. A simplified equivalent circuit diagram of the analog input is shown in Figure 24. A signal source driving the analog input must be able to provide the charge onto the sampling capacitors every half MCLKIN cycle and settle to the required accuracy within the next half cycle.

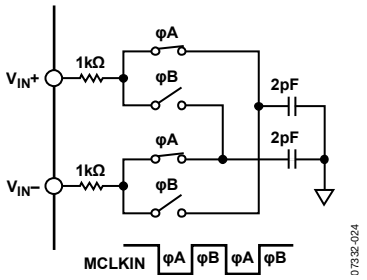

Figure 24. Analog Input Equivalent Circuit

Because the AD7401A samples the differential voltage across its analog inputs, low noise performance is attained with an input circuit that provides low common-mode noise at each input. The amplifiers used to drive the analog inputs play a critical role in attaining the high performance available from the AD7401A.

When a capacitive load is switched onto the output of an op amp, the amplitude momentarily drops. The op amp tries to correct the situation and, in the process, hits its slew rate limit. This nonlinear response, which can cause excessive ringing, can lead to distortion. To remedy the situation, a low-pass RC filter can be connected between the amplifier and the input to the AD7401A. The external capacitor at each input aids in supplying the current spikes created during the sampling process, and the resistor isolates the op amp from the transient nature of the load.

The recommended circuit configuration for driving the differential inputs to achieve best performance is shown in Figure 25. A capacitor between the two input pins sources or sinks charge to allow most of the charge that is needed by one input to be effectively supplied by the other input. The series resistor again isolates any op amp from the current spikes created during the sampling process. Recommended values for the resistors and capacitor are 22 Ω and 47 pF, respectively.

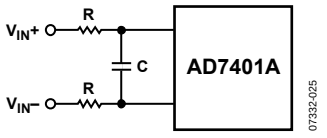

Figure 25. Differential Input RC Network

CURRENT SENSING APPLICATIONS

The AD7401A is ideally suited for current sensing applications where the voltage across a shunt resistor is monitored. The load current flowing through an external shunt resistor produces a voltage at the input terminals of the AD7401A. The AD7401A provides isolation between the analog input from the current sensing resistor and the digital outputs. By selecting the appropriate shunt resistor value, a variety of current ranges can be monitored.

Choosing R_{SHUNT}

The shunt resistor values used in conjunction with the AD7401A are determined by the specific application requirements in terms of voltage, current, and power. Small resistors minimize power dissipation, while low inductance resistors prevent any induced voltage spikes, and good tolerance devices reduce current variations. The final values chosen are a compromise between low power dissipation and good accuracy. Low value resistors have less power dissipated in them, but higher value resistors may be required to utilize the full input range of the ADC, thus achieving maximum SNR performance.

When the peak sense current is known, the voltage range of the AD7401A (±200 mV) is divided by the maximum sense current to yield a suitable shunt value. If the power dissipation in the shunt resistor is too large, the shunt resistor can be reduced and less of the ADC input range is used. Using less of the ADC input range results in performance that is more susceptible to noise and offset errors because offset errors are fixed and are thus more significant when smaller input ranges are used.

R_{SHUNT} must be able to dissipate the I2R power losses. If the power dissipation rating of the resistor is exceeded, its value may drift or the resistor may be damaged, resulting in an open circuit. This can result in a differential voltage across the terminals of the AD401A in excess of the absolute maximum ratings. If I_{SENSE} has a large high frequency component, take care to choose a resistor with low inductance.

VOLTAGE SENSING APPLICATIONS

The AD7401A can also be used for isolated voltage monitoring. For example, in motor control applications, it can be used to sense bus voltage. In applications where the voltage being monitored exceeds the specified analog input range of the AD7401A, a voltage divider network can be used to reduce the voltage to be monitored to the required range.

DIGITAL FILTER

The overall system resolution and throughput rate is determined by the filter selected and the decimation rate used. The higher the decimation rate, the greater the system accuracy, as illustrated in Figure 26. However, there is a tradeoff between accuracy and throughput rate and, therefore, higher decimation rates result in lower throughput solutions. Note that for a given bandwidth requirement, a higher MCLKIN frequency can allow for higher decimation rates to be used, resulting in higher SNR performance.

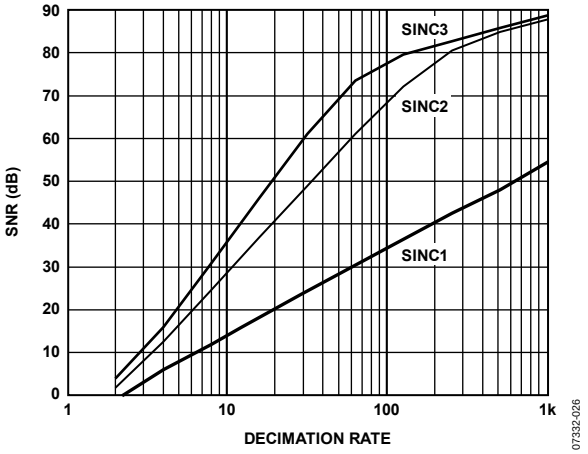

Figure 26. SNR vs. Decimation Rate for Different Filter Types

A sinc3 filter is recommended for use with the AD7401A. This filter can be implemented on an FPGA or a DSP.

$$H(z) = \left(\frac{\left(1 - Z^{DR}\right)}{\left(1 - Z^{-1}\right)} \right)^3$$

where *DR* is the decimation rate.

The following Verilog code provides an example of a sinc3 filter implementation on a Xilinx® Spartan-II 2.5 V FPGA. This code can possibly be compiled for another FPGA, such as an Altera® device. Note that the data is read on the negative clock edge in this case, although it can be read on the positive edge, if preferred.

```
/*`Data is read on negative clk edge*/
module DEC256SINC24B(mdata1, mclk1, reset,
DATA);
input  mclk1;       /*used to clk filter*/
input  reset;       /*used to reset filter*/
input  mdata1;      /*ip data to be
filtered*/
output [15:0] DATA;       /*filtered op*/
integer location;
integer info_file;
reg [23:0]          ip_data1;
reg [23:0]          acc1;
reg [23:0]          acc2;
reg [23:0]          acc3;
reg [23:0]          acc3_d1;
reg [23:0]          acc3_d2;
reg [23:0]          diff1;
reg [23:0]          diff2;
reg [23:0]          diff3;
reg [23:0]          diff1_d;
reg [23:0]          diff2_d;
reg [15:0]          DATA;
reg [7:0]           word_count;
reg word_clk;
reg init;


/*Perform the Sinc ACTION*/
always @ (mdata1)
if(mdata1==0)
     ip_data1 <= 0;        /* change from a 0
to a -1 for 2's comp */
else
     ip_data1 <= 1;
/*ACCUMULATOR (INTEGRATOR)
Perform the accumulation (IIR) at the speed
of the modulator.
```

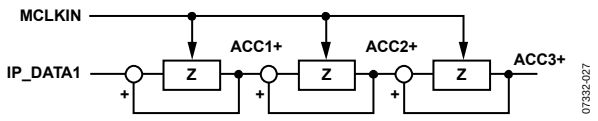

Figure 27. Accumulator

```
Z = one sample delay
MCLKOUT = modulators conversion bit rate
*/

always @ (posedge mclk1 or posedge reset)
if (reset)
     begin
      /*initialize acc registers on reset*/
     acc1 <= 0;
     acc2 <= 0;
     acc3 <= 0;
     end
else
     begin
      /*perform accumulation process*/
     acc1 <= acc1 + ip_data1;
     acc2 <= acc2 + acc1;
     acc3 <= acc3 + acc2;
     end

/*DECIMATION STAGE (MCLKOUT/ WORD_CLK)
*/

always @ (negedge mclk1 or posedge reset)
if (reset)
        word_count <= 0;
else
        word_count <= word_count + 1;

always @ (word_count)
        word_clk <= word_count[7];

/*DIFFERENTIATOR ( including decimation
stage)
Perform the differentiation stage (FIR) at a
lower speed.
```

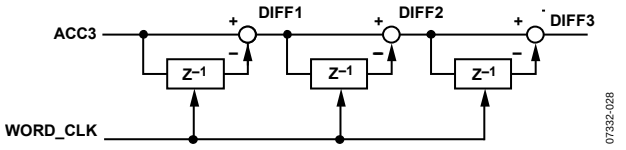

Figure 28. Differentiator

```
Z = one sample delay
WORD_CLK = output word rate
*/


always @ (posedge word_clk or posedge reset)
if(reset)
     begin
     acc3_d2 <= 0;
     diff1_d <= 0;
     diff2_d <= 0;
     diff1 <= 0;
     diff2 <= 0;
     diff3 <= 0;
     end


else
     begin
     diff1 <= acc3 - acc3_d2;
     diff2 <= diff1 - diff1_d;
     diff3 <= diff2 - diff2_d;
     acc3_d2 <= acc3;
     diff1_d <= diff1;
     diff2_d <= diff2;
     end

/* Clock the Sinc output into an output
register
```

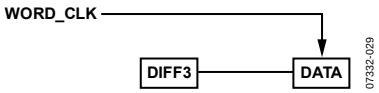

Figure 29. Clocking Sinc Output into an Output Register

```
WORD_CLK = output word rate
*/

always @ (posedge word_clk)
begin

DATA[15] <= diff3[23];
DATA[14] <= diff3[22];
DATA[13] <= diff3[21];
DATA[12] <= diff3[20];
DATA[11] <= diff3[19];
DATA[10] <= diff3[18];
DATA[9]  <= diff3[17];
DATA[8]  <= diff3[16];
DATA[7]  <= diff3[15];
DATA[6]  <= diff3[14];
DATA[5]  <= diff3[13];
DATA[4]  <= diff3[12];
DATA[3]  <= diff3[11];
DATA[2]  <= diff3[10];
DATA[1]  <= diff3[9];
DATA[0]  <= diff3[8];

end
  endmodule
```

APPLICATIONS INFORMATION

GROUNDING AND LAYOUT

Supply decoupling with a value of 100 nF is recommended on both V_{DD1} and V_{DD2}. In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed so that any coupling that occurs equally affects all pins on a given component side. Failure to ensure this may cause voltage differentials between pins to exceed the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage. Any decoupling used should be placed as close to the supply pins as possible.

Series resistance in the analog inputs should be minimized to avoid any distortion effects, especially at high temperatures. If possible, equalize the source impedance on each analog input to minimize offset. Beware of mismatch and thermocouple effects on the analog input PCB tracks to reduce offset drift.

EVALUATING THE AD7401A PERFORMANCE

An AD7401A evaluation board is available with split ground planes and a board split beneath the AD7401A package to ensure isolation. This board allows access to each pin on the device for evaluation purposes.

The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via the EVAL-CED1Z. The software also includes a sinc3 filter implemented on an FPGA. The evaluation board is used in conjunction with the EVAL-CED1Z board and can also be used as a standalone board. The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7401A. The software and documentation are on a CD that is shipped with the evaluation board.

INSULATION LIFETIME

All insulation structures, subjected to sufficient time and/or voltage, are vulnerable to breakdown. In addition to the testing performed by the regulatory agencies, Analog Devices has carried out an extensive set of evaluations to determine the lifetime of the insulation structure within the AD7401A.

These tests subjected devices to continuous cross-isolation voltages. To accelerate the occurrence of failures, the selected test voltages were values exceeding those of normal use. The time-to-failure values of these units were recorded and used to calculate acceleration factors. These factors were then used to calculate the time-to-failure under normal operating conditions. The values shown in Table 7 are the lesser of the following two values:

- The value that ensures at least a 50-year lifetime of continuous use.
- The maximum CSA/VDE approved working voltage.

It should also be noted that the lifetime of the AD7401A varies according to the waveform type imposed across the isolation barrier. The *i*Coupler insulation structure is stressed differently depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 30, Figure 31, and Figure 32 illustrate the different isolation voltage waveforms.

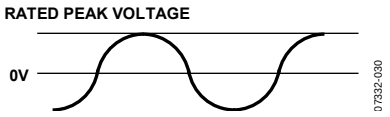

Figure 30. Bipolar AC Waveform

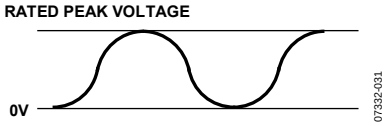

Figure 31. Unipolar AC Waveform

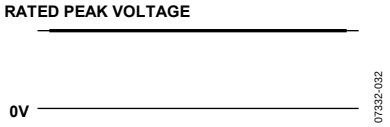

Figure 32. DC Waveform

OUTLINE DIMENSIONS

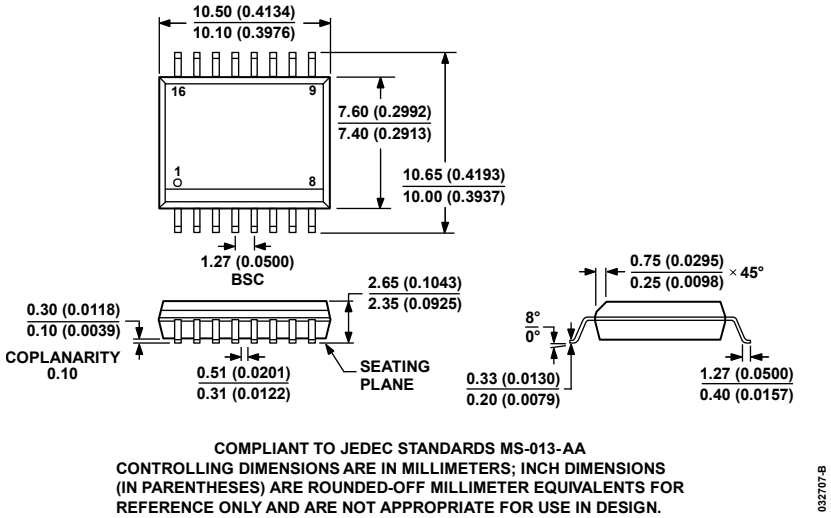

Figure 33. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7401AYRWZ[1]	−40°C to +125°C	16-Lead Standard Small Outline Package (SOIC_W)	RW-16
AD7401AYRWZ-RL[1]	−40°C to +125°C	16-Lead Standard Small Outline Package (SOIC_W)	RW-16
EVAL-AD7401AEDZ[1]		Evaluation Board	
EVAL-CED1Z[1]		Development Board	

[1] Z = RoHS Compliant Part.

NOTES

D07332-0-7/08(0)