

M62371GP

3 V Type 8-bit 36ch Selector SW Built-in D/A Converter with Buffer Amplifiers

REJ03D0880-0201

Rev.2.01

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Description

The M62371GP is a CMOS semiconductor IC, containing 36 channels of 8-bit D/A converters. It is operable with a low supply voltage between 2.7 to 3.6 V, and is easy to use due to serial data input, and 3-pin (DI, CLK, LD) connection with microcomputer.

The IC also contains D_O pin terminal, enabling cascade connection, and therefore is suitable for automatic control in combination with a microcomputer.

(M62371GP is an advanced product of M62370GP on its buffer amp. drivability.)

Features

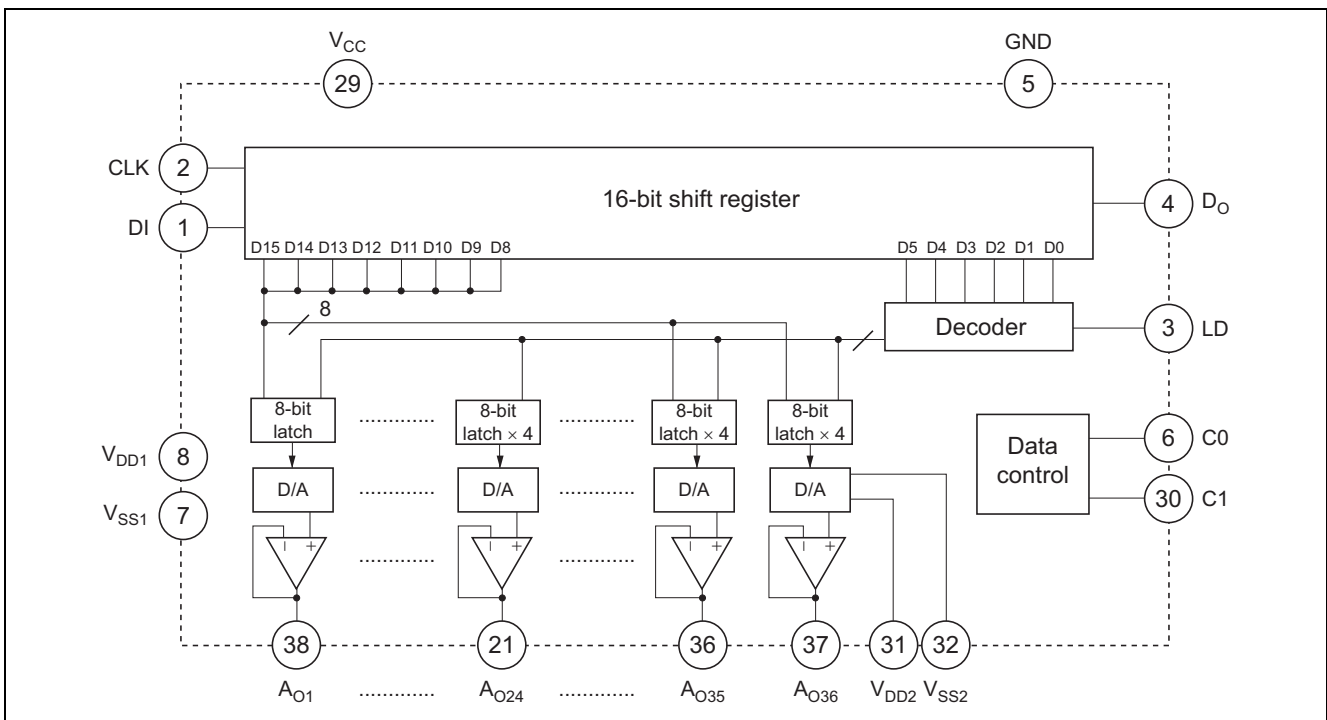
- Operable with a low voltage between 2.7 to 3.6 V
- 16-bit serial data input (connected via 3 pins: DI, CLK, LD)
- 36 channels built-in of 8-bit D/A converter
- 6 channels of D/A converters capable of selecting and outputting 4 data stored in each converter, through 2 control terminals

Application

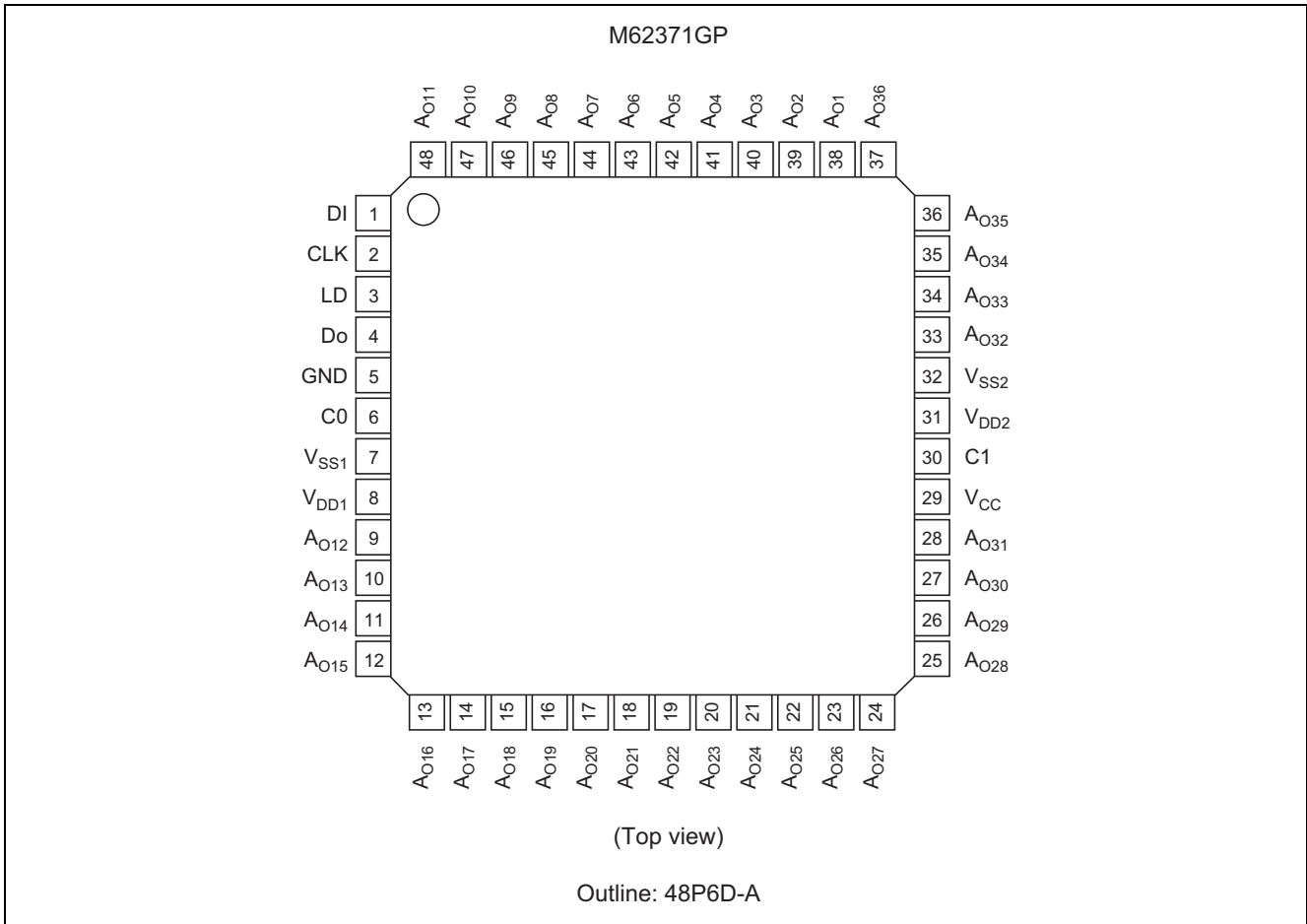
Digital/analog conversion in industrial or home-use electronic equipment.

Automatic control in combination with EEPROM and microcomputer (Substitute for conventional semi-fixed resistor).

Block Diagram



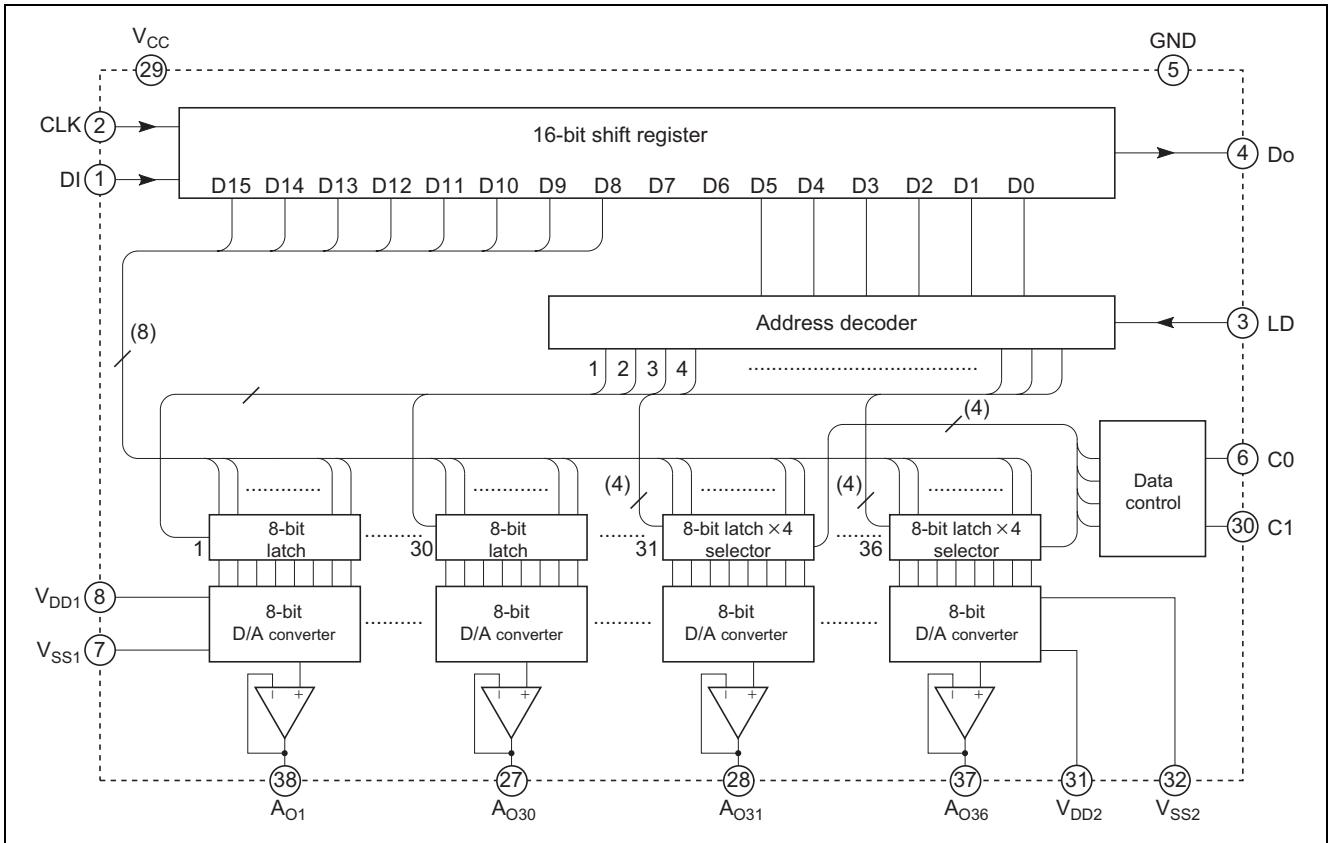
Pin Arrangement



Pin Description

Pin No.	Pin Name	Function
1	DI	Serial data input terminal to input 16-bit long serial data
4	Do	Terminal to output MSB data of 16-bit shift register
2	CLK	Shift clock input terminal. Input signal at DI pin is input to 16-bit shift register at rise of shift clock pulse
3	LD	When H-level signal is input to this terminal, the value stored in 16-bit shift register is loaded in decoder and D/A converter output register.
38 to 48	AO ₁ to AO ₁₁	8-bit D/A converter output terminal
9 to 28	AO ₁₂ to AO ₃₁	
33 to 37	AO ₃₂ to AO ₃₆	
29	V _{CC}	Power supply terminal
5	GND	GND terminal
6	C0	Data select signal input terminal 1 for channel No.31 through 36
30	C1	Data select signal input terminal 2 for channel No.31 through 36
8	V _{DD1}	Upper reference voltage input terminal and power supply to operational amplifier for channel No.1 through 24
7	V _{SS1}	Lower reference voltage input terminal for channel No.1 through 24
31	V _{DD2}	Upper reference voltage input terminal and power supply to operational amplifier for channel No.25 through 36
32	V _{SS2}	Lower reference voltage input terminal for channel No.25 through 36

Block Diagram for Explanation of Terminals



Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted.)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V _{CC}	-0.3 to +7.0	V	
Output voltage	V _O	-0.3 to V _{CC} + 0.3	V	
Power dissipation	P _d	400	mW	
Thermal derating	Kθ	4	mW/°C	Ta ≤ 25°C
Operating temperature	T _{opr}	-20 to +85	°C	
Storage temperature	T _{stg}	-40 to +125	°C	

Electrical Characteristics

<Digital Part>

($V_{CC} = +3\text{ V} \pm 10\%$, $V_{CC} = V_{DD}$, $T_a = -20$ to $+85^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	V_{CC}	2.7	3.0	5.5	V	
Circuit current	I_{CC}	—	1.0	—	mA	CLK = 1 MHz operation, $V_{CC} = 3\text{ V}$, $I_{AO} = 0\ \mu\text{A}$
Input leak current	I_{ILK}	-10	—	10	μA	
Input low voltage	V_{IL}	—	—	0.6	V	
Input high voltage	V_{IH}	2.4	—	—	V	
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2.5\text{ mA}$
Output high voltage	V_{OH}	$V_{CC} - 0.4$	—	—	V	$I_{OH} = -400\ \mu\text{A}$

Note: Standard value is at $T_a = 25^\circ\text{C}$

<Analog Part>

($V_{CC} = +3\text{ V} \pm 10\%$, $V_{CC} = V_{DD}$, $T_a = -20$ to $+85^\circ\text{C}$, unless otherwise noted.)

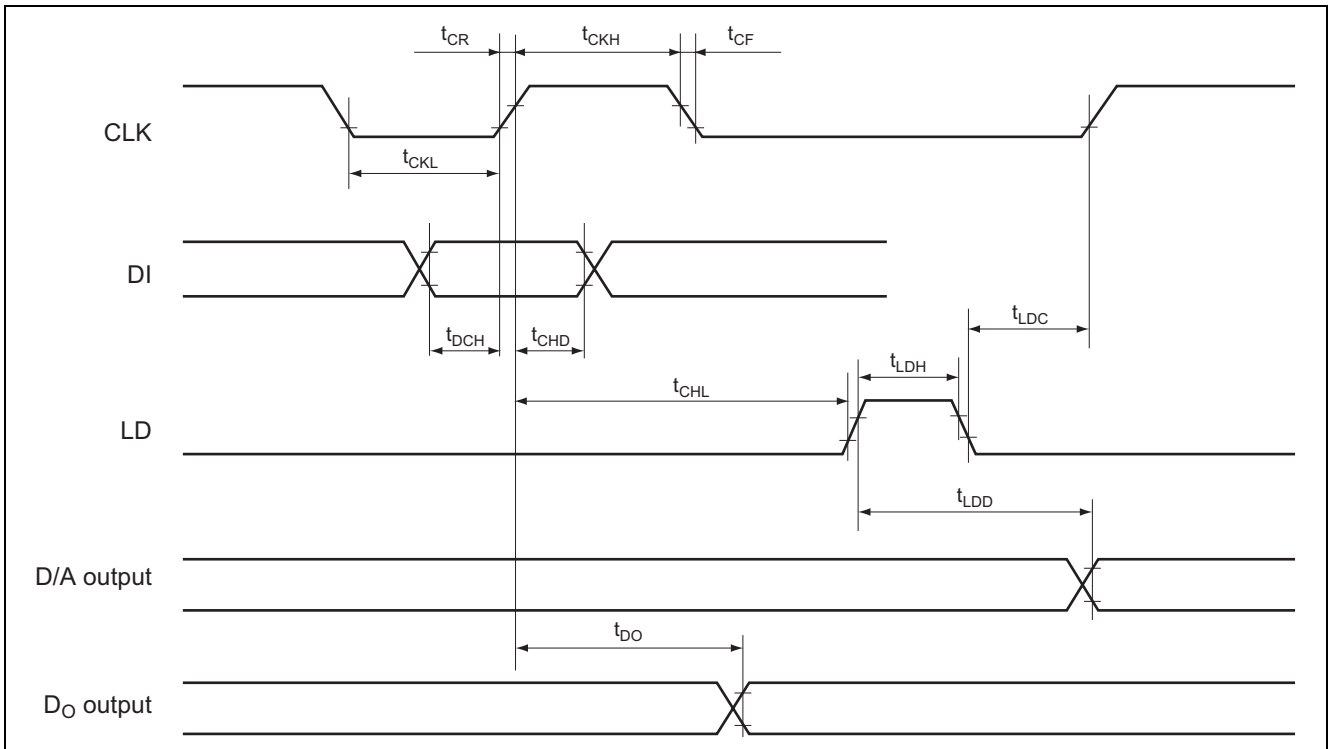
Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Current dissipation	I_{DD}	—	8.0	12.0	mA	
D/A converter upper reference voltage range	V_{DD}	2.7	3.0	5.5	V	
D/A converter lower reference voltage range	V_{SS}	GND	—	$V_{DD} - 2$	V	
Buffer amplifier output voltage range	V_{AO}	0.1	—	$V_{DD} - 0.1$	V	$I_{AO} = \pm 0.5\text{ mA}$
		0.2	—	$V_{DD} - 0.2$	V	$I_{AO} = \pm 1.0\text{ mA}$
Buffer amplifier output driving range	I_{AO}	-1.5	—	1.5	mA	Upper saturation voltage = 0.4 V Lower saturation voltage = 0.4 V
Differential nonlinearity error	S_{DL}	-1.0	—	1.0	LSB	$V_{CC} = 2.700\text{ V}$ $V_{DD} = 2.700\text{ V}$
Nonlinearity error	S_L	-1.5	—	1.5	LSB	$V_{SS} = 0.050\text{ V}$
Zero code error	S_{ZERO}	-2	—	2	LSB	No load ($I_{AO} = \pm 0$)
Full scale error	S_{FULL}	-2	—	2	LSB	
Output capacitive load	C_O	—	—	0.1	μF	
Buffer amplifier output impedance	R_O	—	50	—	Ω	

AC Characteristics

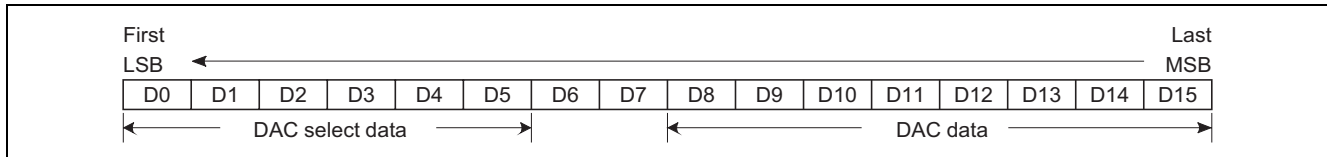
(V_{CC} = V_{DD}, T_a = -20 to +85°C, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Clock "L" pulse width	t _{CKL}	200	—	—	ns	
Clock "H" pulse width	t _{CKH}	200	—	—	ns	
Clock rise time	t _{CR}	—	—	200	ns	
Clock fall time	t _{CF}	—	—	200	ns	
Data setup time	t _{DCH}	30	—	—	ns	
Data hold time	t _{CHD}	60	—	—	ns	
LD setup time	t _{CHL}	200	—	—	ns	
LD hold time	t _{LDC}	100	—	—	ns	
LD "H" pulse duration time	t _{LDH}	100	—	—	ns	
Data output delay time	t _{DO}	70	—	350	ns	C _L = 100 pF
D/A converter output setting time	t _{LDD}	—	—	100	μs	C _L ≤ 100 pF, V _{AO} : 0.3 V ↔ 2.7 V This time until the output becomes the final value of ±2 LSB

Timing Chart



Digital Data Format



DAC Data

D8	D9	D10	D11	D12	D13	D14	D15	D/A Output
0	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 1 + V_{refL}$
1	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 2 + V_{refL}$
0	1	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 3 + V_{refL}$
1	1	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 4 + V_{refL}$
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	$(V_{refU} - V_{refL}) / 256 \times 255 + V_{refL}$
1	1	1	1	1	1	1	1	V_{refU}

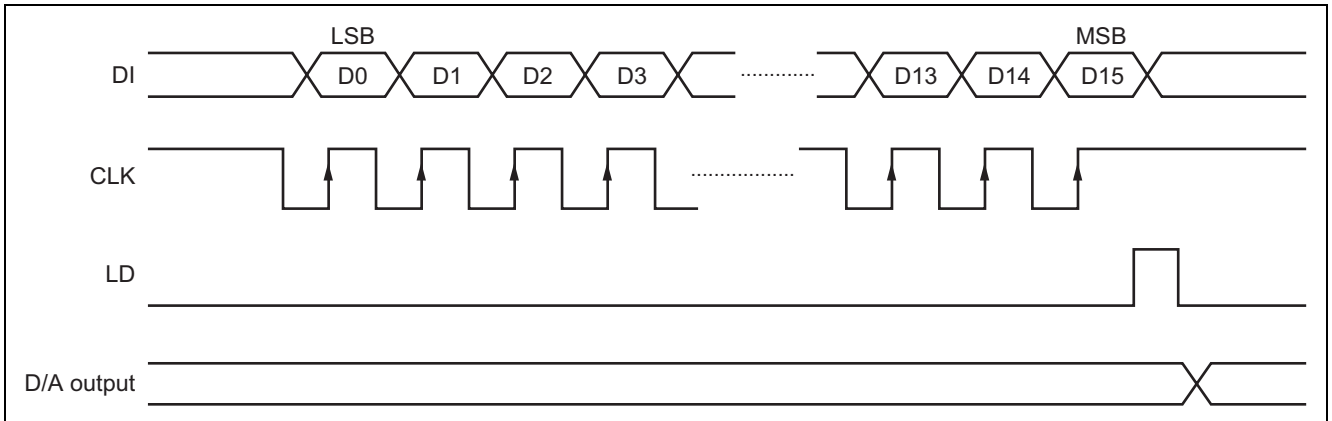
Note: $V_{refU} = V_{DD1}, V_{DD2}, V_{refL} = V_{SS1}, V_{SS2}$

DAC Select Data

D5	D4	D3	D2	D1	D0	DAC Selection
0	0	0	0	0	0	Don't care
0	0	0	0	0	1	A ₀₁ selection
0	0	0	0	1	0	A ₀₂ selection
:	:	:	:	:	:	:
0	1	1	1	1	0	A ₀₃₀ selection
0	1	1	1	1	1	A _{031 (0)} selection
1	0	0	0	0	0	A _{032 (0)} selection
:	:	:	:	:	:	:
1	0	0	1	0	0	A _{036 (0)} selection
1	0	0	1	0	1	A _{031 (1)} selection
:	:	:	:	:	:	:
1	0	1	0	1	0	A _{036 (1)} selection
1	0	1	0	1	1	A _{031 (2)} selection
:	:	:	:	:	:	:
1	1	0	0	0	0	A _{036 (2)} selection
1	1	0	0	0	1	A _{031 (3)} selection
:	:	:	:	:	:	:
1	1	0	1	1	0	A _{036 (3)} selection
1	1	0	1	1	1	Don't care
:	:	:	:	:	:	:
1	1	1	1	1	1	Don't care

C0	C1	A ₀₃₁ Through A ₀₃₆ Data Selected
0	0	Address 0 selected
0	1	Address 1 selected
1	0	Address 2 selected
1	1	Address 3 selected

Timing Chart (Model)

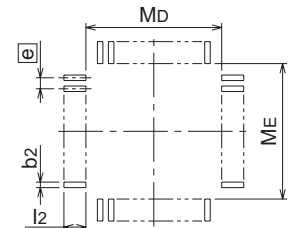
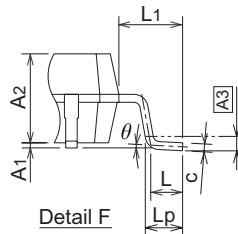
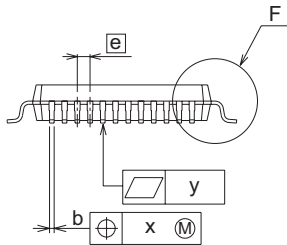
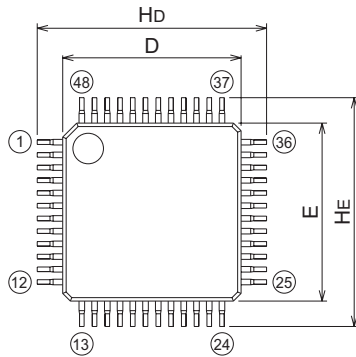


Package Dimensions

48P6D-A

Plastic 48pin 7 × 7mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP48-P-77-0.50	—	0.18	Alloy 42



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A1	0	0.1	0.2
A2	—	1.4	—
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	—	0.5	—
H_d	8.8	9.0	9.2
H_E	8.8	9.0	9.2
L	0.3	0.5	0.7
L_1	—	1.0	—
L_p	0.45	0.6	0.75
A3	—	0.25	—
x	—	—	0.08
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.225	—
l_2	1.0	—	—
MD	—	7.4	—
ME	—	7.4	—

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