Ordering number : ENA1205

SANYO Semiconductors
DATA SHEET

LV23014T — Bi-CMOS IC For Mini Component, receiver 1-chip Tuner IC Incorporating PLL

Overview

The LV23014T is a Single-chip tuner IC with built-in PLL for mini component, receiver.

Functions

- AM tuner
- FM tuner
- MPX stereo decoder
- PLL frequency synthesizer

Specifications

Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max	V_{CC}	7.0	V
Maximum input voltage	$V_{IN}1$ max	CE, CI, CL	7.0	V
	$V_{IN}2$ max	XIN	*1 Vreg2+0.3	V
Maximum output voltage	$V_{O}1$ max	DO	7.0	V
	$V_{O}2$ max	XOUT, PD	Vreg2+0.3	V
	$V_{O}3$ max	BO1, AOUT	12.0	V
Allowable power dissipation	Pd max	Ta≤70°C *2	400	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

*1 Vreg2 : 21 pin output voltage (Reference voltage of PLL) Reference value (3.0V±0.2V)

*2 Specified board : 114.3mm×76.1mm×1.6mm, glass epoxy board.

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Operating Condition at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5.0	V
Operating supply voltage range	V_{CC} op		4.0 to 6.0	V

PLL block Allowable Operating Range at Ta = -20°C to +70°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high level voltage	V_{IH}	CE, CL, DI	0.7Vreg2		6.0	V
Input low level voltage	V_{IL}	CE, CL, DI	0		0.3Vreg2	V
Output voltage	V_O1	DO	0		6.0	V
	V_O2	BO1, AOUT	0		10	V
Operating frequency	$f_{IN}1$	XIN ; $V_{IN}1$		4.5		MHz
	$f_{IN}2$	FMIN ; $V_{IN}2$	10		160	MHz
	$f_{IN}3$	AMIN (SNS = 1) ; $V_{IN}3$	2		40	MHz
	$f_{IN}4$	AMIN (SNS = 0) ; $V_{IN}4$	0.5		10	MHz

Note : The XIN pin has extremely high input impedance, so that due care must be taken to prevent leakage.

Operating Characteristics at Ta = 25°C, V_{CC} = 5.0V, for the specified test circuit.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
FM-FE characteristics : fc = 98MHz, fm = 1kHz, 22.5kHzdev.						
3dB sensitivity	-3dB LS	60dBμV, 22.5kHzdev output reference, -3dB input		5		dBμV EMF
Practical sensitivity	QS	S/N = Input at S/N = 30dB		8		dBμV EMF
FM-EF stereo characteristics : fc = 98MHz, fm = 1kHz, 75kHzdev, L+R = 90%, Pilot = 10%, V_{IN} = 60dBμVEMF						
Stereo ON bandwidth	ST-BW	ST-ON frequency bandwidth, 18pin (DO) output		(300) Reference value		kHz
FM-IF monaural characteristics : fc = 10.7MHz, fm = 1kHz, 75kHzdev.						
Demodulation output	V_O	100dBμV, 12pin output	750	1000	1200	mVrms
Channel balance	CB	100dBμV, 12pin output	-1.0	0	+1.0	dB
Signal to noise ratio	S/N	100dBμV, 12pin output	68	74		dB
AM suppression ratio	AMR	70dBμV input 12pin output reference, FM = no-mod, AM = 1kHz-30%mod, 12pin output	40	50		dB
Total harmonic distortion (monaural)	THD	100dBμV, 12pin output		0.6	1.5	%
3dB sensitivity	3dB LS	100dBμV, 75kHzdev output reference, -3dB input		38	44	dBμV
IF count sensitivity	IF-C3	SDC0 = 1, SDC1 = 0, 18pin (DO) output	38	46	54	dBμV
Mute attenuation	Mute-Att	100dBμV, 12pin output	60	70		dB
FM-IF stereo characteristics : fc = 10.7MHz, fm = 1kHz, Pilot = 10%						
Separation	SEP	100dBμV, L+R = 90%, L-mod, 12pin output/13pin output	28	38		dB
Total harmonic distortion (main)	THD-ST	100dBμV, L+R = 90%, Main-mod, 12pin output		1.0	2.0	%
Total harmonic distortion (L only)	THD-L	100dBμV, L+R = 90%, L-mod, 12pin output		0.6	2.0	%
Stereo ON sensitivity	ST-ON	100dBμV, L+R = 90%, 18 (DO) pin output	0.6		6.5	%
AM characteristics : fc = 1000kHz, fm = 1kHz, 30%mod						
Detection output 1	V_O1	23dBμV, 12pin output	60	120	240	mVrms
Detection output 2	V_O2	80dBμV, 12pin output	220	330	440	mVrms
Signal to noise ratio 1	S/N1	23dBμV, 12pin output	15	20		dB
Signal to noise ratio 2	S/N2	80dBμV, 12pin output	47	54		dB
Total harmonic distortion	THD	80dBμV, 12pin output		1.2	2.5	%
IF count sensitivity	IF-C	18pin (DO) output	16	26	36	dBμV
Mute attenuation	Mute-Att	80dBμV, 12pin output	54	65		dB

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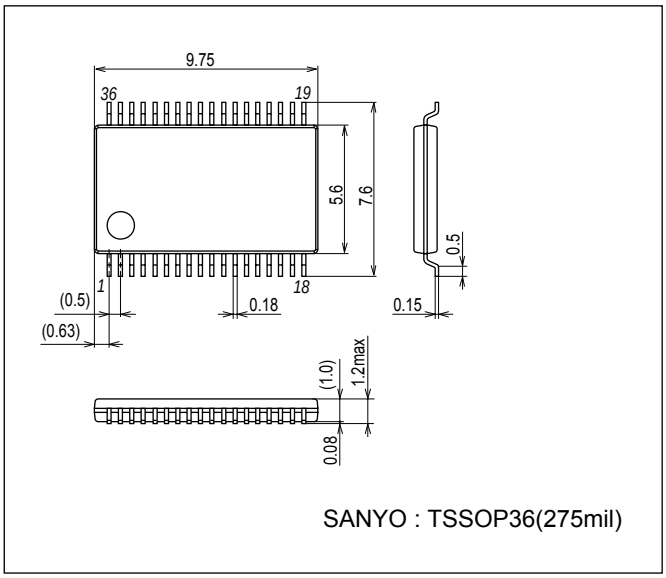
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain						
FM tuner	$I_{CC}FM$	No input at FM	25	35	45	mA
AM tuner	$I_{CC}AM$	No input at AM	11	22	33	mA
PLL characteristics						
Built-in return resistor	Rf	XIN		8		MΩ
Built-in output resistor	Rd	XOUT		250		kΩ
Hysteresis width	V_{HIS}	CE, CL, DI		0.1Vreg2		V
Output high level voltage	V_{OH}	PD ; I_O = -1mA	Vreg2-1.0			V
Output low level voltage	$V_{OL}2$	BO1 ; I_O = 1mA			0.25	V
		BO1 ; I_O = 5mA			1.25	V
	$V_{OL}3$	DO ; I_O = 1mA			0.25	V
	$V_{OL}4$	AOUT ; I_O = 1mA, A_{IN} = 2.0V			0.5	V
Input high level current	$I_{IH}1$	CE, CL, DI ; V_I = 6.0V			5.0	μA
	$I_{IH}2$	XIN ; V_I = V_{DD}	0.16		0.9	μA
	$I_{IH}3$	AIN ; V_I = 6.0V			200	nA
Input low level current	$I_{IL}1$	CE, CL, DI ; V_I = 0V			5.0	μA
	$I_{IL}2$	XIN ; V_I = 0V	0.16		0.9	μA
	$I_{IL}3$	AIN ; V_I = 0V			200	nA
Output off-leak current	$I_{OFF}1$	AOUT, BO1 ; V_O = 10V			5.0	μA
	$I_{OFF}2$	DO ; V_O = 6.0V			5.0	μA

Package Dimensions

unit : mm (typ)

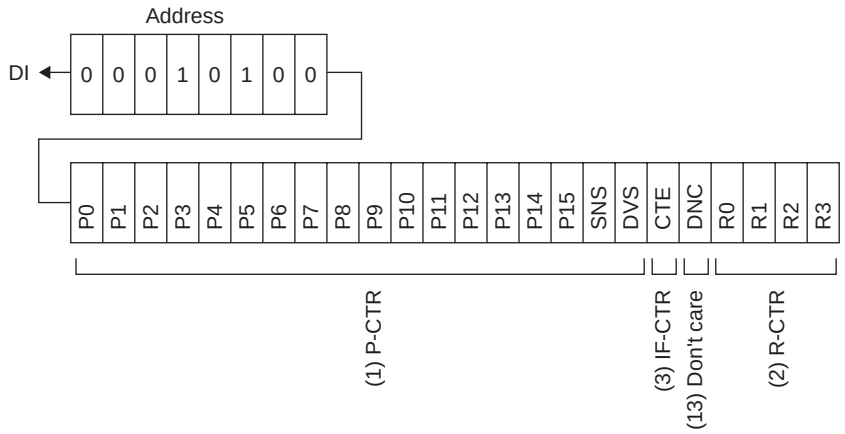
3253B



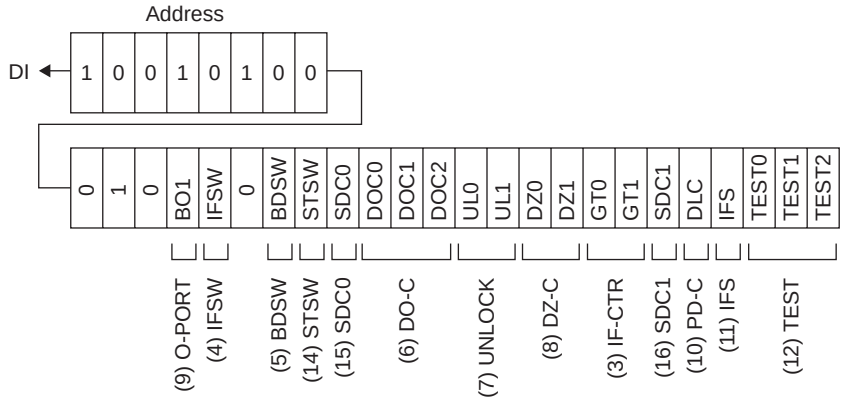
SANYO : TSSOP36(275mil)

Composition of DI control data (serial data input)

(1) IN mode



(2) IN2 mode



Description of DI control Data

<table>
<tr><th>No.</th><th>Control/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data

P0 to P15
DVS, SNS</td><td>
• Data to set the number of divisions of programmable divider Binary value using P15 as MSB. LSB varies depending on DVS and SNS.
(* : don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>Set number of divisions (N)</th><th>Actual number of divisions</th></tr>
<tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the set value</td></tr>
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>Set value</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>Set value</td></tr>
</table>
* LSB : P0 to P3 invalid when LSB is P4.
• Selection of the signal input (FMIN, AMIN) to the programmable divider and switching of the input frequency.
(* : don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>Input</th><th>Operation frequency range</th></tr>
<tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 160MHz</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40MHz</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10MHz</td></tr>
</table>
</td><td></td></tr>
<tr><td>(2)</td><td>Reference divider data

R0 to R3</td><td>
• Data to select the reference frequency.
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>25kHz</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>25kHz</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25kHz</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25kHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5kHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25kHz</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125kHz</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125kHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5kHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5kHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5kHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1kHz</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3kHz</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15kHz</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT+X'tal OSC STOP</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr>
</table>
* PLL INHIBIT
• Programmable divider and IF counter blocks stop, FMIN, AMIN, and IFIN inputs enter the pull-down state (GND), and the charge pump has high impedance.
</td><td></td></tr>
<tr><td>(3)</td><td>IF counter control data

CTE
GT0, GT1</td><td>
• IF counter measurement start data
CTE = 1 : Count start
= 0 : Count reset
• Determines the universal counter measurement time.
<table>
<tr><th>GT1</th><th>GT0</th><th>Measurement time</th><th>Wait time</th></tr>
<tr><td>0</td><td>0</td><td>4ms</td><td>3 to 4ms</td></tr>
<tr><td>0</td><td>1</td><td>8ms</td><td>3 to 4ms</td></tr>
<tr><td>1</td><td>0</td><td>16ms</td><td>3 to 4ms</td></tr>
<tr><td>1</td><td>1</td><td>32ms</td><td>3 to 4ms</td></tr>
</table>
</td><td>IFS</td></tr>
<tr><td>(4)</td><td>MUTE
IF count output
SD time constant changeover control data

IFSW</td><td>
• Data to determine the output of the output port IFSW, controlling the MUTE function, IF count output (*1), and SD time constant changeover circuit (*2).
"Data" = 0 : MUTE, IF count output, SD time constant changeover circuit-OFF (during normal reception)
1 : MUTE, IF count output, SD time constant changeover circuit-ON (during search of the desired station)
*1 : IF counter buffer output entered in the IF counter circuit of the PLL logic block
*2 : The rise time of AM-AGC voltage is shortened through rapid charge to the pin-25 external capacity when IFSW has been set to 1.
</td><td></td></tr>
<tr><td>(5)</td><td>FM/AM BAND switch control data
BDSW</td><td>
• Data to determine the output of the output port BDSW, controlling switching of BAND.
"Data" = 0 : AM
1 : FM
</td><td></td></tr>
</table>

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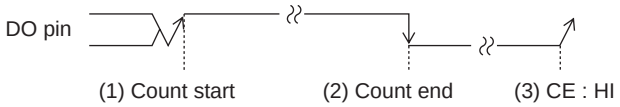
<table>
<tr><th>No.</th><th>Control/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(6)</td><td>DO pin
control data

DOC0
DOC1
DOC2</td><td>• Data to determine the output of the DO pin.
<table>
<tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>DO pin state</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Low detection of unlock</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC (See below)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Low at SD ON</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Low at stereo</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr>
</table>
• Open selected with power ON reset
* IF counter measurement end check


(1) DO pin open automatically when end-UC is set and the IF counter starts (CTE = 0→1).
(2) DO pin becomes low, enabling check of the counter end when the IF counter measurement is over.
(3) DO pin open with serial data input/output (CE pin : Hi)
Note)DO pin open regardless of the DO pin control data (DOC0 to 2) during data input period (IN1 and IN2 modes CE-Hi period).
The DO pin state allows output of the content of internal DO serial data in synchronization with CL regardless of the DO pin control data (DOC0 to 2) during data input period (OUT mode CE : Hi period).</td><td>UL0, UL1
CTE</td></tr>
<tr><td>(7)</td><td>Unlock
detection data

UL0, UL1</td><td>• Data to select the phase error (ϕE) detection width to determine if PLL is locked. Unlock is determined when the phase error exceeding the detection width occurs.
(* : don't care)
<table>
<tr><th>UL1</th><th>UL0</th><th>ϕE Detection width</th><th>Detection output</th></tr>
<tr><td>0</td><td>0</td><td>Stop</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ϕE output directly</td></tr>
<tr><td>1</td><td>*</td><td>±6.67μs</td><td>ϕE extended by 1 to 2ms</td></tr>
</table>
* unlock : DO pin becomes Low and the serial data output becomes UL = 0.</td><td>DOC0
DOC1
DOC2</td></tr>
<tr><td>(8)</td><td>Phase
comparator
control data

DZ0, DZ1</td><td>• Data to control the dead band of phase comparator.
<table>
<tr><th>DZ1</th><th>DZ0</th><th>Deadband mode</th></tr>
<tr><td>0</td><td>0</td><td>DZA</td></tr>
<tr><td>0</td><td>1</td><td>DZB</td></tr>
<tr><td>1</td><td>0</td><td>DZC</td></tr>
<tr><td>1</td><td>1</td><td>DZD</td></tr>
</table>
Dead band : DZA < DZB < DZC < DZD</td><td></td></tr>
<tr><td>(9)</td><td>Output port data

$\overline{BO1}$</td><td>• Data to determine the output of output ports $\overline{BO1}$
"Data" = 0 : OPEN
1 : Low</td><td></td></tr>
<tr><td>(10)</td><td>Charge pump
control data

DLC</td><td>• Data for forced control of the charge pump output
<table>
<tr><th>DLC</th><th>Charge pump output</th></tr>
<tr><td>0</td><td>Normal operation</td></tr>
<tr><td>1</td><td>Forced Low</td></tr>
</table>
When the VCO control voltage (Vtune) develops dead lock because of stop of oscillation of VCO at 0V, set the charge pump output to LOW and Vtune to V_{CC} to escape the dead lock. (Dead lock clear circuit)</td><td></td></tr>
<tr><td>(11)</td><td>IFS</td><td>• Normally, set data = 1. Setting the data = 0 causes worsening of the input sensitivity, resulting in decrease of the sensitivity by about 10 to 30mVrms.</td><td></td></tr>
<tr><td>(12)</td><td>LSI test data

TEST0 to 2</td><td>• LSI test data
TEST0
TEST1
TEST2 ┘ All to be set to "0"
All set to 0 for power ON reset</td><td></td></tr>
<tr><td>(13)</td><td>DNC</td><td>• Set data = 0.</td><td></td></tr>
</table>

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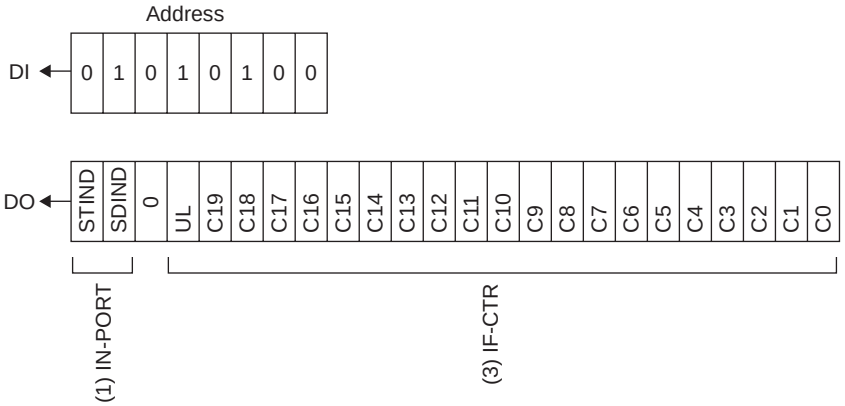
No.	Control block data	Description	Related data
(14)	Forced monaural control data STSW	• Data to determine the output of the output port STSW, controlling the forced monaural stereo function "Data" = 0 : MONO 1 : STEREO	
(15) (16)	SD sensitivity adjustment data SDC0 SDC1	• Data to determine the output of output ports SDC0 and SDC1, setting the SD sensitivity "Data" = SDC0 : 0, SDC1 : 0 → SD sensitivity = 37dBμV (Typ) SDC0 : 0, SDC1 : 1 → SD sensitivity = 40dBμV (Typ) SDC0 : 1, SDC1 : 0 → SD sensitivity = 46dBμV (Typ) SDC0 : 1, SDC1 : 1 → SD sensitivity = 51dBμV (Typ)	

Composition of the DO control data (serial data output)

(1) OUT mode

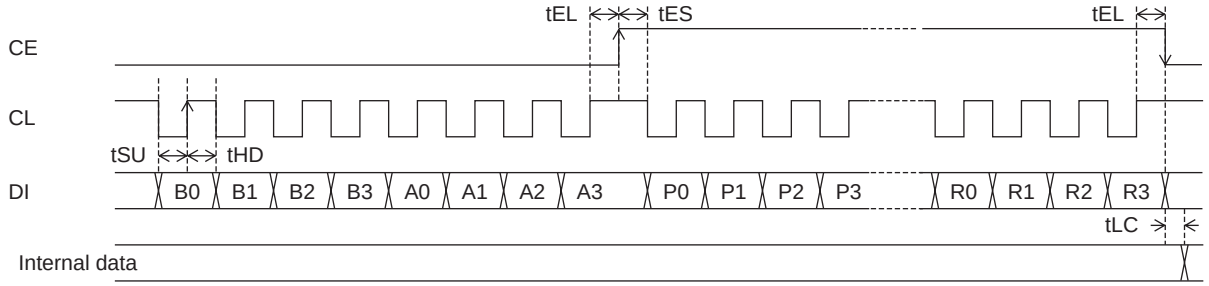


Description of DO output data

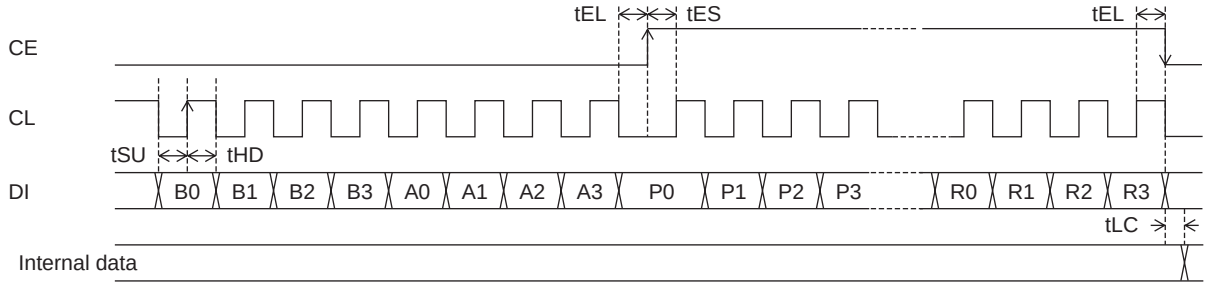
No.	Control/data	Description	Related data
(1)	Stereo indicator SD indicator Control data STIND, SDIND	• Data latching stereo indicator and SI indicator states. Latch made at a time of the data output mode (OUT mode). STIND←Stereo indicator state 0 : ST ON, 1 : ST OFF SDIND←SD indicator state 0 : SD ON, 1 : SD OFF	
(2)	PLL unlock data UL	• Data latching the content of the unlock detection circuit UL←0 : At unlock 1 : At lock or detection stop mode	UL0 UL1
(3)	IF counter Binary counter C19 to C0	• Data latching the content of IF counter (20 bit binary counter) C19←MSB of binary counter C0 ←LSB of binary counter	CTE GT0 GT1

Serial data input (IN1/IN2) tSU, tHD, tEL, tES, tEH ≥ 0.75µs tLC < 0.75µs

(1) CL : normal Hi

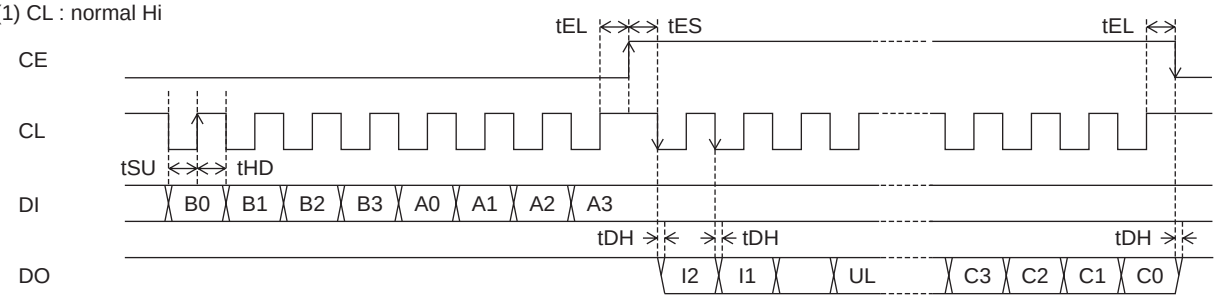


(2) CL : normal Low

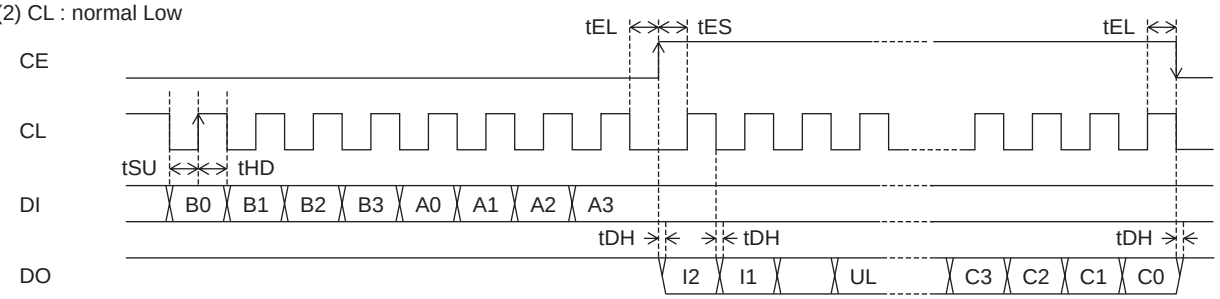


Serial data output (OUT) tSU, tHD, tEL, tES, tEH ≥ 0.75µs tDC, tDH < 0.35µs

(1) CL : normal Hi

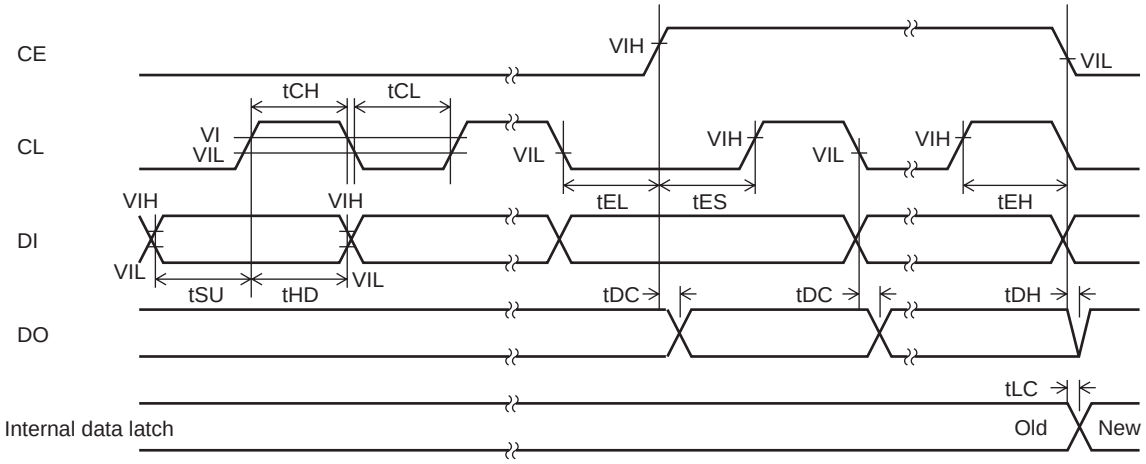


(2) CL : normal Low

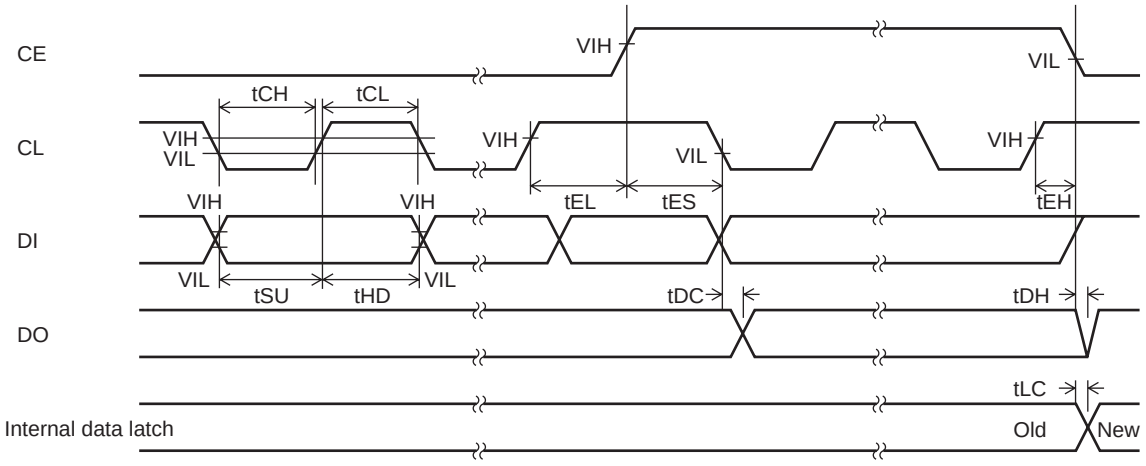


Note : The DO pin is an Nch open drain pin, so that the data change time (tDC, tDH) changes depending on the pull-up resistance and substrate capacity.

Serial data timing



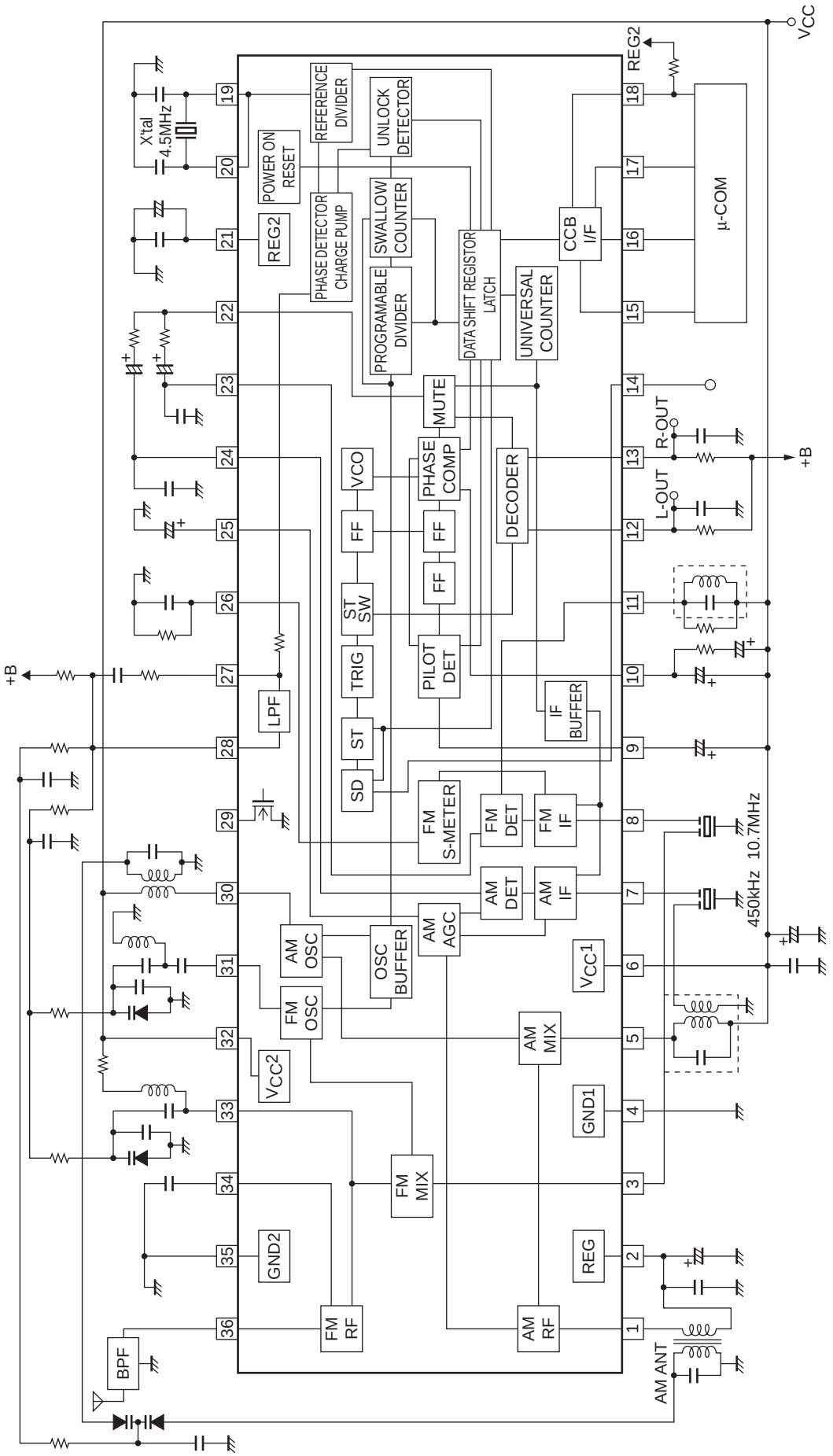
<< CL stopped at “L” level >>



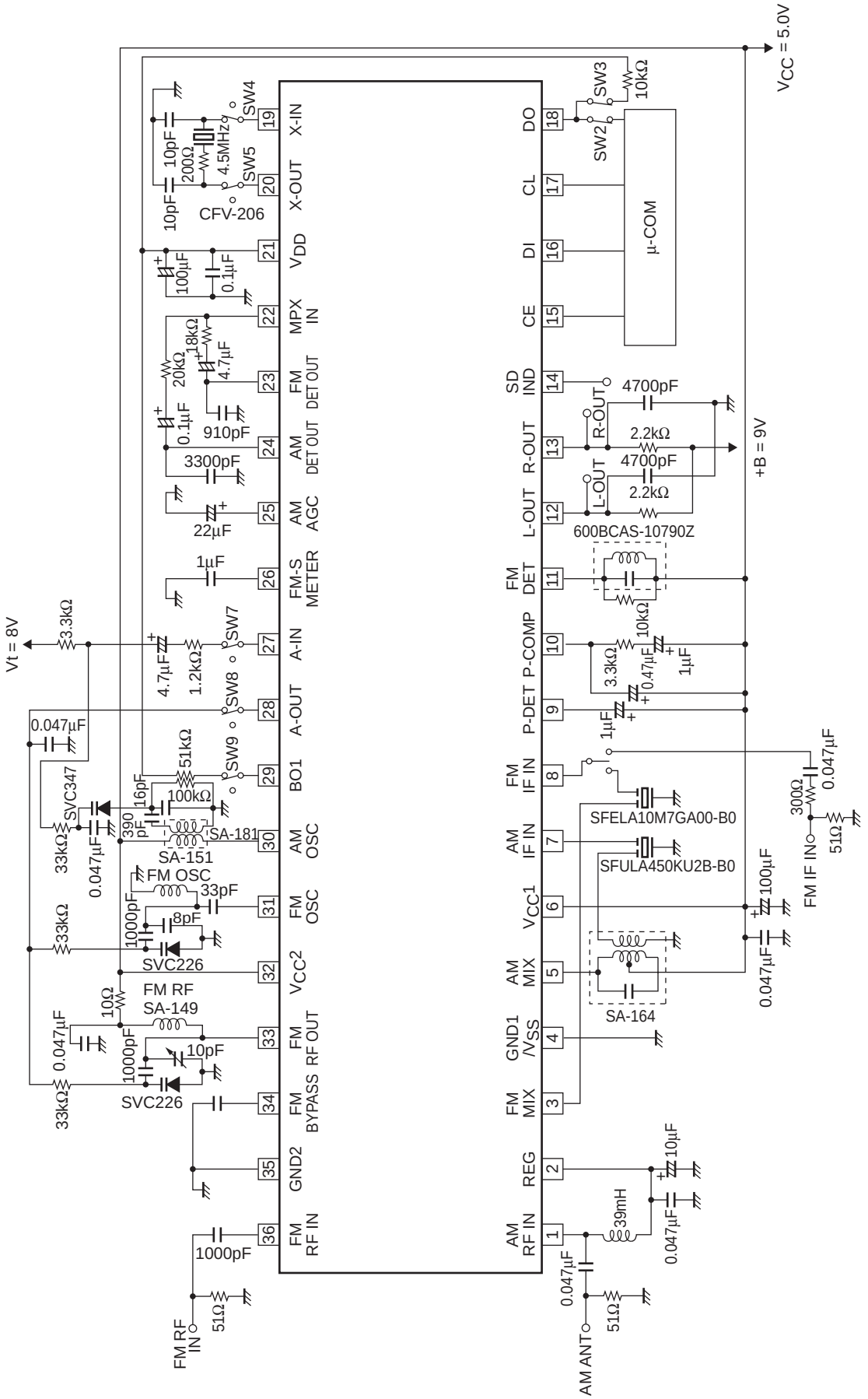
<< CL stopped at “H” level >>

Parameter	Symbol	Pin	Conditions	Min	Typ	Max	Unit
Data setup time	tSU	DI, CL		0.75			µs
Data hold time	tHD	DI, CL		0.75			µs
Clock L level time	tCL	CL		0.75			µs
Clock H level time	tCH	CL		0.75			µs
CE wait time	tEL	CE, CL		0.75			µs
CE setup time	tES	CE, CL		0.75			µs
CE hold time	tEH	CE, CL		0.75			µs
Data latch change time	tLC					0.75	µs
Data output time	tDC	DO, CL	Varies depending on the pull-up resistance and substrate capacity			0.35	µs
	tDH	DO, CE					

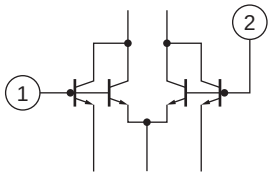
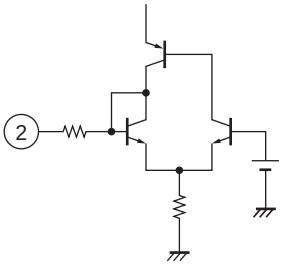
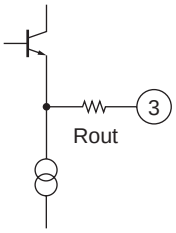
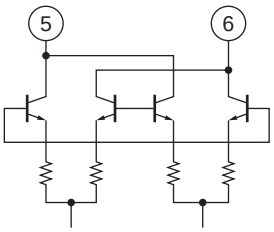
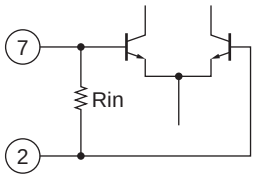
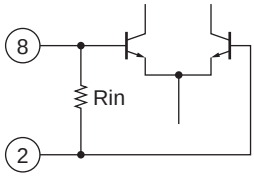
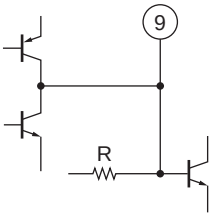
Block Diagram



Test Circuit



LV23014T Pin description and pin voltage (V_{CC} = 5.0V, +B = 9.0V)

No.	Pin name	Pin description	No input voltage (V)		Internal equivqlent circuit
			AM	FM	
1	AM RF input	Connect the AM ANT coil between this pin and pin 2 (Vreg1).	Vreg1	Vreg1	
2	REG1	Reference voltage of AM/FM, IF/MPX block	2.2	2.2	
3	FM MIX output	Rout = 270Ω	(2/3) V_{CC} -0.5	(2/3) V_{CC} -0.7	
4	GND1	GND of AM/FM, IF/MPX block	0	0	
5	AM MIX output	Connect the AM MIX coil between this pin and pin 6 (V_{CC} voltage).	V_{CC}	V_{CC}	
6	V_{CC}1	V_{CC} of AM/FM, IF/MPX block	5.0	5.0	
7	AM IF input	Rin = 2kΩ	Vreg1	Vreg1	
8	FM IF input	Rin = 330Ω	Vreg1	Vreg1	
9	Pilot filter	R = 10kΩ	V_{CC}-1	V_{CC}-1	

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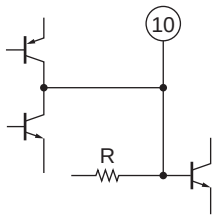
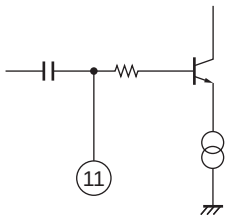
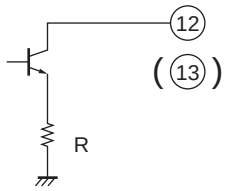
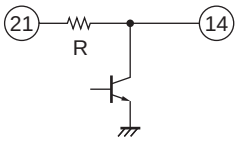
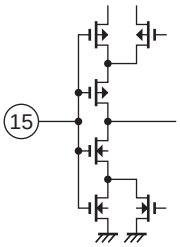
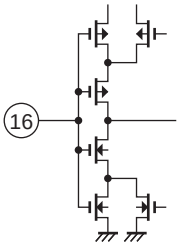
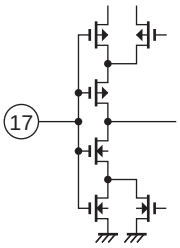
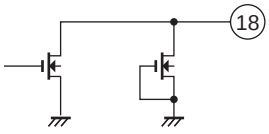
No.	Pin name	Pin description	No input voltage (V)		Internal equivqlent circuit
			AM	FM	
10	Phase comparator filter	R = 10kΩ	V_{CC}-1	V_{CC}-1	
11	FM DET	Connect the FM DET coil between this pin and pin 6 (V_{CC} voltage). Recommended detection coil : 600BCAS-10790Z by TOKO.	V_{CC}	V_{CC}	
12 13	L output R output	Resistance 2.2kΩ for output level adjustments is connected between pin 12/13 and +B (+9V). R = 600Ω	6.0 6.0	6.0 6.0	
14	SD IND	SD indicator Active low output. R = 30kΩ	Vreg2	Vreg2	
15	CE	Chip enable port At changeover from "L" to "H" address latching. At changeover from "H" to "L" data latching.			
16	DI	Serial data input port Sets data in synchronization with rise of data clock.			
17	CL	Data clock input port			
18	DO	Data output port Outputs various data in synchronization with fall of data clock in the out mode.			

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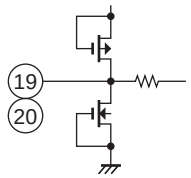
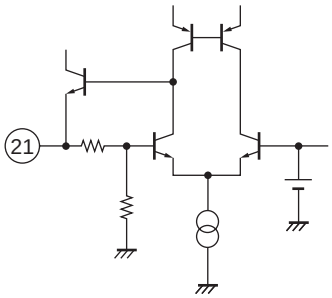
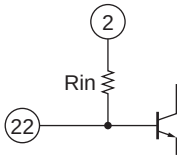
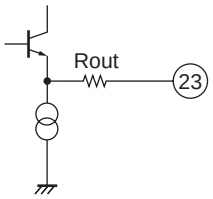
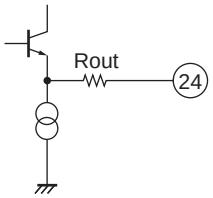
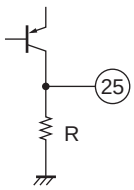
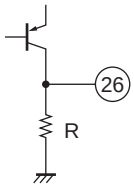
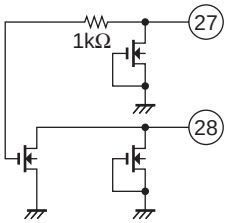
No.	Pin name	Pin description	No input voltage (V)		Internal equivqlent circuit
			AM	FM	
19 20	XIN XOUT	Clock for internal reference Connect 4.5MHz crystal oscillator.			
21	VREG2	Reference voltage of PLL block	3.0	3.0	
22	MPX input	Rin = 20kΩ	Vreg1	Vreg1	
23	FM detection output	The separation can be adjusted with an external capacitor connected between this pin and GND. Rout = 3.3kΩ	0.8	Vreg1	
24	AM detection output	AM low frequency characteristic can be adjusted with an external capacitor connected between this pin and GND. Rout = 5.0kΩ	2.0	0	
25	AM AGC output	R = 13.8kΩ	0.8	0	
26	FM S-meter output and FM SD adjust	The FMSD sencitivity can be adjusted with an external resistor connected between this pin and GND. R = 14.0kΩ	0	0.8	
27 28	AIN AOUT	Nch MOS transistor for PLL active low pass filter.			

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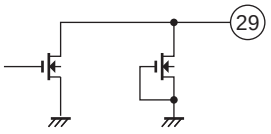
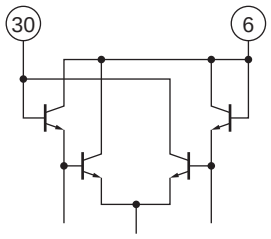
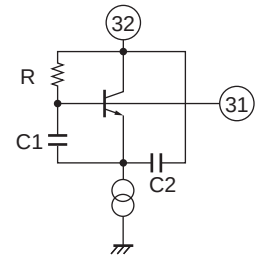
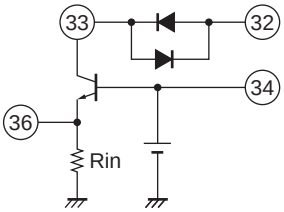
No.	Pin name	Pin description	No input voltage (V)		Internal equivqlent circuit
			AM	FM	
29	BO1	General purpose output port			
30	AM OSC	AM OSC circuit with ALC AM OSC coil used between pins 31 and 6 (V_{CC} voltage).	V_{CC}	V_{CC}	
31	FM OSC	R = 10kΩ C1 = 10pF C2 = 20pF	V_{CC}	4.95	
32	$V_{CC}2$	V_{CC} of FM FE block	5.0	5.0	
33	FM RF output	FM RF coil used between pins 33 and 32 (V_{CC} voltage).	V_{CC}	V_{CC}	
34	FM bypass	The capacity of 1000pF is connected between pins 34 and 35 (GND).	0	1.6	
35	FM RF input	Rin = 1.5kΩ	0	0.9	
35	GND2	GND of FM FE block	0	0	

Application Circuit