



N-Channel 40-V (D-S) MOSFET

| PRODUCT SUMMARY | | | |
|---------------------|-----------------------------------|---------------------------------|-----------------------|
| V _{DS} (V) | R _{DS(on)} (Ω) | I _D (A) ^a | Q _g (Typ.) |
| 40 | 0.0088 at V _{GS} = 10 V | 50 | 16 nC |
| | 0.0105 at V _{GS} = 4.5 V | 50 | |

FEATURES

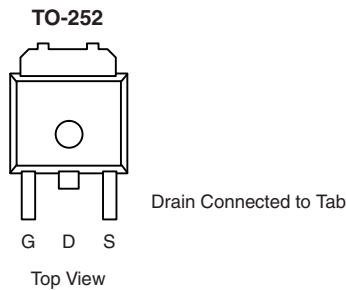
- Halogen-free
- TrenchFET[®] Power MOSFET
- 100 % UIS Tested
- 100 % R_g Tested
- PWM Optimized



RoHS COMPLIANT

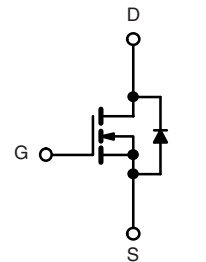
APPLICATIONS

- LCD Display Backlight Inverters
- DC/DC Converters



Ordering Information:

SUD50N04-8m8P-4GE3 (Lead (Pb)-free and Halogen-free)



| ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted | | | | |
|---|-----------------------------------|------------------------|-------------------|---|
| Parameter | Symbol | Limit | Unit | |
| Drain-Source Voltage | V _{DS} | 40 | V | |
| Gate-Source Voltage | V _{GS} | ± 20 | | |
| Continuous Drain Current (T _J = 150 °C) | I _D | T _C = 25 °C | 50 ^a | A |
| | | T _C = 70 °C | 44 | |
| | | T _A = 25 °C | 14 ^b | |
| | | T _A = 70 °C | 11.2 ^b | |
| Pulsed Drain Current | I _{DM} | 100 | | |
| Continuous Source-Drain Diode Current | I _S | T _C = 25 °C | 40 | |
| | | T _A = 25 °C | 2.6 ^b | |
| Single Pulse Avalanche Current | I _{AS} | 30 | | |
| Avalanche Energy | E _{AS} | 45 | mJ | |
| Maximum Power Dissipation | P _D | T _C = 25 °C | 48.1 | W |
| | | T _C = 70 °C | 30.8 | |
| | | T _A = 25 °C | 3.1 ^b | |
| | | T _A = 70 °C | 2.0 ^b | |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | - 55 to 150 | °C | |

| THERMAL RESISTANCE RATINGS | | | | | |
|--|-------------------|---------|---------|------|--|
| Parameter | Symbol | Typical | Maximum | Unit | |
| Maximum Junction-to-Ambient ^b | R _{thJA} | 32 | 40 | °C/W | |
| Maximum Junction-to-Case | R _{thJC} | 2.1 | 2.6 | | |

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

| SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted | | | | | | |
|---|-------------------------|---|--|--------|-----------|----------------------|
| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
| Static | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | 40 | | | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | $I_D = 1.0\text{ mA}$ | | 44 | | mV/ $^\circ\text{C}$ |
| $V_{GS(th)}$ Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | | | - 5.9 | | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | 1.0 | | 3.0 | V |
| Gate-Source Leakage | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$ | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$ | | | 1 | μA |
| | | $V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ }^\circ\text{C}$ | | | 20 | |
| On-State Drain Current ^a | $I_{D(on)}$ | $V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$ | 50 | | | A |
| Drain-Source On-State Resistance ^a | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 20\text{ A}$ | | 0.0069 | 0.0088 | Ω |
| | | $V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$ | | 0.0084 | 0.0105 | |
| Forward Transconductance ^a | g_{fs} | $V_{DS} = 15\text{ V}, I_D = 15\text{ A}$ | | 75 | | S |
| Dynamic^b | | | | | | |
| Input Capacitance | C_{iss} | $V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | | 2400 | | pF |
| Output Capacitance | C_{oss} | | | 260 | | |
| Reverse Transfer Capacitance | C_{rss} | | | 100 | | |
| Total Gate Charge | Q_g | $V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$ | | 37 | 56 | nC |
| | | | $V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$ | | 16 | |
| Gate-Source Charge | Q_{gs} | | | 6.5 | | |
| Gate-Drain Charge | Q_{gd} | | 4.5 | | | |
| Gate Resistance | R_g | $f = 1\text{ MHz}$ | 2.5 | 5.5 | 8.5 | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 20\text{ V}, R_L = 1\text{ }\Omega$ $I_D \cong 20\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$ | | 30 | 45 | ns |
| Rise Time | t_r | | | 15 | 25 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 45 | 70 | |
| Fall Time | t_f | | | 15 | 25 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 20\text{ V}, R_L = 1\text{ }\Omega$ $I_D \cong 20\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$ | | 9 | 15 | |
| Rise Time | t_r | | | 5 | 10 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 40 | 60 | |
| Fall Time | t_f | | | 5 | 10 | |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I_S | $T_C = 25\text{ }^\circ\text{C}$ | | | 40 | A |
| Pulse Diode Forward Current ^a | I_{SM} | | | | 100 | |
| Body Diode Voltage | V_{SD} | $I_S = 10\text{ A}$ | | 0.81 | 1.2 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $I_F = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$ | | 22 | 35 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | 14 | 25 | nC |
| Reverse Recovery Fall Time | t_a | | | 11 | | ns |
| Reverse Recovery Rise Time | t_b | | | 11 | | |

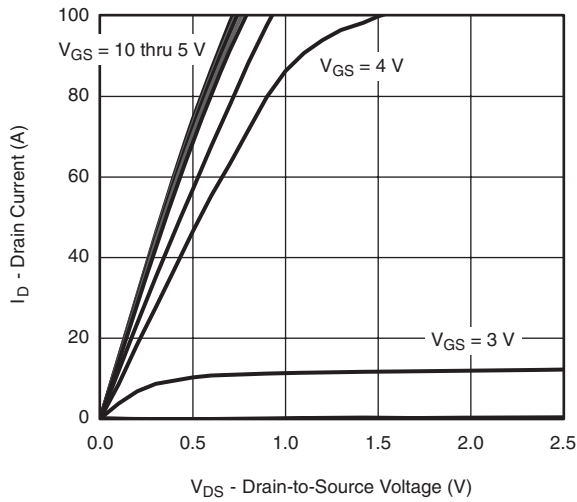
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

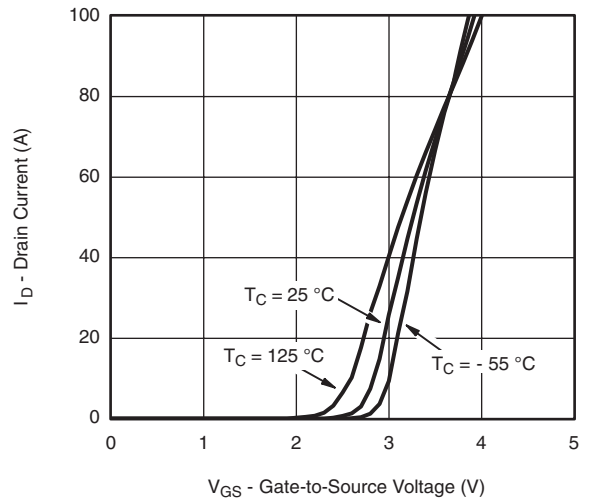
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



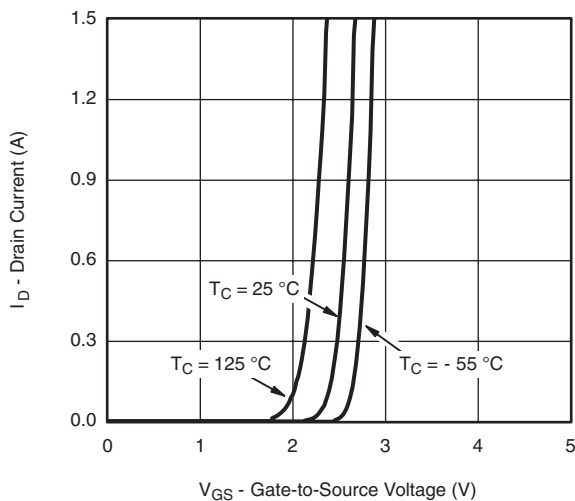
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



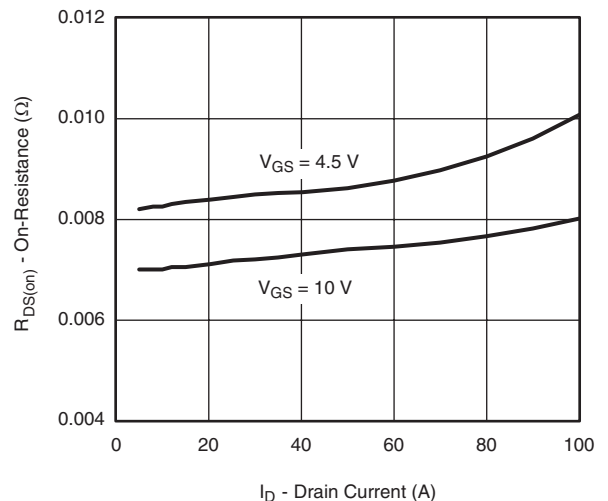
Output Characteristics



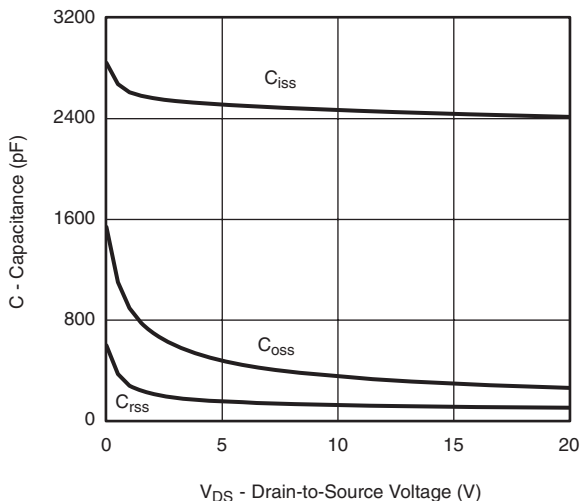
Transfer Characteristics



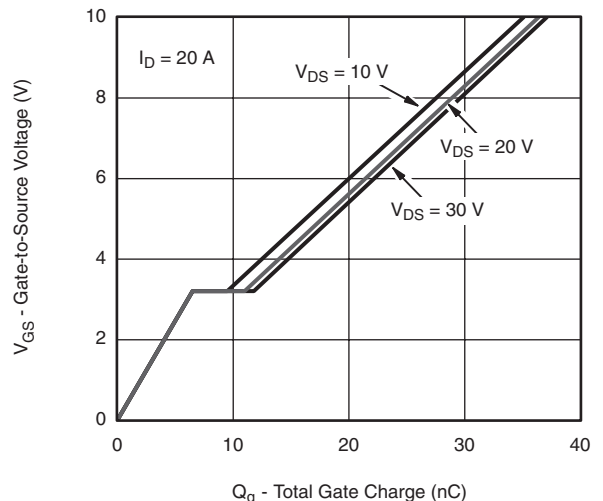
Transfer Characteristics



On-Resistance vs. Drain Current



Capacitance



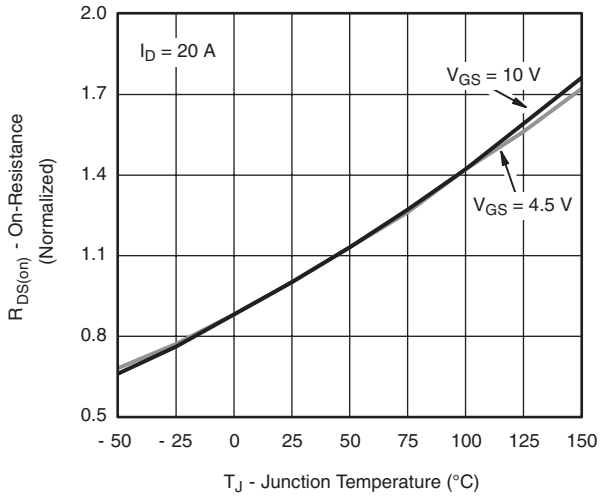
Gate Charge

SUD50N04-8m8P

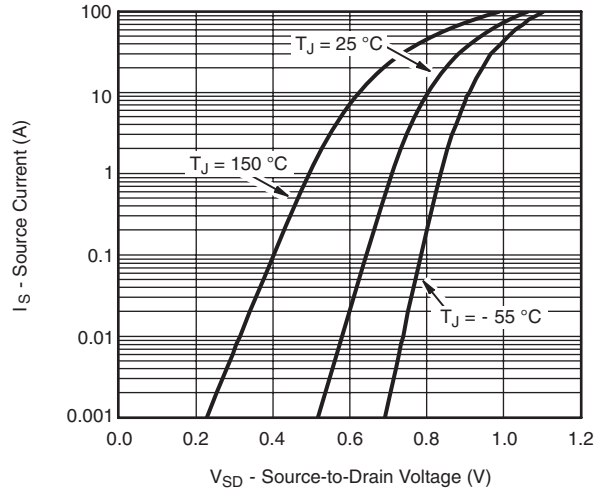


Vishay Siliconix

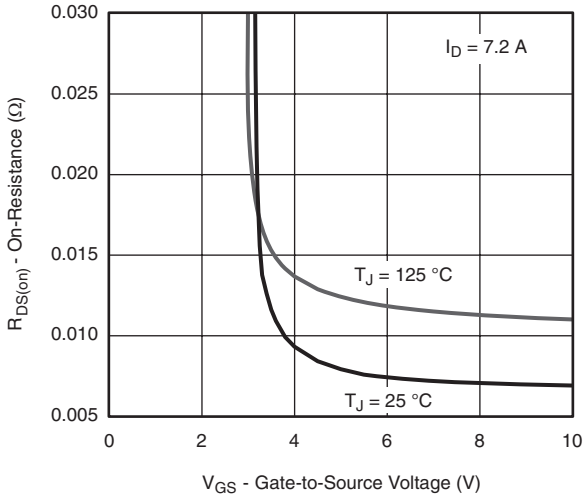
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



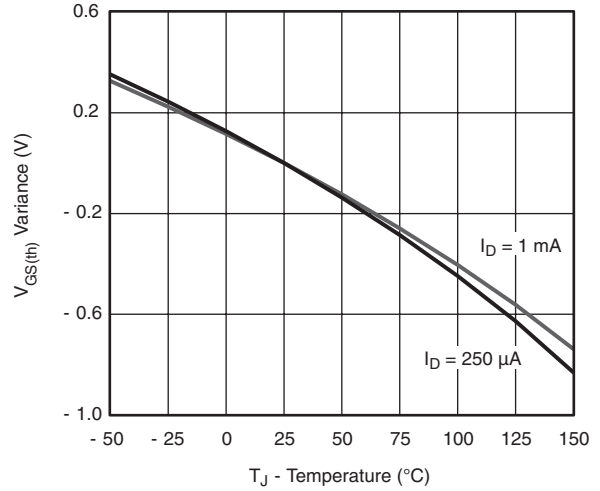
On-Resistance vs. Junction Temperature



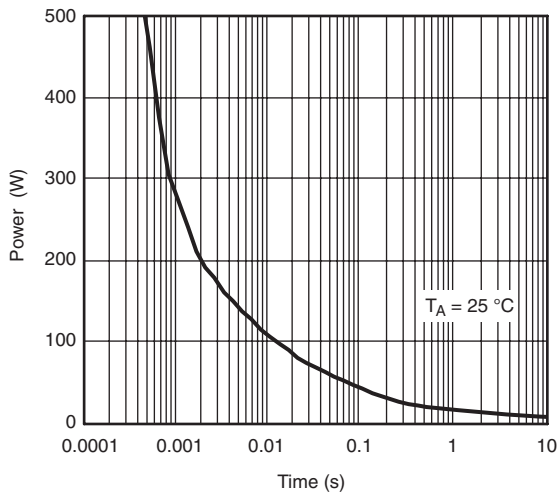
Source-Drain Diode Forward Voltage



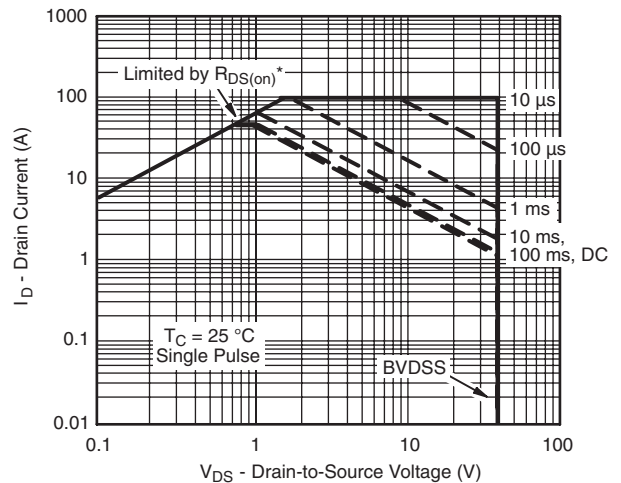
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



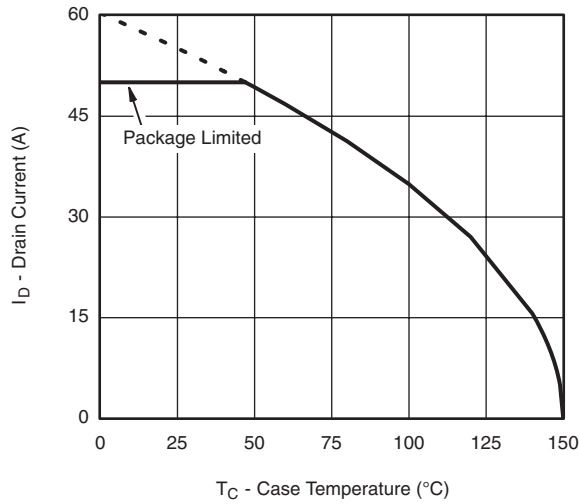
Single Pulse, Junction-to-Ambient



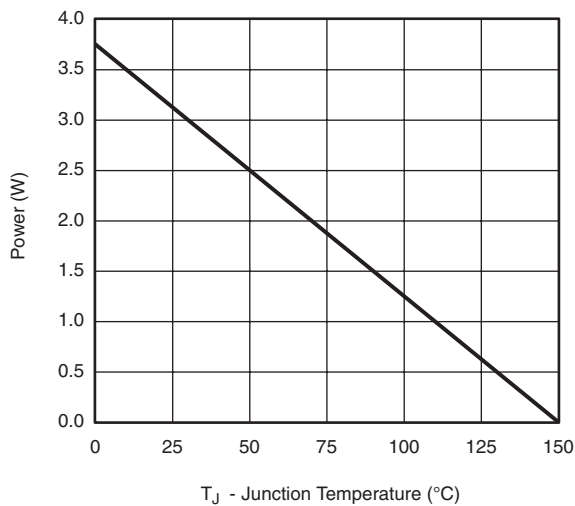
Safe Operating Area, Junction-to-Case



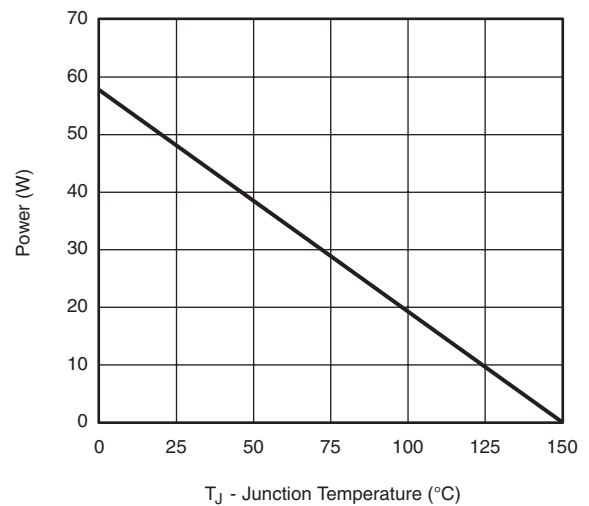
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*, Junction-to-Case



Power Derating, Junction-to-Ambient



Power Derating, Junction-to-Case

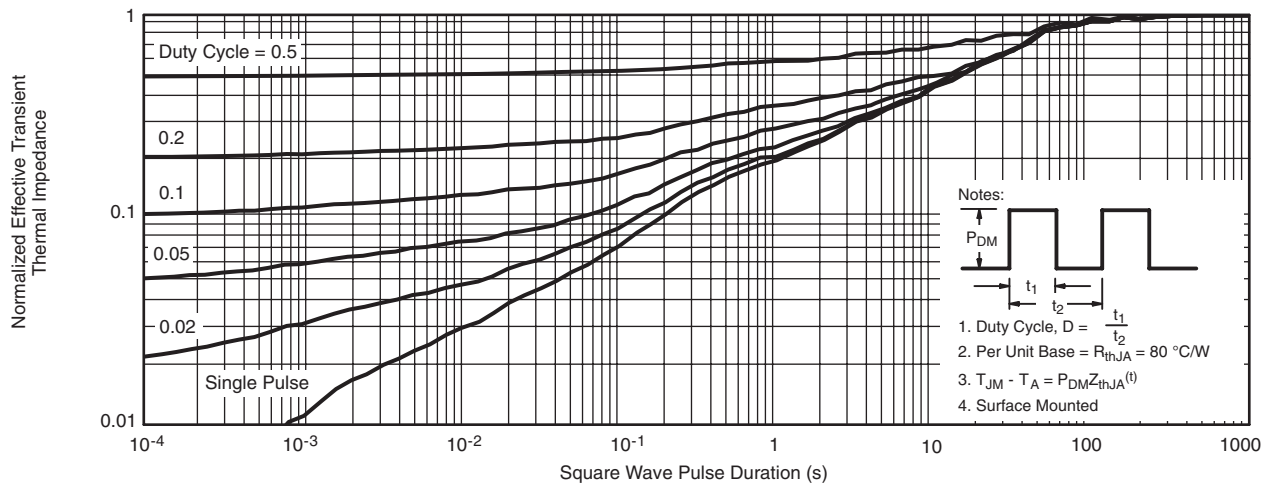
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

SUD50N04-8m8P

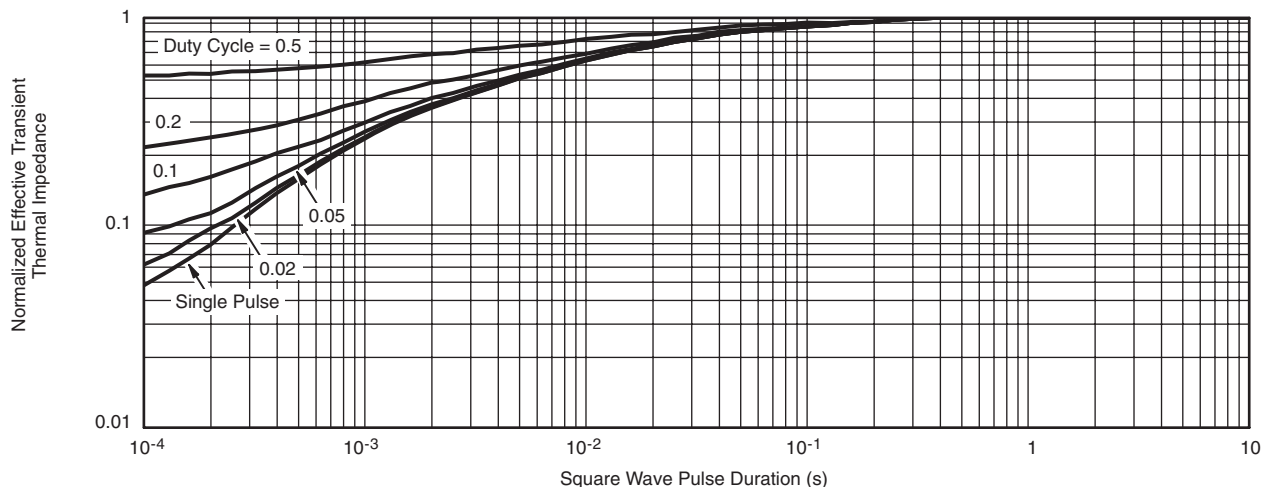
Vishay Siliconix



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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