PCF8534A

Universal LCD driver for low multiplex rates

Rev. 00.90 — 4 February 2008 Product data sheet

1. General description

The PCF8534A is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 60 segments and can easily be cascaded for larger LCD applications. The PCF8534A is compatible with most microprocessors / microcontrollers and communicates via a two-line bidirectional I^2C-bus. Communication overheads are minimized using a display RAM with auto-incremented addressing, hardware subaddressing and display memory switching (static and duplex drive modes).

2. Features

- Single-chip LCD controller / driver
- Selectable backplane drive configuration: static or 2 / 3 / 4 backplane multiplexing
- 60 segment drives: up to thirty 8-segment numeric characters; up to sixteen 15-segment alphanumeric characters; or any graphics of up to 240 elements
- May be cascaded for larger applications
- 60 × 4-bit RAM for display data storage
- Wide LCD supply range: from 2.5 V for low threshold LCDs and up to 6.5 V for guest-host LCDs and high threshold (automobile) twisted nematic LCDs
- Internal LCD bias generation with voltage-follower buffers
- Selectable display bias configuration: static, ½ or ⅓
- Wide logic power supply range: from 1.8 to 5.5 V
- LCD and logic supplies may be separated
- Low power consumption
- 400 kHz I^2C-bus interface
- Compatible with 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- No external components
- Display memory bank switching in static and duplex drive modes
- Auto-incremented display data loading across device subaddress boundaries
- Versatile blinking modes
- TTL/CMOS compatible
- Manufactured in silicon gate CMOS process
- Automotive AEC-Q100 compliant.

3. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCF8534AH	PCF8534AH	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

4. Block diagram

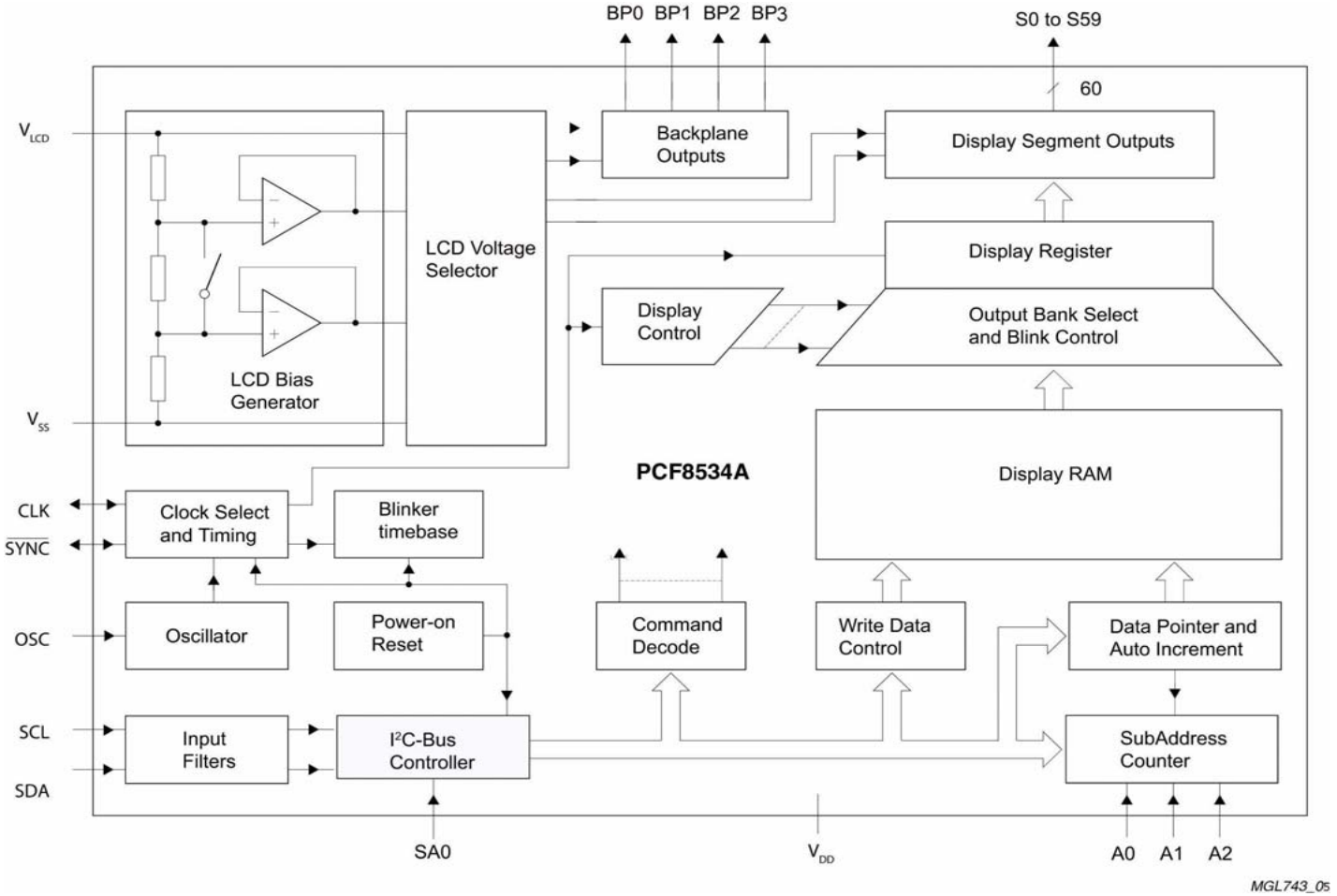


Fig 1. PCF8534A block diagram

5. Pinning information

5.1 Pinning

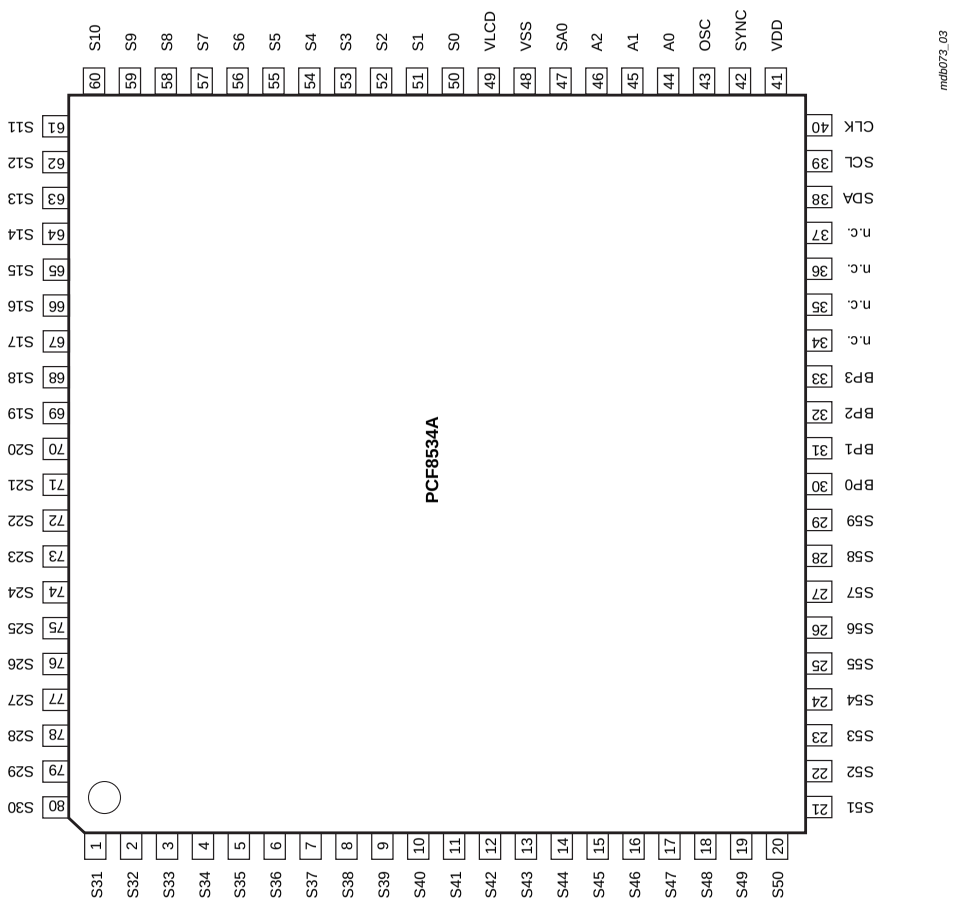


Fig 2. PCF8534A pin configuration

Table 2. Pin allocation table

Pin	Symbol	Pin	Symbol
1	S31	41	V_{DD}
2	S32	42	SYNC
3	S33	43	OSC
4	S34	44	A0
5	S35	45	A1
6	S36	46	A2
7	S37	47	SA0
8	S38	48	V_{SS}
9	S39	49	V_{LCD}
10	S40	50	S0
11	S41	51	S1
12	S42	52	S2
13	S43	53	S3
14	S44	54	S4
15	S45	55	S5
16	S46	56	S6
17	S47	57	S7
18	S48	58	S8
19	S49	59	S9
20	S50	60	S10
21	S51	61	S11
22	S52	62	S12
23	S53	63	S13
24	S54	64	S14
25	S55	65	S15
26	S56	66	S16
27	S57	67	S17
28	S58	68	S18
29	S59	69	S19
30	BP0	70	S20
31	BP1	71	S21
32	BP2	72	S22
33	BP3	73	S23
34	n.c.	74	S24
35	n.c.	75	S25
36	n.c.	76	S26
37	n.c.	77	S27
38	SDA	78	S28
39	SCL	79	S29
40	CLK	80	S30

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
SDA	38	I^2C-bus serial data input / output
SCL	39	I^2C-bus serial clock input
CLK	40	external clock input / output
V_{DD}	41	supply voltage
SYNC	42	cascade synchronization input / output
OSC	43	internal oscillator enable input
A0, A1 and A2	44 to 46	subaddress inputs
SA0	47	I^2C-bus slave address input: [0]
V_{SS}	48	logic ground
V_{LCD}	49	LCD supply voltage
BP0, BP1, BP2 and BP3	30 to 33	LCD backplane outputs
S0 to S59	50 to 80 and 1 to 29	LCD segment outputs

6. Device protection diagram

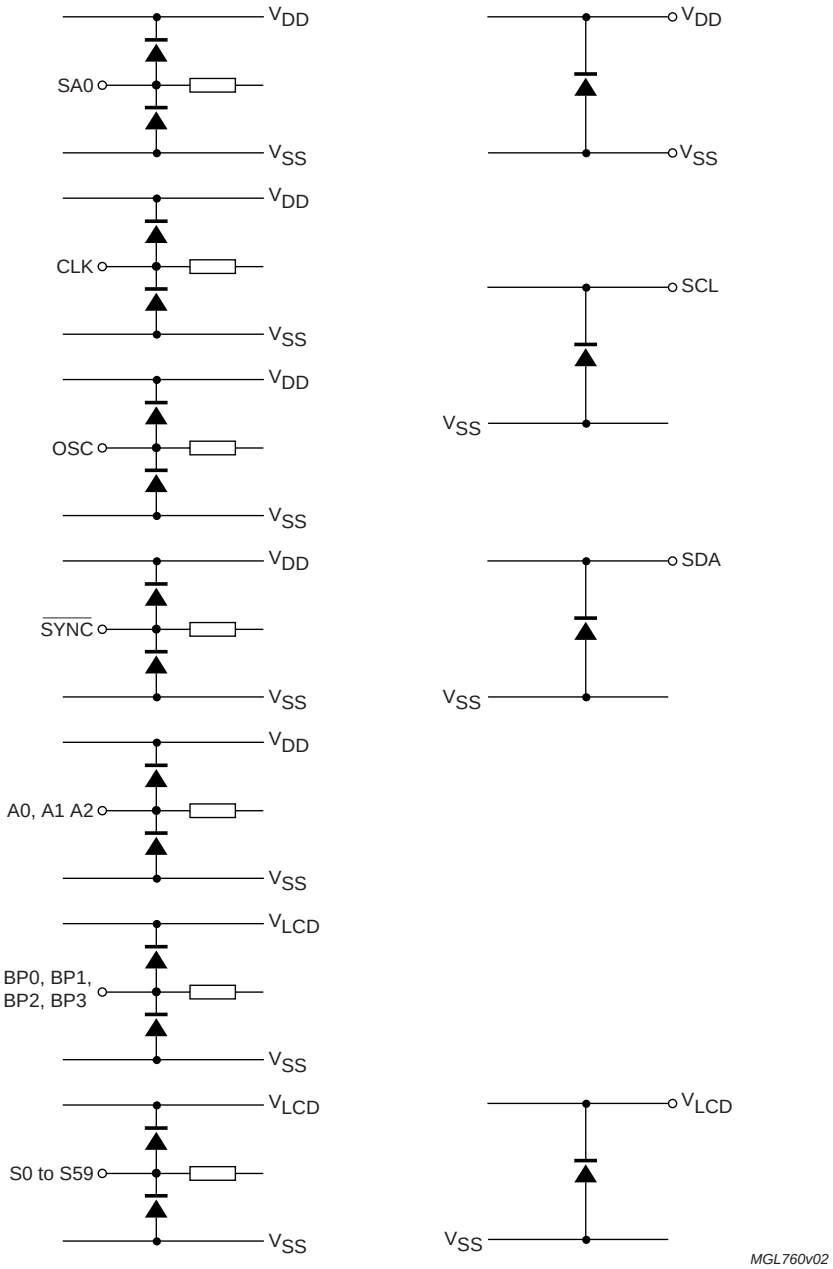


Fig 3. Device protection diagram

7. Functional description

The PCF8534A is a versatile peripheral device designed to interface any microprocessor / microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 60 segments.
The display configurations possible with the PCF8534A depend on the number of active backplane outputs required; a selection of display configurations is given in Table 4.

All of the display configurations given in Table 4 can be implemented in the typical system shown in Figure 4.

The host microprocessor / microcontroller maintains the 2-line I²C-bus communication channel with the PCF8534A. The internal oscillator is selected by connecting pin OSC to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the power supplies (V_{DD}, V_{SS} and V_{LCD}) and the LCD panel selected for the application.

Table 4. Selection of display configurations

Number of		7 segment numeric		14 segment numeric		Dot matrix
Backplanes	Segments	Digits	Indicator symbols	Characters	Indicator symbols	
4	240	30	30	16	16	240 (4 × 60)
3	180	22	26	12	12	180 (3 × 60)
2	120	15	15	8	8	120 (2 × 60)
1	60	7	11	4	4	60 (1 × 60)

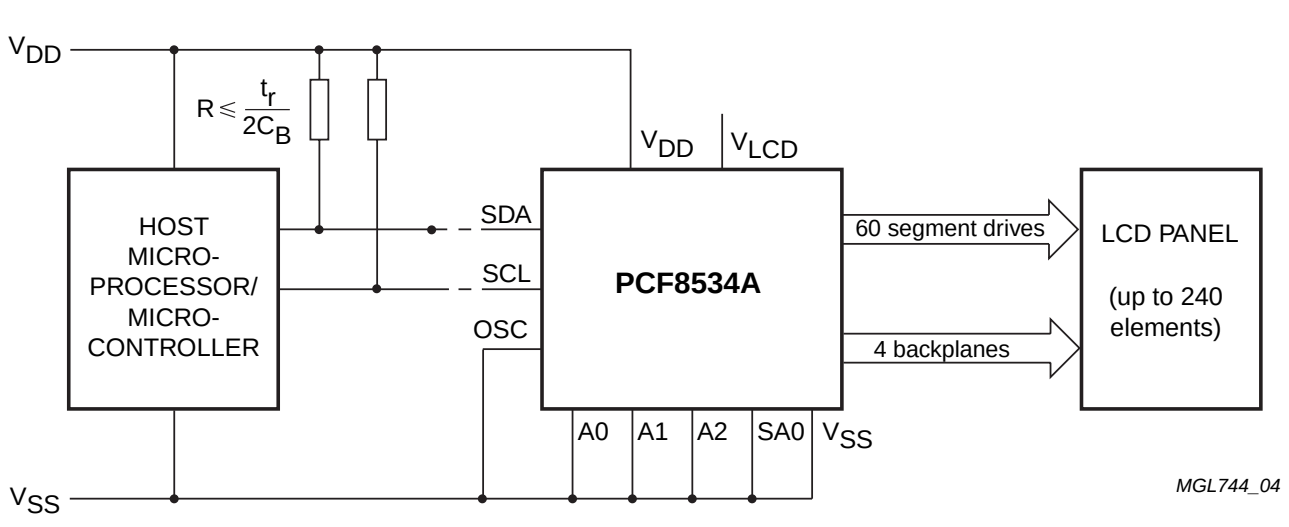


Fig 4. Typical system configuration

7.1 Power-on reset

At power on the PCF8534A resets to a starting condition as follows:

1. All backplane outputs are set to V_{LCD}.
2. All segment outputs are set to V_{LCD}.
3. The drive mode '1 : 4 multiplex with ⅓ bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset.
6. The I²C-bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.
8. Display disabled.

Data transfers on the I^2C-bus must be avoided for 1 ms following power-on to allow completion of the reset action.

7.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of the three series resistors connected between V_{LCD} and V_{SS}. The center resistor can be switched out of the circuit to provide a ½ bias voltage level for the 1:2 multiplex configuration.

7.3 LCD voltage selector

The LCD voltage selector co-ordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder.

The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{OP} and the resulting discrimination ratios (D), are shown in Table 5.

A practical value for V_{OP} is determined by equating $V_{OFF(rms)}$ with a defined LCD threshold voltage (V_{TH}), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{OP} > 3\ V_{TH}$.

Multiplex drive ratios of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller e.g.:

$$\sqrt{3} = 1.732 \text{ for 1:3 multiplex or } \left(\frac{\sqrt{21}}{3} = 1.528\right) \text{for 1:4 multiplex}$$

The advantage of these modes is a reduction of the LCD full-scale voltage V_{OP} as follows:

- 1:3 multiplex (½ bias): $V_{OP} = \sqrt{6} \times V_{OFF(rms)} = 2.449 V_{OFF(rms)}$
- 1:4 multiplex (½ bias): $V_{OP} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{OFF(rms)}$

These compare with $V_{OP} = 3 \times V_{OFF(rms)}$ when ⅓ bias is used. Note: $V_{OP} = V_{LCD}$.

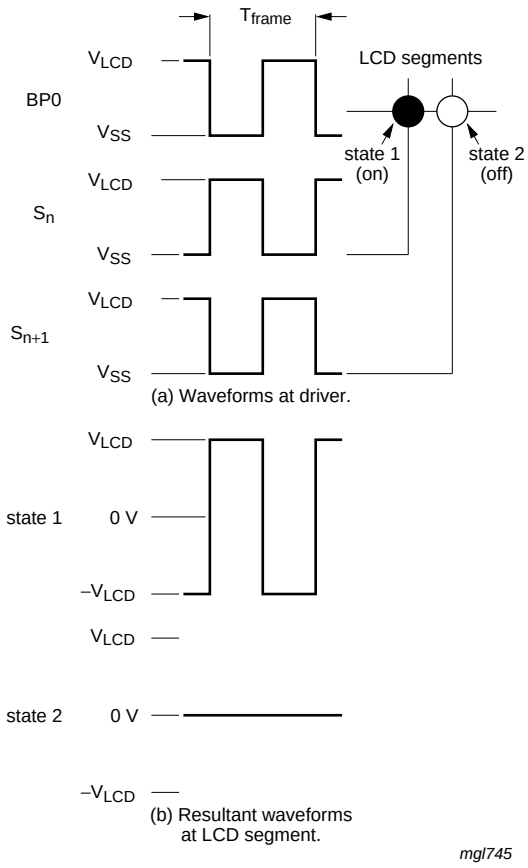
Table 5. Preferred LCD drive modes: summary of characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{OFF(ms)}}{V_{OP}}$	$\frac{V_{ON(ms)}}{V_{OP}}$	$D = \frac{V_{ON(ms)}}{V_{OFF(ms)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2	2	3	½	0.354	0.791	2.236
1:2	2	4	⅓	0.333	0.745	2.236
1:3	3	4	⅓	0.333	0.638	1.915
1:4	4	4	⅓	0.333	0.577	1.732

7.4 LCD drive mode waveforms

7.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Figure 5.



$V_{state1}(t) = V_{sn}(t) - V_{BP0}(t)$.

$V_{ON(rms)} = V_{LCD}$.

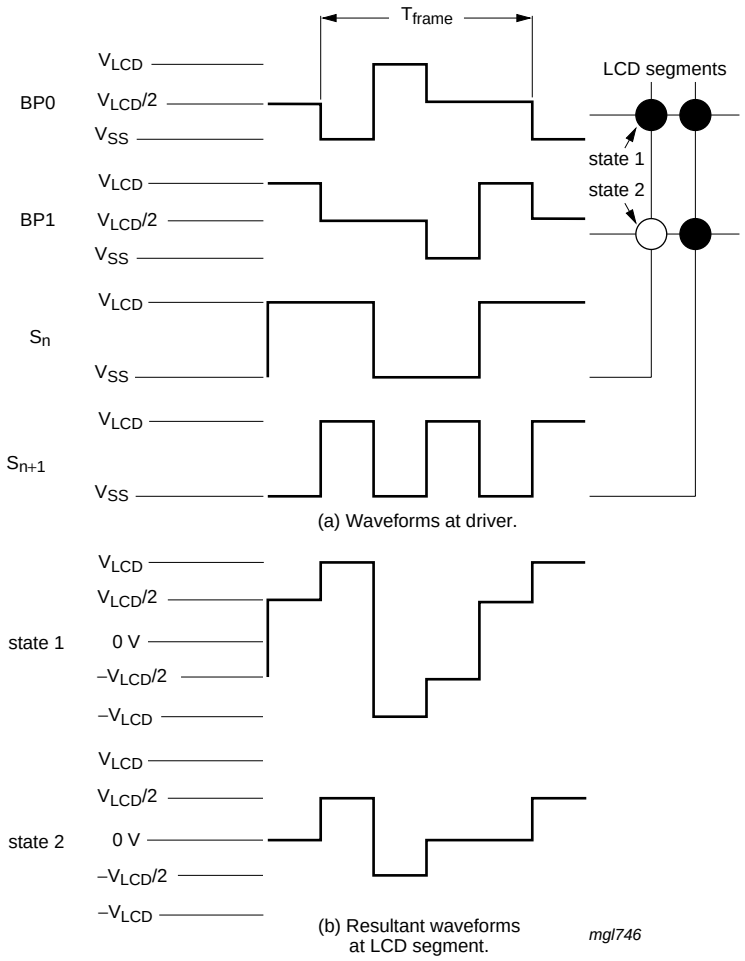
$V_{state2}(t) = V_{(sn + 1)}(t) - V_{BP0}(t)$.

$V_{OFF(rms)} = 0$ V.

Fig 5. Static drive mode waveforms

7.4.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCF8534A allows the use of ½ bias or ⅓ bias in this mode as shown in Figure 6 and Figure 7.



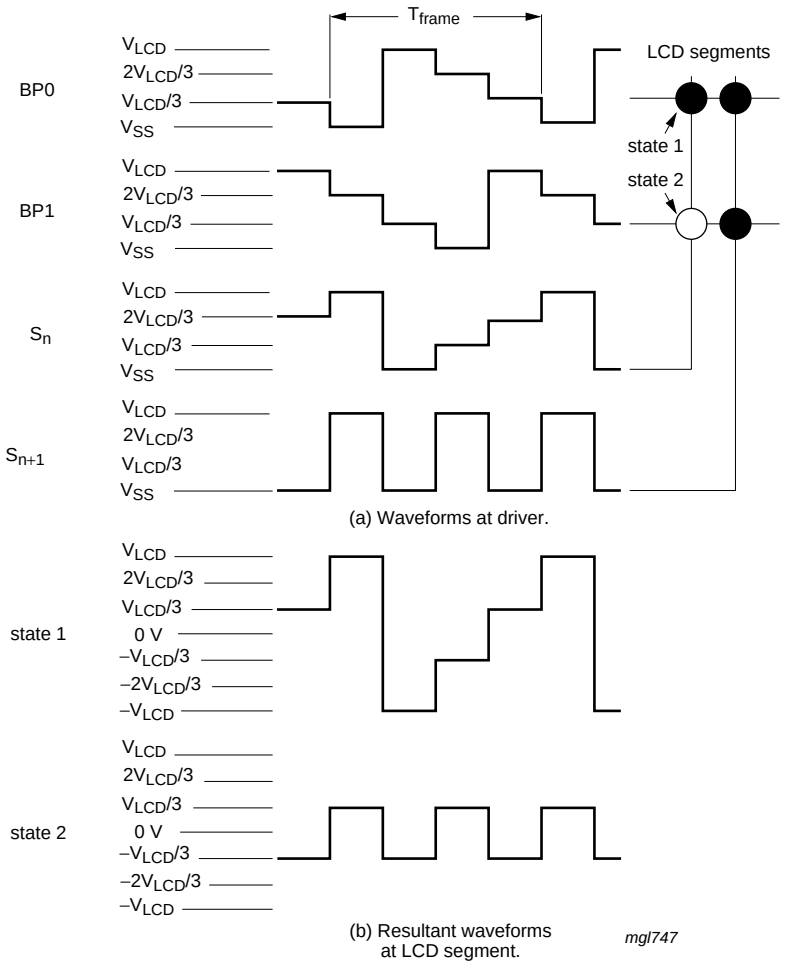
$V_{state1}(t) = V_{sn}(t) - V_{BP0}(t)$.

$V_{ON(rms)} = 0.791\ V_{LCD}$.

$V_{state2}(t) = V_{(sn)}(t) - V_{BP1}(t)$.

$V_{OFF(rms)} = 0.354\ V_{LCD}$.

Fig 6. Waveforms for the 1:2 multiplex drive mode with ½ bias



$V_{state1}(t) = V_{sn}(t) - V_{BP0}(t)$.

$V_{ON(rms)} = 0.745\ V_{LCD}$.

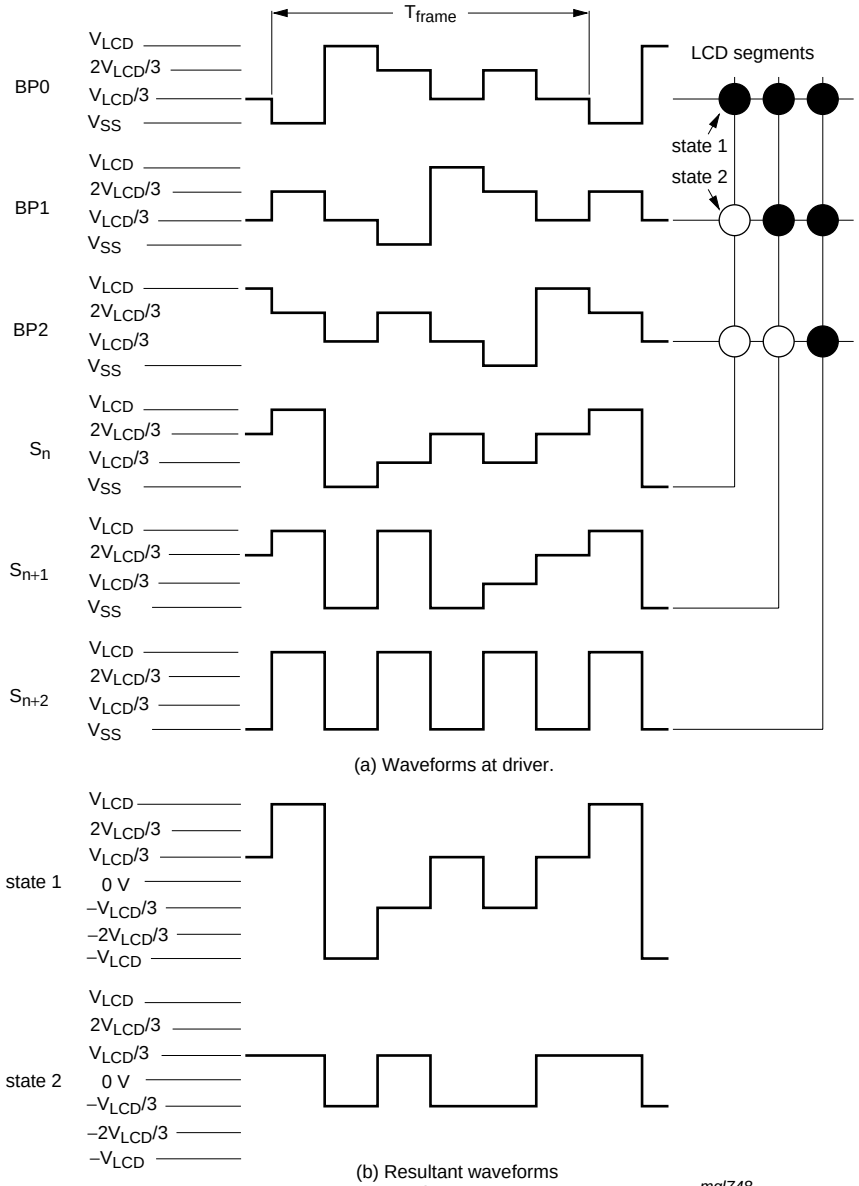
$V_{state2}(t) = V_{(sn)}(t) - V_{BP1}(t)$.

$V_{OFF(rms)} = 0.333\ V_{LCD}$.

Fig 7. Waveforms for the 1:2 multiplex drive mode with $\frac{1}{3}$ bias

7.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in Figure 8.



$V_{state1}(t) = V_{sn}(t) - V_{BP0}(t)$.

$V_{ON(rms)} = 0.638\ V_{LCD}$.

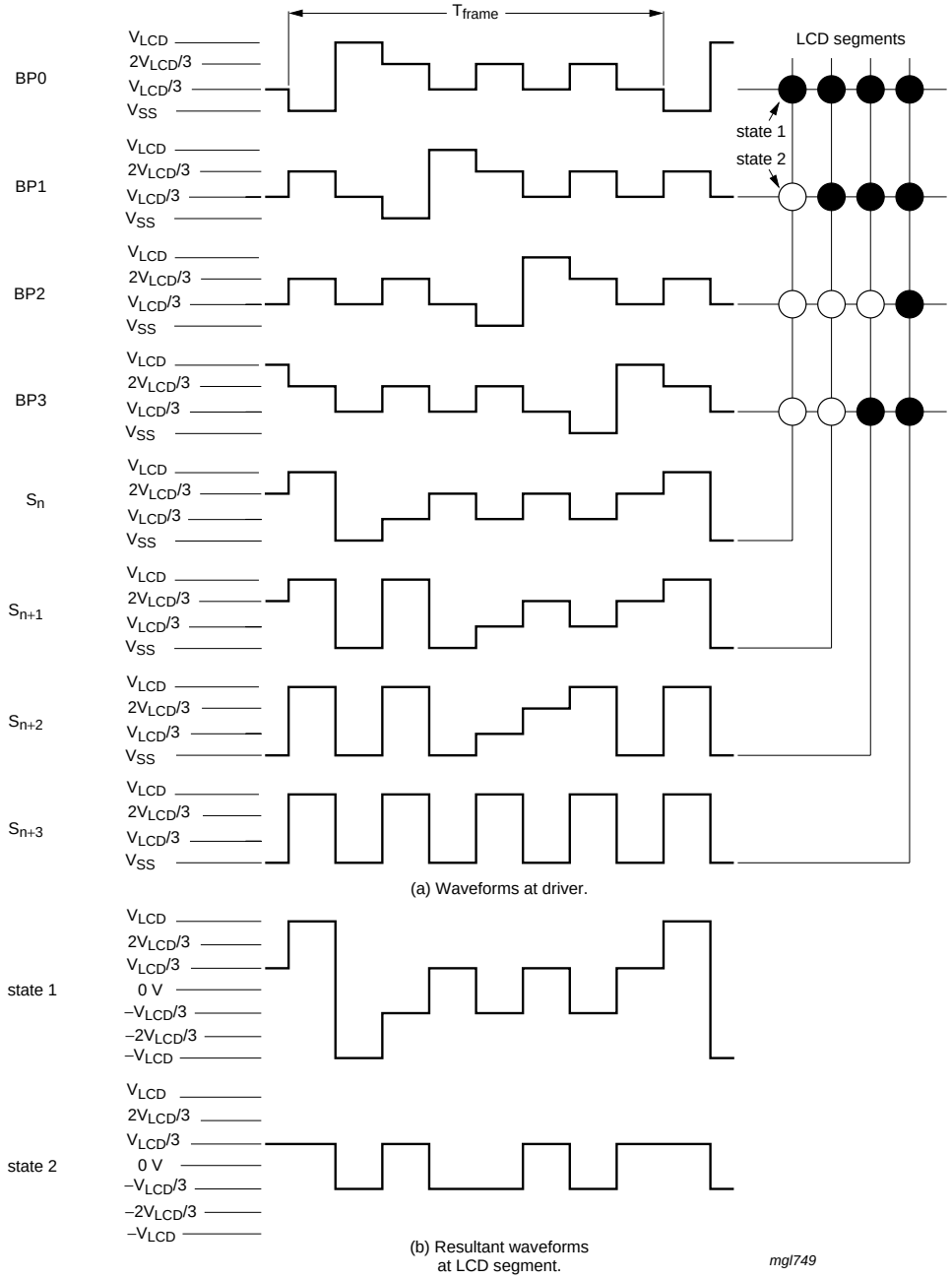
$V_{state2}(t) = V_{(sn)}(t) - V_{BP1}(t)$.

$V_{OFF(rms)} = 0.333\ V_{LCD}$.

Fig 8. Waveforms for the 1:3 multiplex drive mode

7.4.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Figure 9.



$V_{state1}(t) = V_{sn}(t) - V_{BP0}(t)$.

$V_{ON(rms)} = 0.577\ V_{LCD}$.

$V_{state2}(t) = V_{(sn)}(t) - V_{BP1}(t)$.

$V_{OFF(rms)} = 0.333\ V_{LCD}$.

Fig 9. Waveforms for the 1:4 multiplex drive mode

7.5 Oscillator

7.5.1 Internal clock

The internal logic and the LCD drive signals of the PCF8534A are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, you must connect pin OSC to V_{SS}. In this event, the output from pin CLK provides the clock signal for cascaded PCF8534As in the system. After power-up, SDA must be HIGH to guarantee that the clock starts.

7.5.2 External clock

The condition for external clock is made by tying pin OSC to V_{DD}; pin CLK then becomes the external clock input.

The clock frequency (f_{CLK}) determines the LCD frame frequency.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

7.6 Timing

The timing of the PCF8534A organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications the synchronization signal ($\overline{SYNC}$) maintains the correct timing relationship between the PCF8534As in the system. The timing also generates the LCD frame frequency which it derives as an integer division of the clock frequency (see Table 6). The frame frequency is a fixed division of the internal clock or of the frequency applied to pin CLK when an external clock is used.

7.7 Display register

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

7.8 Segment outputs

The LCD drive section includes 60 segment outputs (S0 to S59) which must be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data resident in the display latch. When less than 60 segment outputs are required the unused segment outputs must be left open-circuit.

7.9 Backplane outputs

The LCD drive section includes four backplane outputs: BP0 to BP3. The backplane output signals are generated in accordance with the selected LCD drive mode.

- In the 1:4 multiplex drive mode BP0 to BP3 must be connected directly to the LCD.

If less than four backplane outputs are required the unused outputs can be left open-circuit.

- In the 1:3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.

- In the 1:2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities.
- In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

7.10 Display RAM

The display RAM is a static 60 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit map indicates the on-state of the corresponding LCD segment; similarly, a logic 0 indicates the off-state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 60 segments operated with respect to backplane BP0 (see Figure 10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

When display data is transmitted to the PCF8534A the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for the acknowledge cycle as with the commands. Depending on the current MUX mode data is stored singularly, in pairs, triplets or quadruplets. e.g. in 1:2 MUX mode the RAM data is stored every second bit. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Figure 11; the RAM filling organization depicted applies equally to other LCD types. With reference to Figure 11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1:2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses.

In the 1:3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1:4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Table 6. LCD frame frequencies

Frame frequency	Nominal frame frequency (Hz)
$\frac{f_{CLK}}{24}$	64

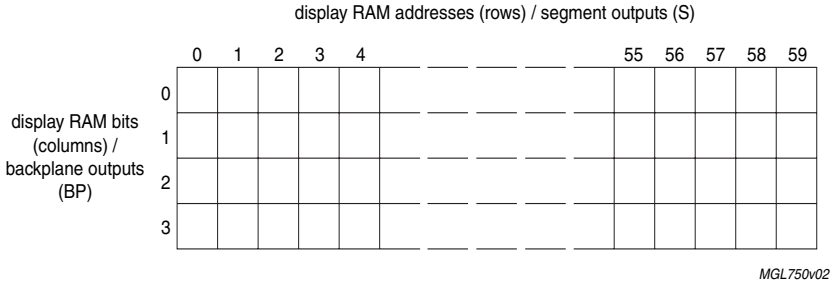


Fig 10. Display RAM bit map showing direct relationship between backplane outputs, display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs

7.11 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Figure 11. The data pointer is automatically incremented in accordance with the chosen LCD configuration. That is, after each byte is stored, the contents of the data pointer are incremented

- by eight (static drive mode),
- by four (1:2 multiplex drive mode),
- by three (1:3 multiplex drive mode) or
- by two (1:4 multiplex drive mode).

If an I^2C-bus data access is terminated early then the state of the data pointer is unknown. The data pointer must be re-written prior to further RAM accesses.

7.12 Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place.
The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8534A occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 27th display data byte transmitted in 1:3 multiplex mode).

The hardware subaddress should not be changed whilst the device is being accessed on the I^2C-bus interface.

7.13 Output bank selector

The output bank selector selects one of the four bits per display RAM address for transfer to the display latch. The actual bit selected depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex, all RAM addresses of bit 0 are selected, these are followed by the contents of bit 1, bit 2 and then bit 3.
- In 1:3 multiplex, bits 0, 1 and 2 are selected sequentially.
- In 1:2 multiplex, bits 0 and 1 are selected and,
- in the static mode, bit 0 is selected.

The $\overline{\text{SYNC}}$ signal will reset these sequences to the following starting points; bit 3 for 1:4 multiplex, bit 2 for 1:3 multiplex, bit 1 for 1:2 multiplex and bit 0 for static mode.

The PCF8534A includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of the contents of bit 0. In the 1:2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

7.14 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1:2 drive mode by using the BANK SELECT command. The input bank selector functions independently to the output bank selector.

7.15 Blinker

The display blinking capabilities of the PCF8534A are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are fractions of the clock frequency. The ratios between the clock and blinking frequencies depend on the mode in which the device is operating, see Table 7.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1:2 LCD drive modes and is implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

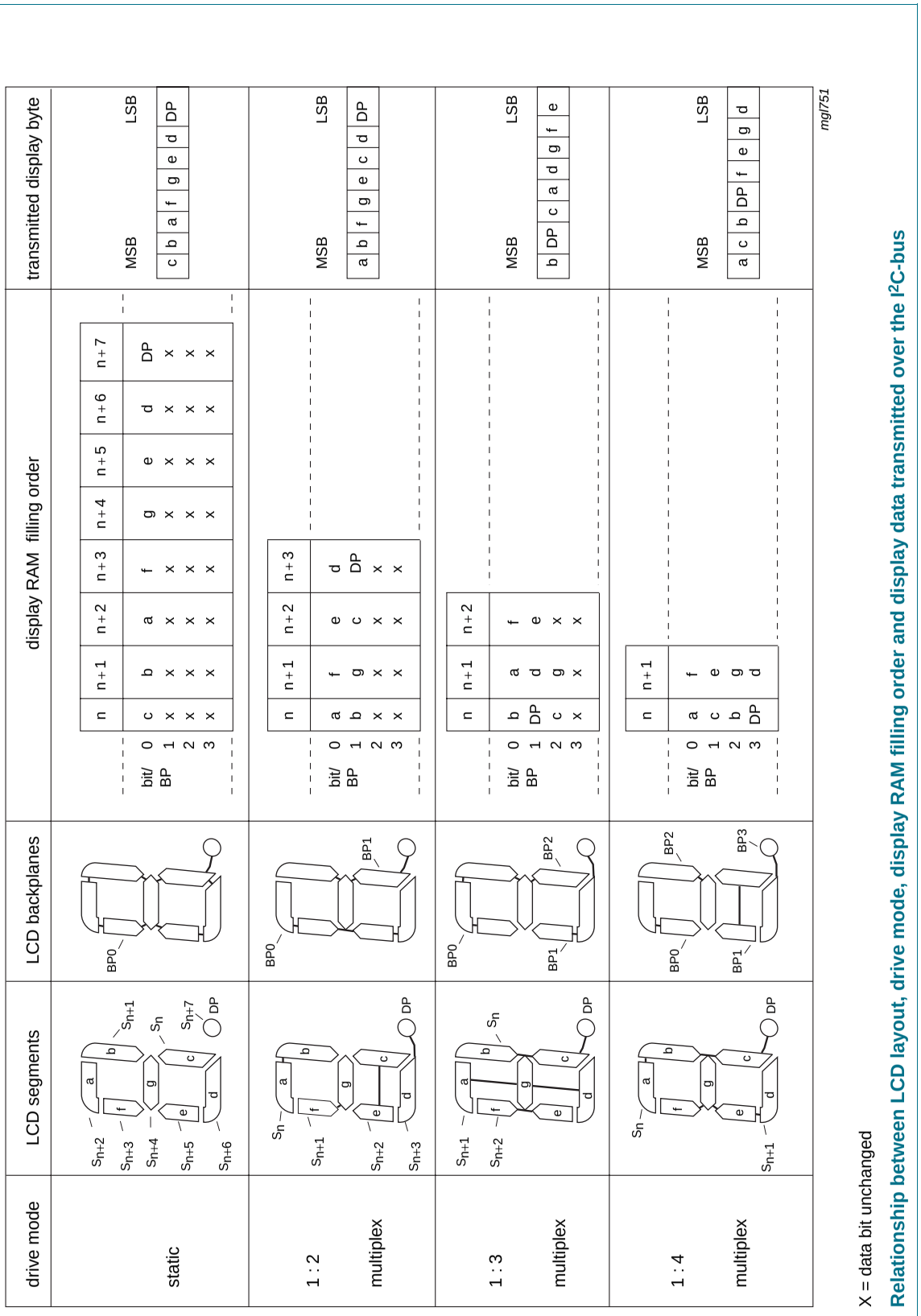
In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 7. Blinking frequencies

Assuming that f_{CLK}= 1536 Hz.

Blinking mode	Normal operating mode ratio	Normal blinking frequency
“Off”	-	Blinking off
“2 Hz”	$\frac{f_{CLK}}{768}$	2 Hz
“1 Hz”	$\frac{f_{CLK}}{1536}$	1 Hz
“0.5 Hz”	$\frac{f_{CLK}}{3072}$	0.5 Hz



X = data bit unchanged

Fig 11. Relationship between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus

8. Basic architecture

8.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer is initiated only when the bus is not busy.

8.1.1 Bit transfer

One data bit is transferred during each clock pulse.
The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Figure 12.

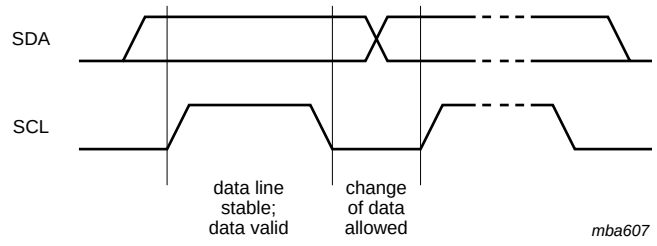


Fig 12. Bit transfer

8.1.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW change of the data line, while the clock is HIGH, is defined as the START condition (S).
A LOW-to-HIGH change of the data line, while the clock is HIGH, is defined as the STOP condition (P). The START and STOP conditions are illustrated in Figure 13.

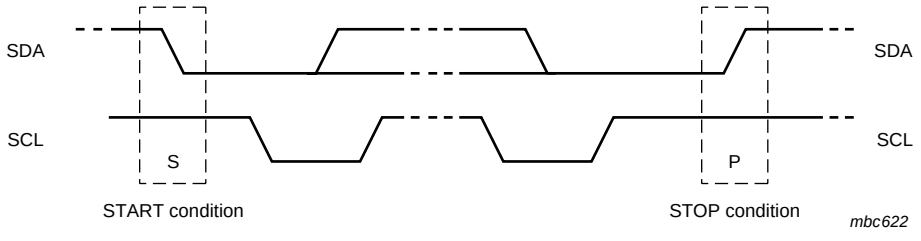


Fig 13. Definition of START and STOP conditions

8.1.2 System configuration

A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’. The system configuration is illustrated in Figure 14.

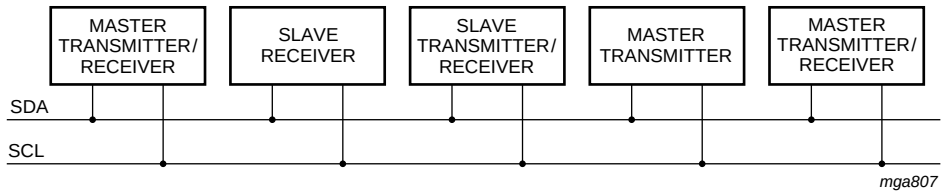


Fig 14. System configuration

8.1.3 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^2C-bus is illustrated in Figure 15.

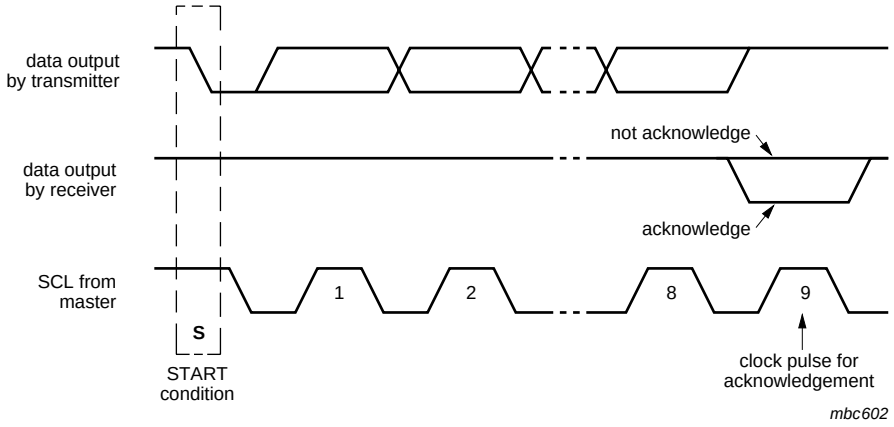


Fig 15. Acknowledgement of the I^2C-bus

8.1.4 PCF8534A I²C-bus controller

The PCF8534A acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8534A are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device application, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} in accordance with a binary coding scheme such that no two devices with a common I²C-bus slave address have the same hardware subaddress.

8.1.5 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

8.1.6 I²C-bus protocol

Two I²C-bus slave addresses (01110000 and 01110010) are reserved for the PCF8534A. The least significant bit of the slave address that a PCF8534A will respond to is defined by the level tied at its input SA0. The PCF8534A is a write only device and will not respond to a read access. Two types of PCF8534A can be distinguished on the same I²C-bus which allows:

- Up to 16 PCF8534As on the same I²C-bus for very large LCD applications
- The use of two types of LCD multiplex on the same I²C-bus.

The I²C-bus protocol is shown in Figure 16. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the two PCF8534A slave addresses available. All PCF8534As with the corresponding SA0 level acknowledge in parallel to the slave address, but all PCF8534As with the alternative SA0 level ignore the whole I²C-bus transfer.

After acknowledgement, a control byte follows which defines if the next byte is RAM or command information. The control byte also defines if the next following byte is a control byte or further RAM/command data.

In this way it is possible to configure the device then fill the display RAM with little overhead.

The command bytes and control bytes are also acknowledged by all addressed PCF8534As connected to the bus.

The display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended PCF8534A device.

The acknowledgement after each byte is made only by the (A0, A1 and A2) addressed PCF8534A. After the last display byte, the I²C-bus master issues a STOP condition (P). Alternatively a START may be issued to RESTART an I²C-bus access.

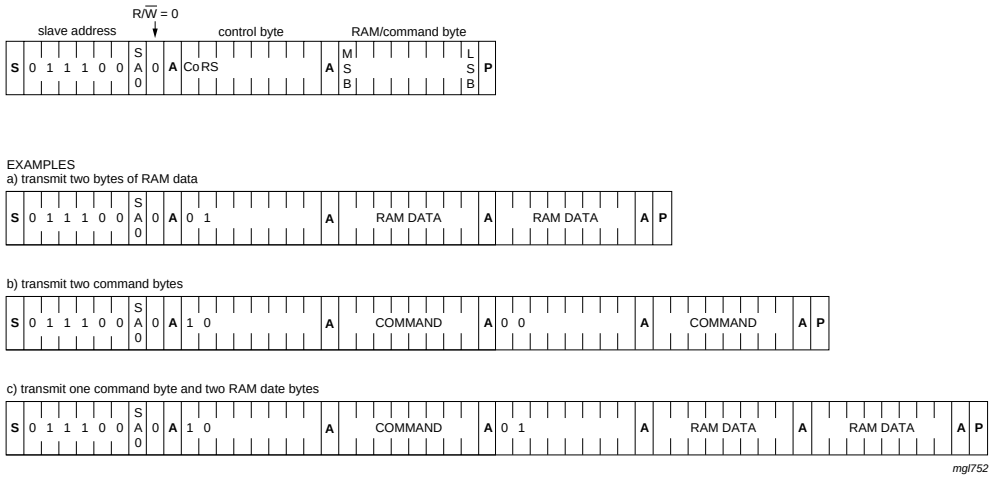
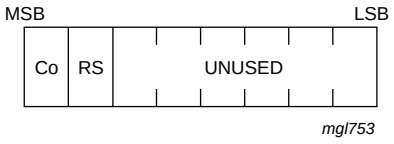


Fig 16. I²C-bus protocol



(1) C_o = 0; last control byte

(2) C_o = 1; control bytes continue

(3) RS = 0; data is a command byte

(4) RS = 1; data is a display byte

Fig 17. Control byte format

8.2 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. The five commands available to the PCF8534A are defined in Table 8.

Table 8. Definition of PCF8534A commands

Command	OPCODE	Options	Description
Mode set	1 1 0 0 E B M1 M0	Table 9	defines LCD drive mode
		Table 10	defines LCD bias configuration
		Table 11	defines display status; the possibility to disable the display allows implementation of blinking under external control
Load data pointer	0 P6 P5 P4 P3 P2 P1 P0	Table 12	7 bits of immediate data, bits P6 to P0, are transferred to the data pointer to define one of 8 hardware subaddresses
Device select	1 1 1 0 0 A2 A1 A0	Table 13	3 bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of 8 hardware subaddresses

Table 8. Definition of PCF8534A commands

Command	OPCODE	Options	Description
Bank select	1 1 1 1 1 0 I 0	Table 14	defines input bank selection (storage of arriving display data)
		Table 15	defines output bank selection (retrieval of LCD display data); the BANK SELECT command has no effect in 1:3 or 1:4 multiplex drive modes
Blink	1 1 1 1 0 A BF BF	Table 16	defines the blinking frequency
	1 0	Table 17	selects the blinking mode; normal operation with frequency set by BF1, BF0 or blinking by alteration of display RAM banks. Alteration blinking does not apply in 1:3 or 1:4 multiplex drive modes.

Table 9. Mode set option 1

LCD drive mode		Bits	
Drive mode	**Backplane**	**M1**	**M0**
static	1	0	1
1:2 MUX	2	1	0
1:3 MUX	3	1	1
1:4 MUX	4	0	0

Table 10. Mode set option 2

LCD bias	Bit B
$\frac{1}{3}$ bias	0
$\frac{1}{2}$ bias	1

Table 11. Mode set option 3

Display status	Bit E
disabled (blank)	0
enabled	1

Table 12. Load data pointer option

Description	Bits						
7 bit ordinary value of 0 to 59	P6	P5	P4	P3	P2	P1	P0

Table 13. Device select option

Description	Bits		
3 bit binary value of 0 to 7	A2	A1	A0

Table 14. Blank select option 1 (input)

Static	1:2 MUX	Bit I
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 15. Blank select option 2 (output)

Static	1:2 MUX	Bit 0
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 16. Blink option 1

Blink frequency	Bits	
	BF1	BF0
off	0	0
2 Hz	0	1
1 Hz	1	0
0.5 Hz	1	1

Table 17. Blink option 2

Blink mode	Bit A	
normal blinking	0	[1]
alteration blinking	1	

[1] Normal blinking is assumed when the multiplex rates 1:3 or 1:4 are selected.

8.3 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8534A and co-ordinates their effects.
The controller is also responsible for loading display data into the display RAM as required by the filling order.

9. Limiting values

Table 18. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	6.5	V
V_{LCD}	LCD supply voltage		V_{SS} – 0.5	7.5	V
V_I	input voltage on pins SDA, SCL, CLK, $\overline{SYNC}$, SA0, OSC and A0 to A2		–0.5	6.5	V
V_O	output voltage on pins SDA, SCL, CLK, $\overline{SYNC}$, SA0, OSC and A0 to A2		–0.5	7.5	V
I_{DD}	supply current		–50	+50	mA
I_{LCD}	LCD supply current		–50	+50	mA
I_{SS}	ground supply current		–50	+50	mA
I_I	input current		–10	+10	mA
I_O	output current		–10	+10	mA
P_{TOT}	total power dissipation		-	400	mW
P_{OUT}	power dissipation per output		-	100	mW
T_{STG}	storage temperature		–65	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM		±2000	V
		MM		±200	V
		CDM		±2000	V
I_{LU}	latch-up current			100	mA

10. Static characteristics

Table 19. Static characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{AMB} = –40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			1.8	-	5.5	V
V_{LCD}	LCD supply voltage			2.5	-	6.5	V
I_{DD}	supply current	f_{CLK} = 1536 Hz	[1]	-	8	20	µA
I_{LCD}	LCD supply current	f_{CLK} = 1536 Hz	[1]	-	24	60	µA
Logic							
V_I	Input voltage			V_{SS} – 0.5		V_{DD} + 0.5	V
V_{IL}	LOW-level input voltage on pins CLK, $\overline{SYNC}$, OSC, A0 to A2 and SA0			V_{SS}	-	0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage on pins CLK, $\overline{SYNC}$, OSC, A0 to A2 and SA0			0.7 V_{DD}	-	V_{DD}	V
V_{POR}	power-on reset voltage			1.0	1.3	1.6	V

Table 19. Static characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{AMB} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{OL1}	LOW-level output current on pins CLK and $\overline{SYNC}$	V_{OL} = 0.4 V; V_{DD} = 5 V		1	-	-	mA
I_{OH1}	HIGH-level output current on pin CLK	V_{OH} = 4.6 V; V_{DD} = 5 V		−1	-	-	mA
I_{L1}	leakage current on pins SA0, A0 to A2, CLK	$V_I = V_{DD}$ or V_{SS}		−1	-	+1	µA
I_{L2}	leakage current on pin OSC	$V_I = V_{DD}$		−1	-	+1	µA
C_I	input capacitance		[2]	-	-	7	pF
I^2C-bus; pins SDA and SCL							
V_I	Input voltage			V_{SS} −0.5	-	5.5	V
$V_{IL(SCL)}$	LOW-level input voltage			V_{SS}	-	0.3 V_{DD}	V
$V_{IL(SDA)}$	LOW-level input voltage			V_{SS}	-	0.2 V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7 V_{DD}	-	5.5	V
I_{OL2}	LOW-level output current on pin SDA	V_{OL} = 0.4 V; V_{DD} = 5 V		3	-	-	mA
I_{L3}	leakage current	$V_I = V_{DD}$ or V_{SS}		−1	-	+1	µA
C_I	input capacitance		[2]	-	-	7	pF
LCD outputs							
V_{BP}	DC voltage component on pins BP0 to BP3	C_{BP} = 35 nF	[4]	−100	-	+100	mV
V_S	DC voltage component on pins S0 to S59	C_S = 5 nF	[5]	−100	-	+100	mV
R_{BP}	output resistance at pins BP0 to BP3	V_{LCD} = 5 V	[3]	-	1.5	10	kΩ
R_S	output resistance at pins S0 to S59	V_{LCD} = 5 V	[3]	-	6.0	13.5	kΩ

[1] LCD outputs are open circuit; inputs at V_{SS} or V_{DD}; external clock with 50 % duty factor; I^2C-bus inactive.

[2] Not tested, design spec only.

[3] Outputs measured individually and sequentially.

[4] C_{BP} = backplane capacitance.

[5] C_S = segment capacitance.

11. Dynamic characteristics

Table 20. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{AMB} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{CLK(int)}$	oscillator frequency on pin CLK (internal clock)	V_{DD} = 5 V	[1]	960	1536	3046	Hz
$f_{CLK(ext)}$	oscillator frequency on pin CLK (external clock)	V_{DD} = 5 V		797	1536	3046	Hz
t_{CLKH}	input CLK HIGH time			130	-	-	µs
t_{CLKL}	input CLK LOW time			130	-	-	µs
t_r	CLK rise time			-	-	-	ns
t_f	CLK fall time			-	-	-	ns

Table 20. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{AMB} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(p)SYNC}$	$\overline{SYNC}$ propagation delay time		-	30	-	ns
t_{SYNCL}	$\overline{SYNC}$ LOW time		1	-	-	µs
$t_{d(PLCD)}$	driver propagation delay	V_{LCD} = 5 V	-	-	30	µs
Timing characteristic: I²C-bus		[2]				
f_{SCL}	SCL clock frequency		-	-	400	kHz
t_{BUF}	bus free time between a STOP and START		1.3	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	-	-	µs
t_{LOW}	LOW period of the SCL clock		1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock		0.6	-	-	µs
t_r	SCL and SDA rise time		-	-	0.3	µs
t_f	SCL and SDA fall time		-		0.3	µs
C_b	capacitive bus line load		-	-	400	pF
$t_{SU;DAT}$	data set-up time		100			ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	-	µs
t_{SW}	tolerable spike pulse width on bus		-	-	50	ns

[1] Typical output duty cycle of 50 %.

[2] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

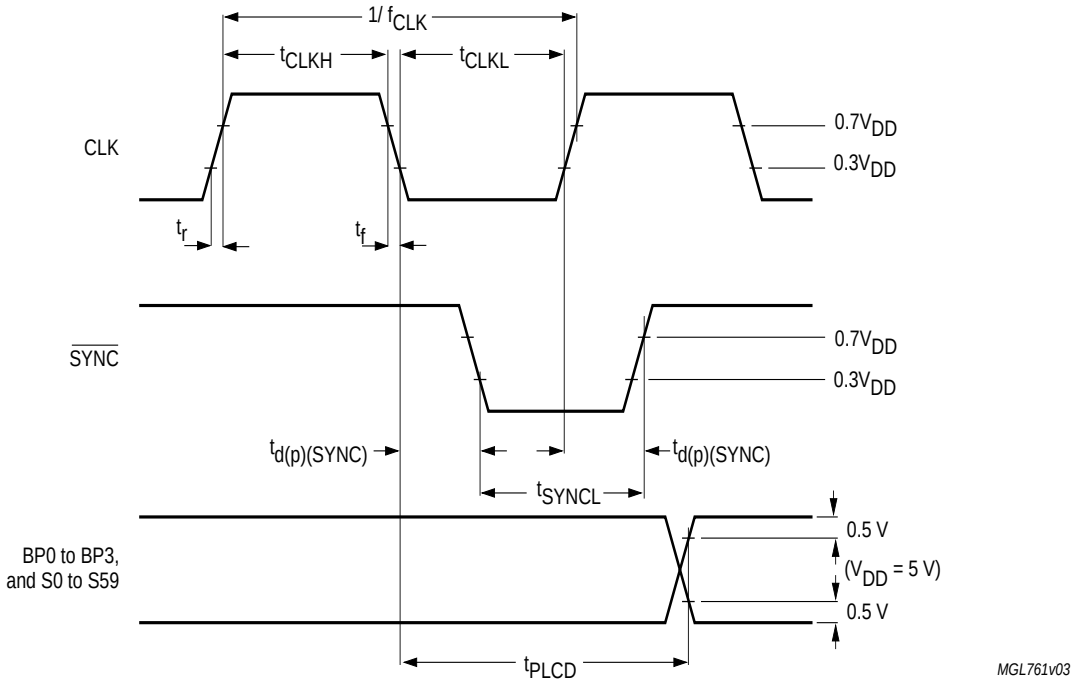


Fig 18. Driver timing waveforms

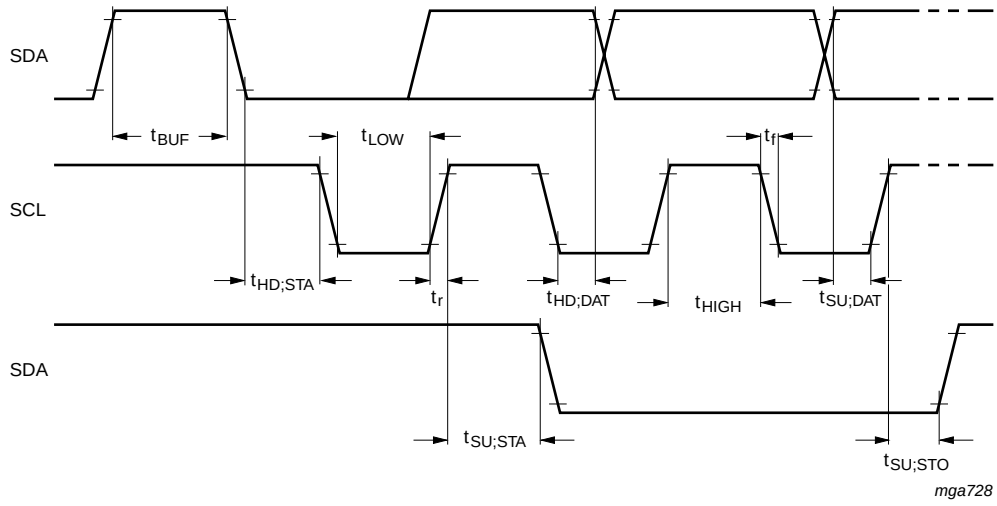


Fig 19. I²C-bus timing waveforms

12. Application information

12.1 Cascaded operation

In large display configurations, up to 16 PCF8534As can be distinguished on the same I²C-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable I²C-bus slave address (SA0). When cascaded PCF8534As are synchronized they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8534As of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (see Figure 20).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8534As. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments, or by the definition of a multiplex mode when PCF8534As with different SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input / output pin; the output selection being realized as an open-drain driver with an internal pull-up resistor. A PCF8534A asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. If synchronization in the cascade is lost, it is restored by the first PCF8534A to assert $\overline{\text{SYNC}}$. The timing relationship between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8534A are shown in Figure 21.

The contact resistance between the $\overline{\text{SYNC}}$ pins of cascaded devices must be controlled. If the resistance is too high then the device will not be able to synchronize properly. Table 21 shows the limiting values for contact resistance.

Table 21. $\overline{\text{SYNC}}$ contact resistance

Number of devices	Maximum contact resistance
2	6000 Ω
3 to 5	2200 Ω
6 to 10	1200 Ω
11 to 16	700 Ω

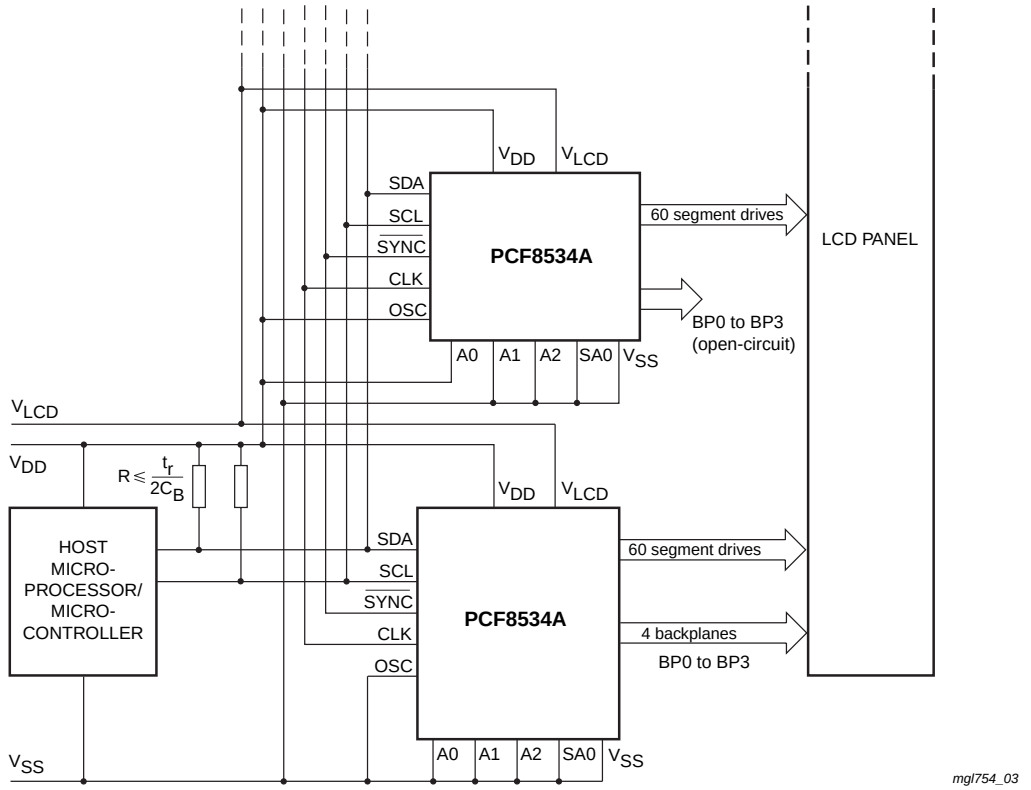


Fig 20. Cascaded PCF8534A configuration

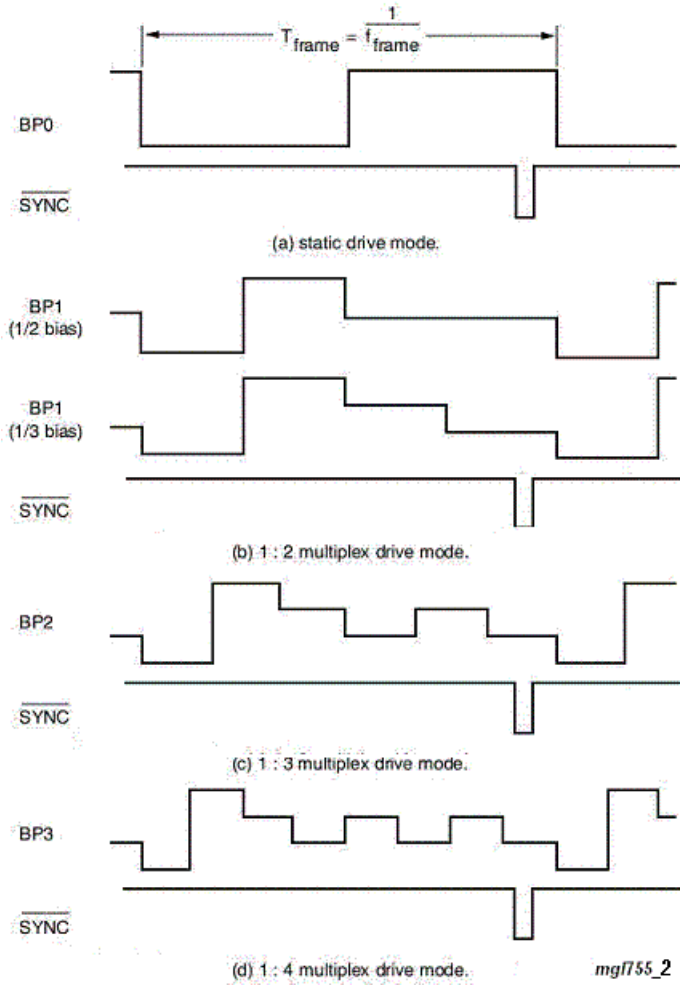


Fig 21. Synchronization of the cascade for various PCF8534A drive modes

13. Test information

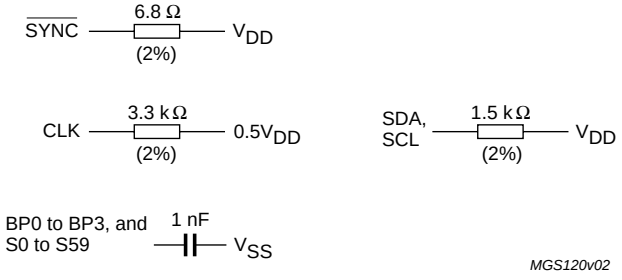
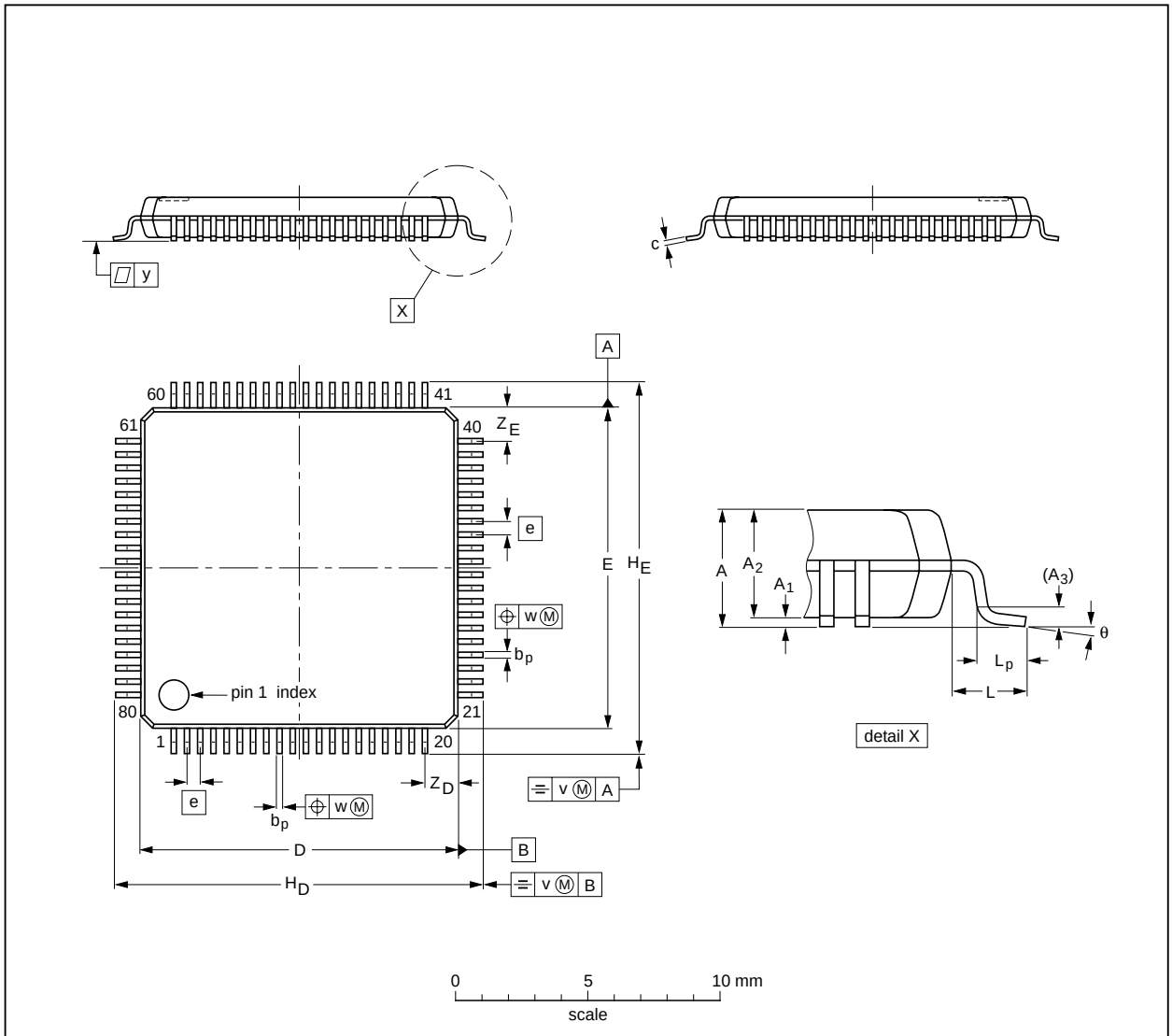


Fig 22. Test loads

14. Package outline

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.27 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1	0.75 0.30	0.2	0.15	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT315-1	136E15	MS-026				~~00-01-19~~ 03-02-25

Fig 23. Package outline LQFP80

15. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling MOS devices; see *JESD625-A and/or IEC61340-5*.

16. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 24) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 22 and 23

Table 22. SnPb eutectic process (from J-STD-020C)

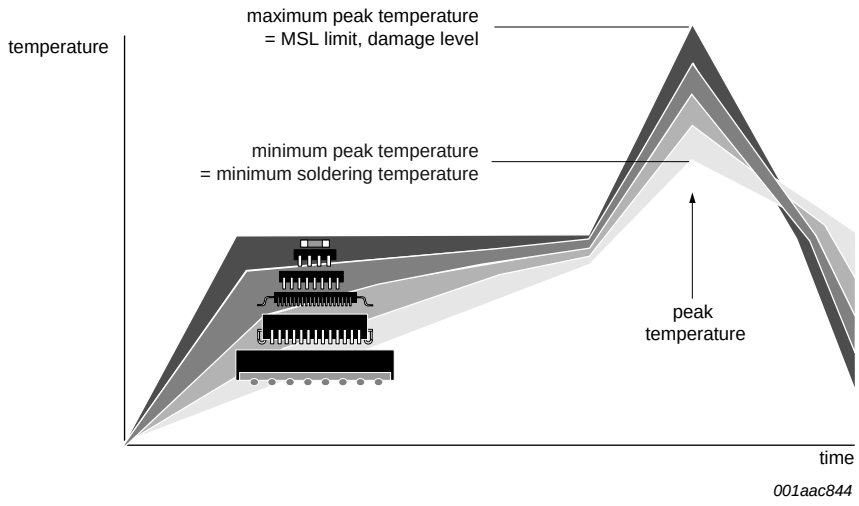
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 23. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 24.



MSL: Moisture Sensitivity Level

Fig 24. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Revision history

Table 24. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8534A_00.90	20080204	Product data sheet	-	-

18. Legal information

19. Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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