IRF840
POWER MOSFET

GENERAL DESCRIPTION

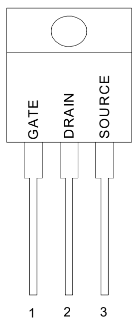
This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. In addition, this advanced MOSFET is designed to withstand high energy in avalanche and commutation modes. The new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional and safety margin against unexpected voltage transients.

FEATURES

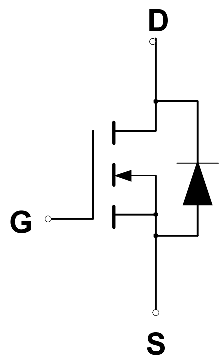
- Robust High Voltage Termination
- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and V_{DS}(on) Specified at Elevated Temperature

PIN CONFIGURATION

TO-220/TO-220FP
Top View



SYMBOL



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain to Current — Continuous	I_D	8.0	A
— Pulsed	I_{DM}	32	
Gate-to-Source Voltage — Continue	V_{GS}	±20	V
— Non-repetitive	V_{GSM}	±40	V
Total Power Dissipation	P_D		W
TO-220		125	
TO-220FP		40	
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	℃
Single Pulse Drain-to-Source Avalanche Energy — T_J = 25℃ (V_{DD} = 100V, V_{GS} = 10V, I_L = 8A, L = 10mH, R_G = 25Ω)	E_{AS}	320	mJ
Thermal Resistance — Junction to Case	θ_{JC}	1.0	℃/W
— Junction to Ambient	θ_{JA}	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	℃

ORDERING INFORMATION

Part Number	Package
IRF840	TO-220
IRF840FP	TO-220 Full Package

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_J = 25℃.

Characteristic		Symbol	IRF840 Min	Typ	Max	Units
Drain-Source Breakdown Voltage (V_{GS} = 0 V, I_D = 250 μA)		$V_{(BR)DSS}$	500			V
Drain-Source Leakage Current (V_{DS} = 500 V, V_{GS} = 0 V) (V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125℃)		I_{DSS}			0.25 1.0	mA
Gate-Source Leakage Current-Forward (V_{gsf} = 20 V, V_{DS} = 0 V)		I_{GSSF}			100	nA
Gate-Source Leakage Current-Reverse (V_{gsr} = 20 V, V_{DS} = 0 V)		I_{GSSR}			100	nA
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	2.0		4.0	V
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 4.0A) *		$R_{DS(on)}$			0.8	Ω
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 8.0 A)		$V_{DS(on)}$		5.0	7.2	V
Forward Transconductance (V_{DS} = 50 V, I_D = 4.0A) *		g_{FS}	4.9			mmhos
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}		1450	1680	pF
Output Capacitance		C_{oss}		190	246	pF
Reverse Transfer Capacitance		C_{rss}		45.4	144	pF
Turn-On Delay Time	(R_{Go} + C17n = 9.1Ω) *	$t_{d(on)}$		15	50	ns
Rise Time		t_r		33	72	ns
Turn-Off Delay Time		$t_{d(off)}$		40	150	ns
Fall Time		t_f		32	60	ns
Total Gate Charge	(V_{DS} = 400 V, I_D = 8.0 A, V_{GS} = 10 V)*	Q_g		40	64	nC
Gate-Source Charge		Q_{gs}		8.0		nC
Gate-Drain Charge		Q_{gd}		17		nC
Internal Drain Inductance (Measured from the drain lead 0.25" from package to center of die)		L_D		4.5		nH
Internal Drain Inductance (Measured from the source lead 0.25" from package to source bond pad)		L_S		7.5		nH
SOURCE-DRAIN DIODE CHARACTERISTICS						
Forward On-Voltage(1)	(I_S = 8.0 A, V_{GS} = 0 V, d_{IS}/d_t = 100A/μs)	V_{SD}			1.5	V
Forward Turn-On Time		t_{on}		**		ns
Reverse Recovery Time		t_{rr}		320		ns

* Pulse Test: Pulse Width ≦300μs, Duty Cycle ≦2%

** Negligible, Dominated by circuit inductance

TYPICAL ELECTRICAL CHARACTERISTICS

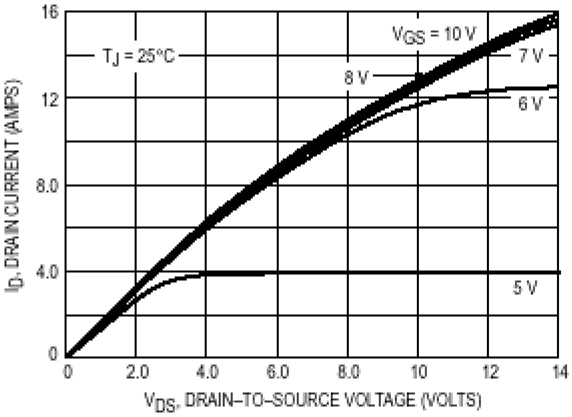


Figure 1. On–Region Characteristics

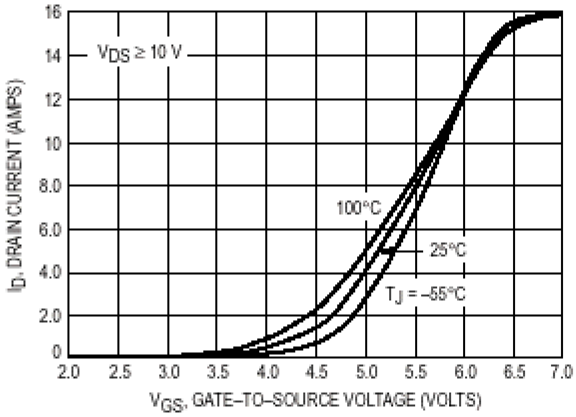


Figure 2. Transfer Characteristics

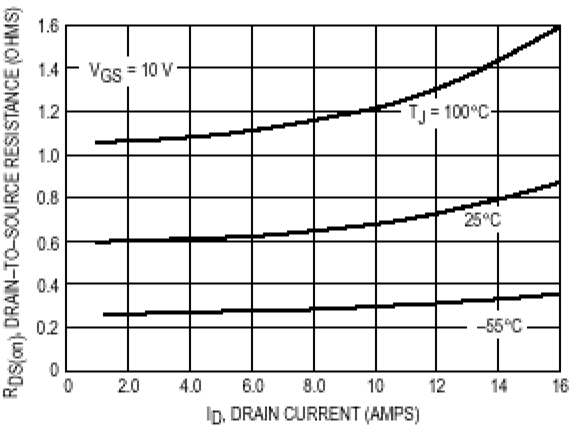


Figure 3. On–Resistance versus Drain Current and Temperature

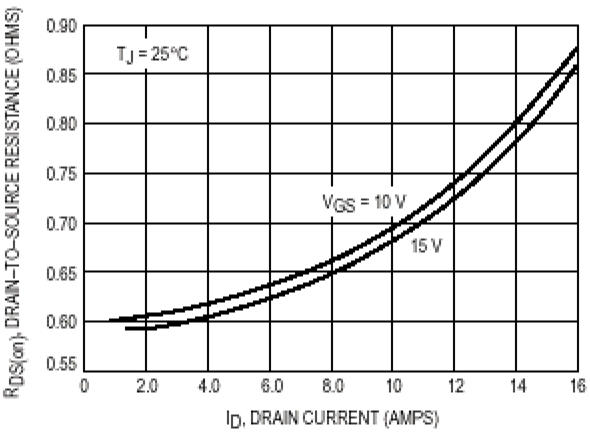


Figure 4. On–Resistance versus Drain Current and Gate Voltage

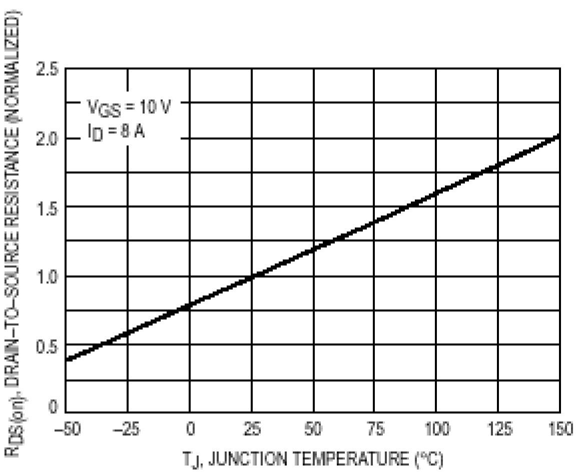


Figure 5. On–Resistance Variation with Temperature

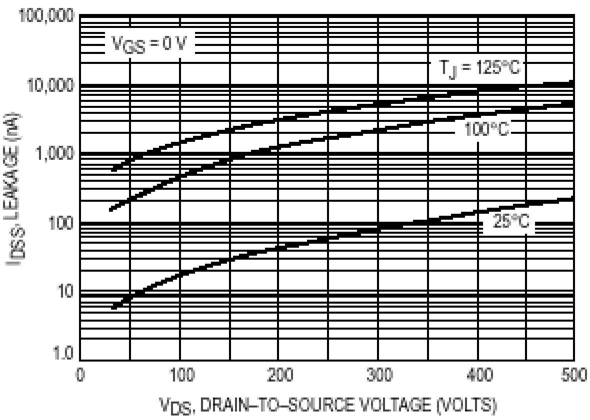


Figure 6. Drain–to–Source Leakage Current versus Voltage

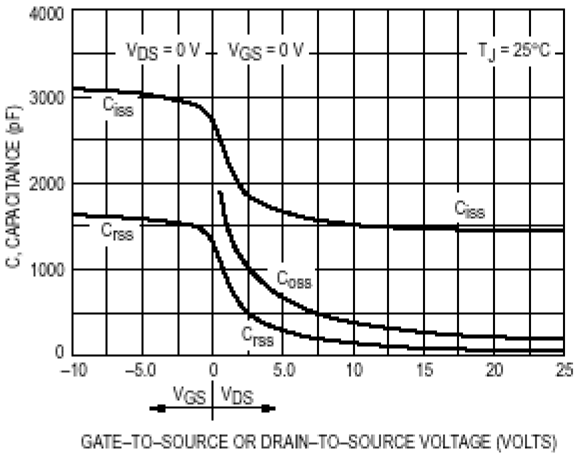


Figure 7. Capacitance Variation

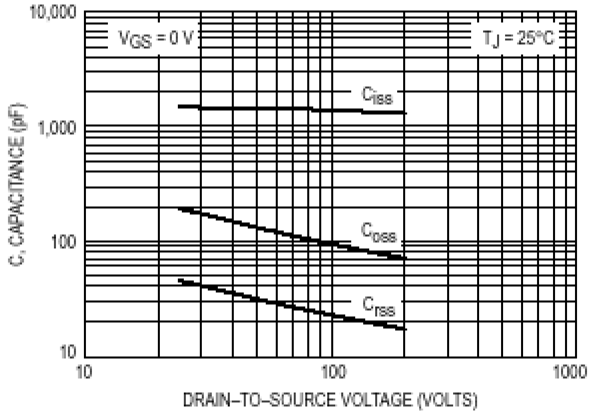


Figure 8. High Voltage Capacitance Variation

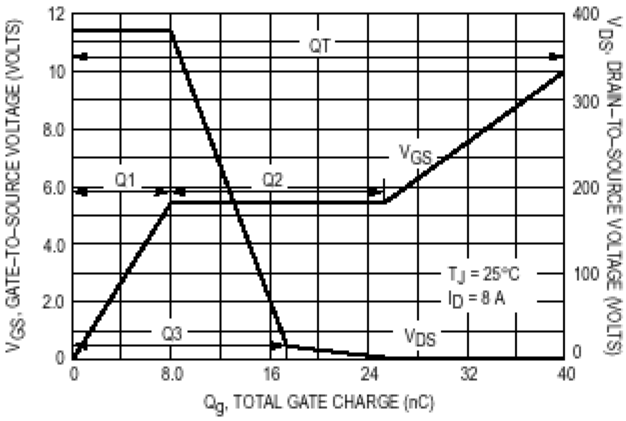


Figure 9. Gate–to–Source and Drain–to–Source Voltage versus Total Charge

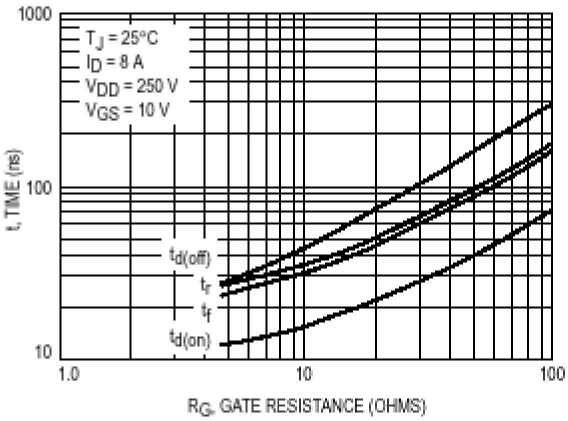


Figure 10. Resistive Switching Time Variation versus Gate Resistance

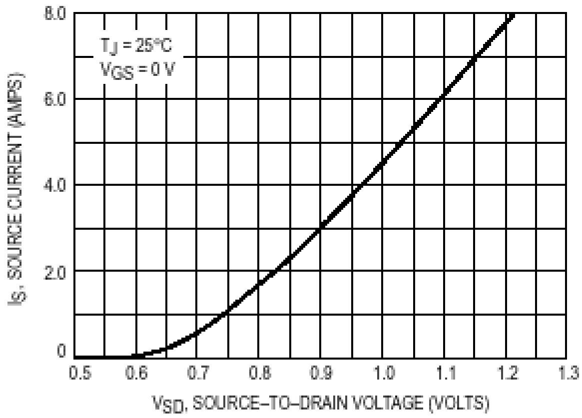


Figure 11. Diode Forward Voltage versus Current

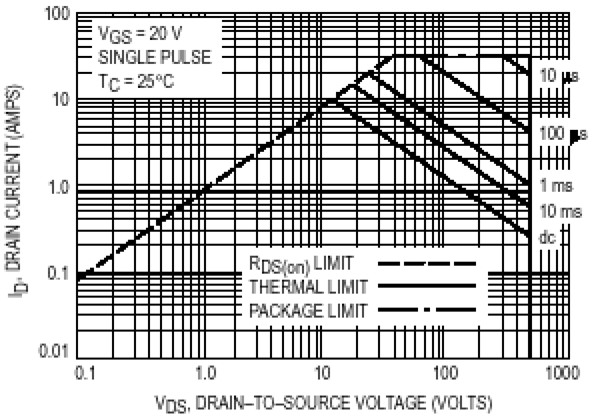


Figure 12. Maximum Rated Forward Biased Safe Operating Area

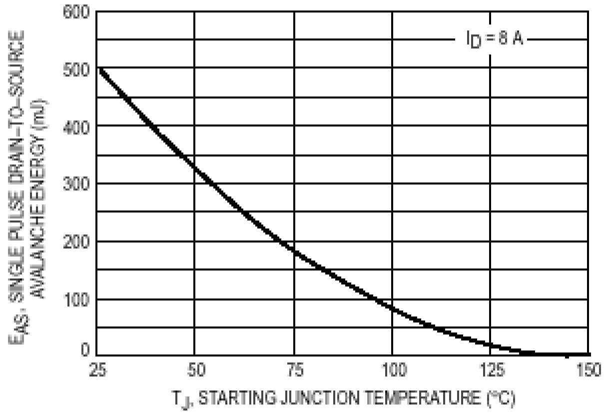


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

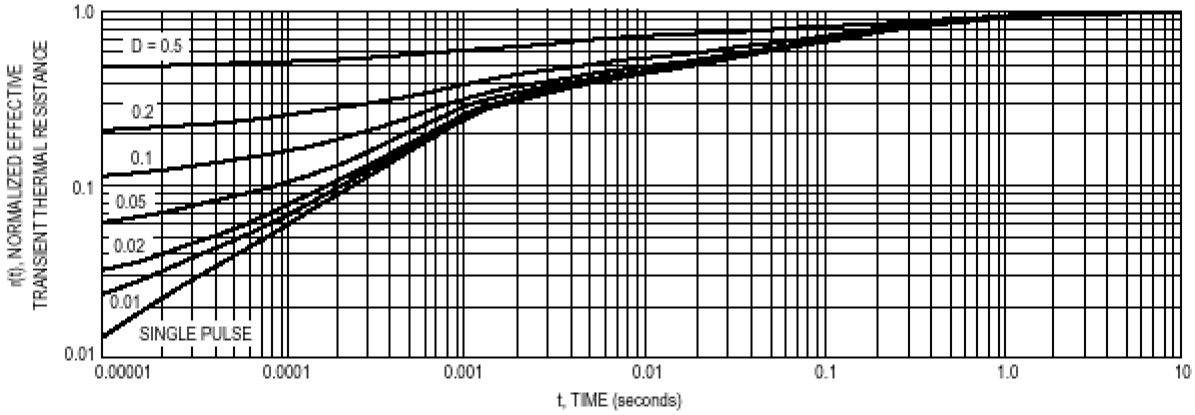


Figure 14. Thermal Response