# HD74LS95B

## 4-bit Parallel Access Shift Register

REJ03D0424-0400
Rev.4.00
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The 4-bit register features parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The register has three mode operation:

- Parallel (broadside) load
- Shift right (the direction $Q_A$ toward $Q_D$)
- Shift left (the direction $Q_D$ toward $Q_A$)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited. Shift right is accomplished on the high-to-low transition of clock-1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock-2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop ($Q_D$ to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock-1 and clock-2 if both modes can be clocked from the same source. Changes at the mode control inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

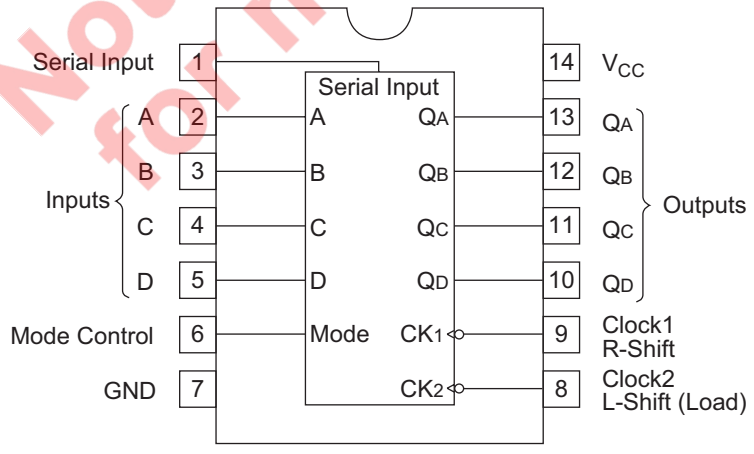


### Features

- Ordering Information

| Part Name | Package Type | Package Code (Previous Code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|---|---|---|---|---|
| HD74LS95BFPEL | SOP-14 pin (JEITA) | PRSP0014DF-B (FP-14DAV) | FP | EL (2,000 pcs/reel) |

### Pin Arrangement




(Top view)

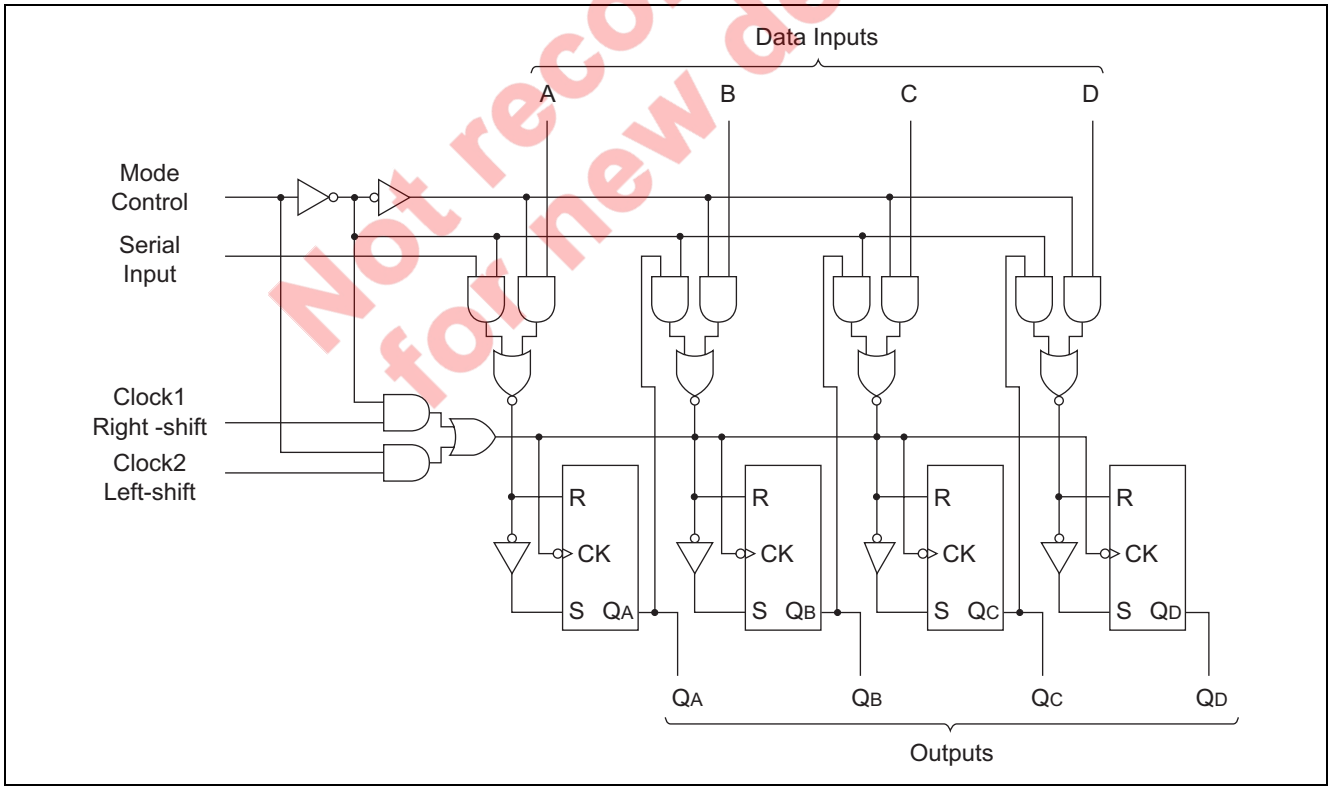
## Function Table

| Inputs | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Mode control | Clocks | | Serial | Parallel | | | | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| | 2(L) | 1(R) | | A | B | C | D | | | | |
| H | H | X | X | X | X | X | X | $Q_{AO}$ | $Q_{BO}$ | $Q_{CO}$ | $Q_{DO}$ |
| H | ↓ | X | X | a | b | c | d | a | b | c | d |
| H | ↓ | X | X | $Q_B$* | $Q_C$* | $Q_D$* | d | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | d |
| L | L | H | X | X | X | X | X | $Q_{AO}$ | $Q_{BO}$ | $Q_{CO}$ | $Q_{DO}$ |
| L | X | ↓ | H | X | X | X | X | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| L | X | ↓ | L | X | X | X | X | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| ↑ | L | L | X | X | X | X | X | $Q_{AO}$ | $Q_{BO}$ | $Q_{CO}$ | $Q_{DO}$ |
| ↓ | L | L | X | X | X | X | X | $Q_{AO}$ | $Q_{BO}$ | $Q_{CO}$ | $Q_{DO}$ |
| ↓ | L | H | X | X | X | X | X | $Q_{AO}$ | $Q_{BO}$ | $Q_{CO}$ | $Q_{DO}$ |
| ↑ | H | L | X | X | X | X | X | $Q_{AO}$ | $Q_{BO}$ | $Q_{CO}$ | $Q_{DO}$ |
| ↑ | H | H | X | X | X | X | X | $Q_{AO}$ | $Q_{BO}$ | $Q_{CO}$ | $Q_{DO}$ |

Notes: 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. ↓; transition from high to low level
4. a to d; the level of steady-state input at inputs A, B, C, or D, respectively.
5. $Q_{AO}$ to $Q_{DO}$; the level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the indicated steady-state input conditions were established.
6. $Q_{An}$ to $Q_{Dn}$; the level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the most-recent (↑) transition of the clock.
7. *; Shifting left require external connection of $Q_B$ to A, $Q_C$ to B, and $Q_D$ to C. Serial data is entered at input D.



## Block Diagram



## Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7 | V |
| Input voltage | $V_{IN}$ | 7 | V |
| Power dissipation | $P_T$ | 400 | mW |
| Storage temperature | Tstg | –65 to +150 | °C |

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

## Recommended Operating Conditions

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output current | $I_{OH}$ | — | — | –400 | µA |
| | $I_{OL}$ | — | — | 8 | mA |
| Operating temperature | Topr | –20 | 25 | 75 | °C |
| Clock frequency | $f_{clock}$ | 0 | — | 25 | MHz |
| Clock pulse width | $t_{w\,(CK)}$ | 20 | — | — | ns |
| Setup time | $t_{su}$ | 20 | — | — | ns |
| Hold time | $t_h$ | 10 | — | — | ns |
| Enable time 1 | $t_{enable\ 1}$ | 20 | — | — | ns |
| Enable time 2 | $t_{enable\ 2}$ | 20 | — | — | ns |
| Inhibit time 1 | $t_{inhibit\ 1}$ | 20 | — | — | ns |
| Inhibit time 2 | $t_{inhibit\ 2}$ | 20 | — | — | ns |



## Electrical Characteristics

(Ta = –20 to +75 °C)

| Item | Symbol | min. | typ.* | max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | 2.0 | — | — | V | |
| | $V_{IL}$ | — | — | 0.8 | V | |
| Output voltage | $V_{OH}$ | 2.7 | — | — | V | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = –400 µA |
| | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 4 mA; $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V |
| | | — | — | 0.5 | | $I_{OL}$ = 8 mA |
| Input current | $I_{IH}$ | — | — | 20 | µA | $V_{CC}$ = 5.25 V, $V_I$ = 2.7 V |
| | $I_{IL}$ | — | — | –0.4 | mA | $V_{CC}$ = 5.25 V, $V_I$ = 0.4 V |
| | $I_I$ | — | — | 0.1 | mA | $V_{CC}$ = 5.25 V, $V_I$ = 7 V |
| Short-circuit output current | $I_{OS}$ | –20 | — | –100 | mA | $V_{CC}$ = 5.25 V |
| Supply current** | $I_{CC}$ | — | 13 | 21 | mA | $V_{CC}$ = 5.25 V |
| Input clamp voltage | $V_{IK}$ | — | — | –1.5 | V | $V_{CC}$ = 4.75 V, $I_{IN}$ = –18 mA |

Notes: * $V_{CC}$ = 5 V, Ta = 25°C

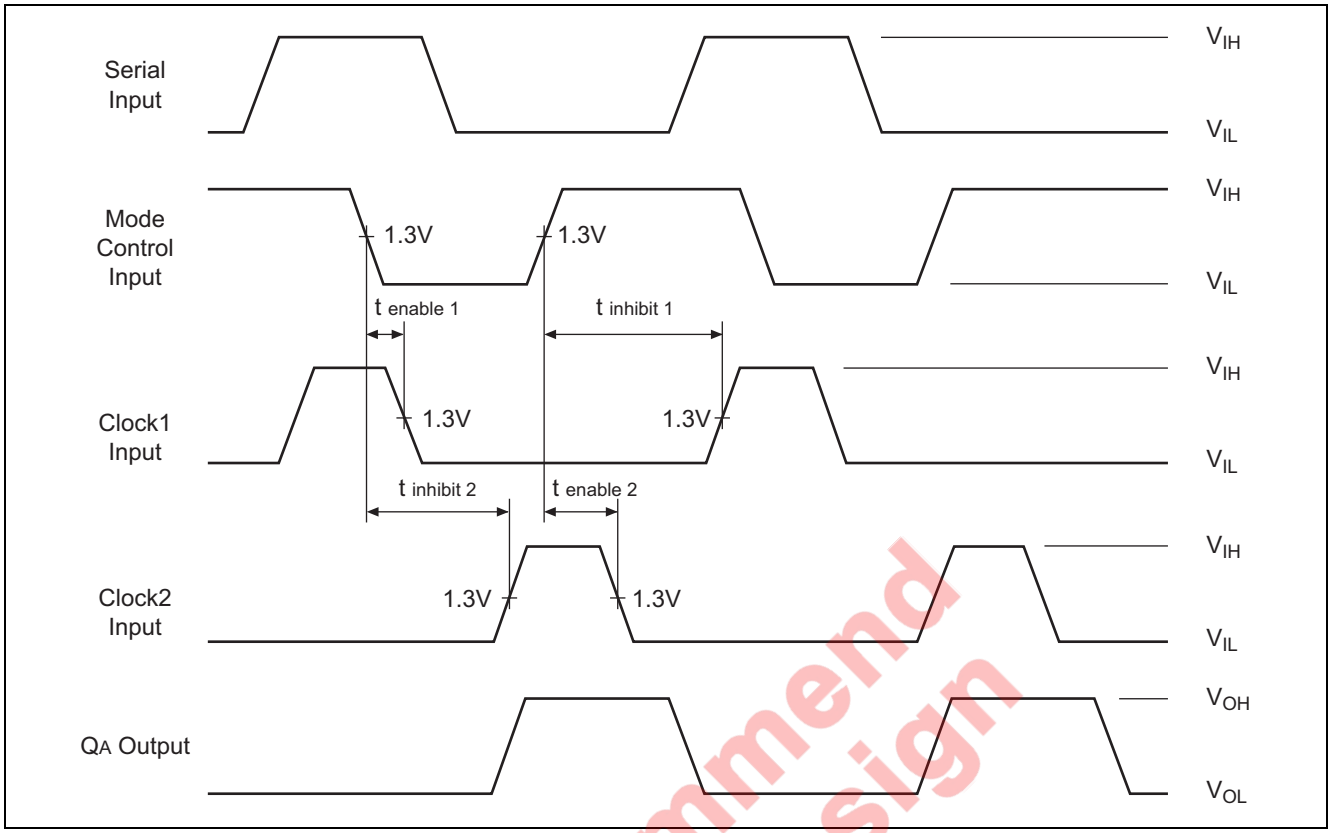
** $I_{CC}$ is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and momentary 3 V, then ground, applied both clock inputs.

## Switching Characteristics

($V_{CC}$ = 5 V, Ta = 25°C)

| Item | Symbol | min. | typ. | max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | 25 | 36 | — | MHz | $C_L$ = 15 pF, $R_L$ = 2 kΩ |
| Propagation delay time | $t_{PLH}$ | — | 18 | 27 | ns | |
| | $t_{PHL}$ | — | 21 | 32 | ns | |

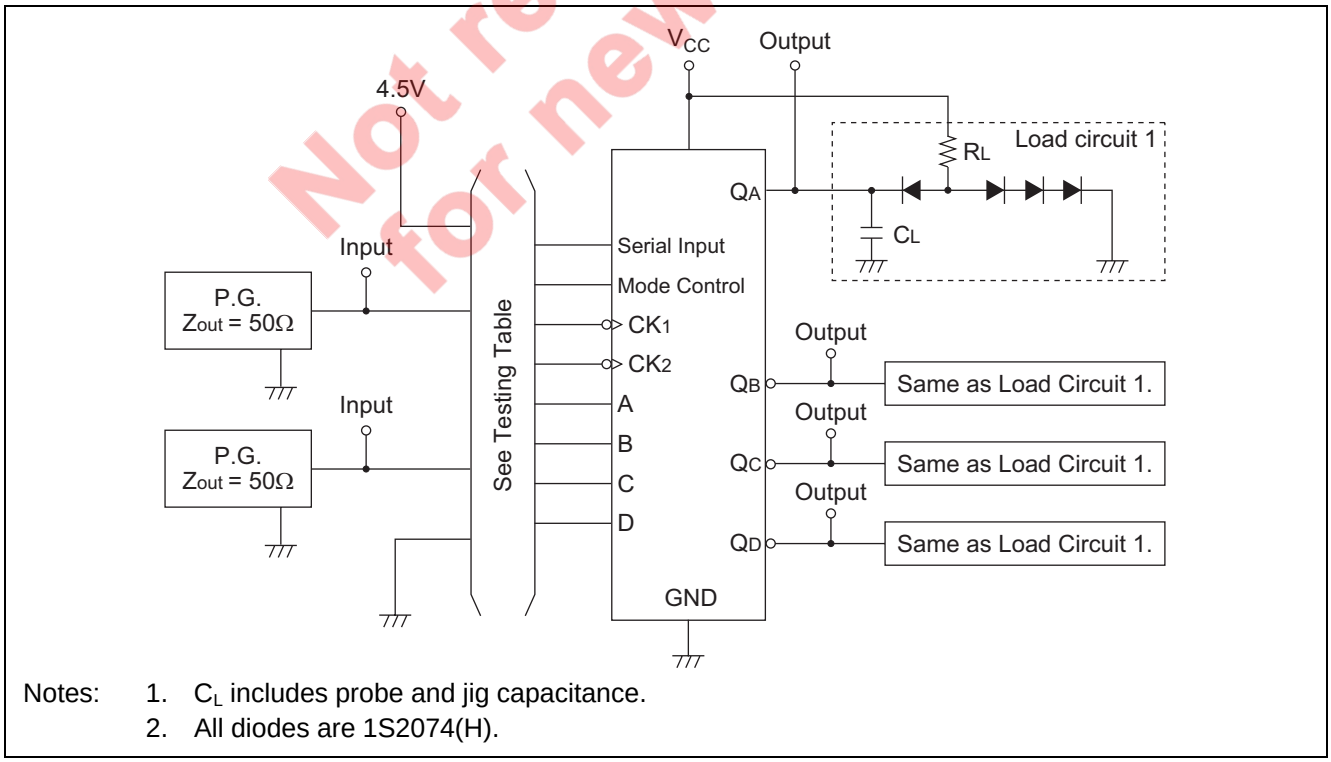
## Clock Enable / Inhibit Times






## Testing Method

### Test Circuit

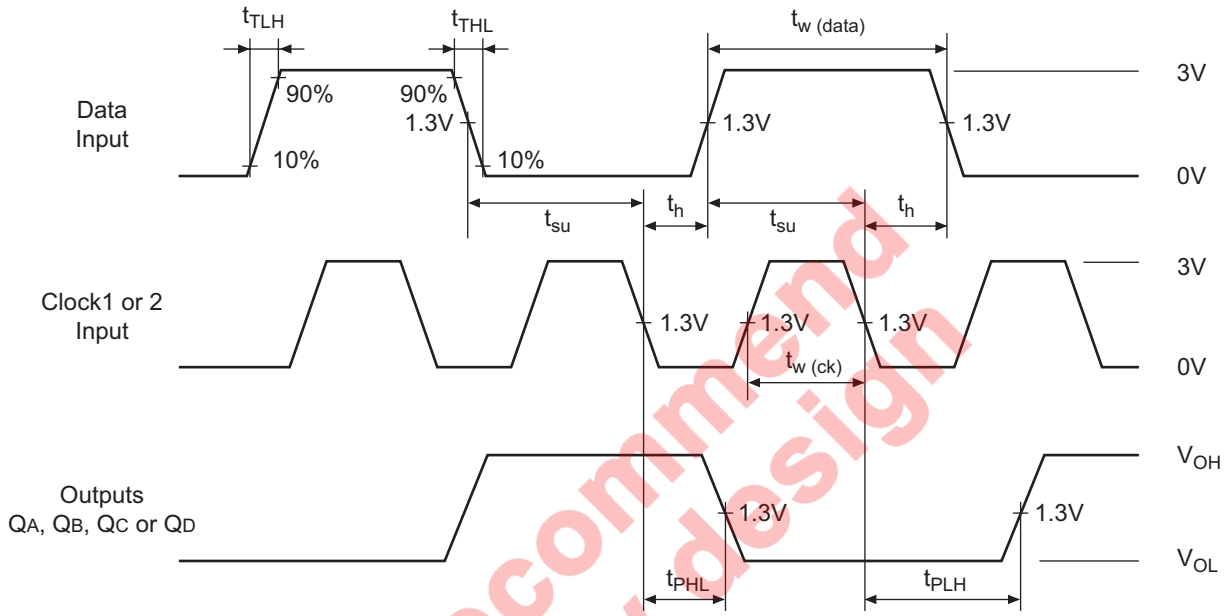



Notes: 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074(H).

## Testing Table

| Item | From input to output | Inputs | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CK-1 | CK-2 | Mode control | Serial Inputs | A | B | C | D | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| $f_{max}$ | CK-1 → Q | IN | 4.5 V | 0 V | IN | 4.5 V | 4.5 V | 4.5 V | 4.5 V | OUT | OUT | OUT | OUT |
| | CK-2 → Q | 4.5 V | IN | 4.5 V | 4.5 V | IN | IN | IN | IN | OUT | OUT | OUT | OUT |
| $t_{PLH}$ $t_{PHL}$ | CK-1 → Q | IN | 4.5 V | 0 V | IN | 4.5 V | 4.5 V | 4.5 V | 4.5 V | OUT | OUT | OUT | OUT |
| | CK-2 → Q | 4.5 V | IN | 4.5 V | 4.5 V | IN | IN | IN | IN | OUT | OUT | OUT | OUT |

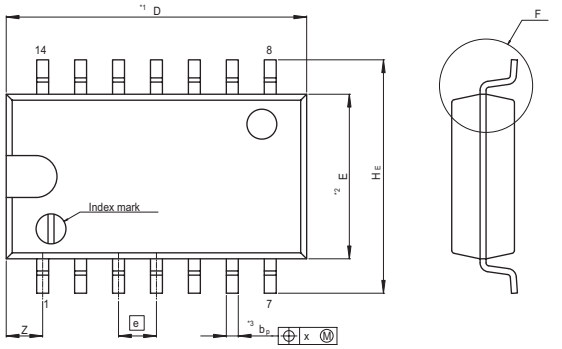
## Waveform

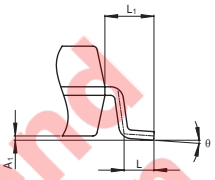



Note: Input pulse; $t_{TLH}$, $t_{THL} \leq 10$ ns, Data PRR = 500 kHz, Clock PRR = 1 MHz,

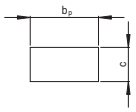
## Package Dimensions

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-SOP14-5.5x10.06-1.27 | PRSP0014DF-B | FP-14DAV | 0.23g |




Detail F




Terminal cross section
( Ni/Pd/Au plating )

NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 10.06 | 10.5 |
| E | — | 5.50 | — |
| $A_2$ | — | — | — |
| $A_1$ | 0.00 | 0.10 | 0.20 |
| A | — | — | 2.20 |
| $b_p$ | 0.34 | 0.40 | 0.46 |
| $b_1$ | — | — | — |
| c | 0.15 | 0.20 | 0.25 |
| $c_1$ | — | — | — |
| θ | 0° | — | 8° |
| $H_E$ | 7.50 | 7.80 | 8.00 |
| e | — | 1.27 | — |
| x | — | — | 0.12 |
| y | — | — | 0.15 |
| Z | — | — | 1.42 |
| L | 0.50 | 0.70 | 0.90 |
| $L_1$ | — | 1.15 | — |

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