

FDD5N50

N-Channel MOSFET

500V, 4A, 1.4Ω

Features

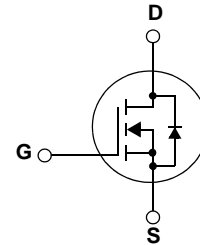
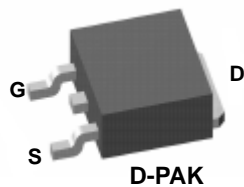
- $R_{DS(on)} = 1.15\Omega$ (Typ.) @ $V_{GS} = 10V, I_D = 2A$
- Low gate charge (Typ. 11nC)
- Low C_{rss} (Typ. 5pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant



Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pluse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted*

| Symbol | Parameter | Ratings | Units |
|----------------|--|--|------------------|
| V_{DSS} | Drain to Source Voltage | 500 | V |
| V_{GSS} | Gate to Source Voltage | ± 30 | V |
| I_D | Drain Current | - Continuous ($T_C = 25^\circ\text{C}$) | 4 |
| | | - Continuous ($T_C = 100^\circ\text{C}$) | 2.4 |
| I_{DM} | Drain Current | - Pulsed (Note 1) | 16 |
| E_{AS} | Single Pulsed Avalanche Energy | (Note 2) | 256 |
| I_{AR} | Avalanche Current | (Note 1) | 4 |
| E_{AR} | Repetitive Avalanche Energy | (Note 1) | 4 |
| dv/dt | Peak Diode Recovery dv/dt | (Note 3) | 4.5 |
| P_D | Power Dissipation | ($T_C = 25^\circ\text{C}$) | 40 |
| | | - Derate above 25°C | 0.3 |
| T_J, T_{STG} | Operating and Storage Temperature Range | -55 to +150 | $^\circ\text{C}$ |
| T_L | Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds | 300 | $^\circ\text{C}$ |

Thermal Characteristics

| Symbol | Parameter | Ratings | Units |
|-----------------|---|---------|---------------------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 1.4 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 110 | |

Package Marking and Ordering Information $T_C = 25^\circ\text{C}$ unless otherwise noted

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|----------------|-----------|---------|-----------|------------|----------|
| FDD5N50 | FDD5N50TM | D-PAK | 380mm | 16mm | 2500 |
| FDD5N50 | FDD5N50TF | D-PAK | 380mm | 16mm | 2000 |

Electrical Characteristics

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|--------|-----------|-----------------|------|------|------|-------|
|--------|-----------|-----------------|------|------|------|-------|

Off Characteristics

| | | | | | | |
|--------------------------------------|---|---|-----|-----|-----------|--------------------|
| BV_{DSS} | Drain to Source Breakdown Voltage | $I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$ | 500 | - | - | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\mu\text{A}$, Referenced to 25°C | - | 0.6 | - | $V/^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 500\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = 400\text{V}, T_C = 125^\circ\text{C}$ | - | - | 1 10 | μA |
| I_{GSS} | Gate to Body Leakage Current | $V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$ | - | - | ± 100 | nA |

On Characteristics

| | | | | | | |
|--------------|--------------------------------------|---|-----|------|-----|----------|
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ | 3.0 | - | 5.0 | V |
| $R_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS} = 10\text{V}, I_D = 2\text{A}$ | - | 1.15 | 1.4 | Ω |
| g_{FS} | Forward Transconductance | $V_{DS} = 20\text{V}, I_D = 2\text{A}$ (Note 4) | - | 4.3 | - | S |

Dynamic Characteristics

| | | | | | | |
|--------------|-------------------------------|--|---|-----|-----|----|
| C_{iss} | Input Capacitance | $V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$ | - | 480 | 640 | pF |
| C_{oss} | Output Capacitance | | - | 66 | 88 | pF |
| C_{rss} | Reverse Transfer Capacitance | | - | 5 | 8 | pF |
| $Q_{g(tot)}$ | Total Gate Charge at 10V | $V_{DS} = 400\text{V}, I_D = 5\text{A}$ $V_{GS} = 10\text{V}$ (Note 4, 5) | - | 11 | 15 | nC |
| Q_{gs} | Gate to Source Gate Charge | | - | 3 | - | nC |
| Q_{gd} | Gate to Drain "Miller" Charge | | - | 5 | - | nC |

Switching Characteristics

| | | | | | | |
|--------------|---------------------|---|---|----|----|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 250\text{V}, I_D = 5\text{A}$ $R_G = 25\Omega$ (Note 4, 5) | - | 13 | 36 | ns |
| t_r | Turn-On Rise Time | | - | 22 | 54 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | - | 28 | 66 | ns |
| t_f | Turn-Off Fall Time | | - | 20 | 50 | ns |

Drain-Source Diode Characteristics

| | | | | | | |
|----------|--|--|---|-----|-----|---------------|
| I_S | Maximum Continuous Drain to Source Diode Forward Current | - | - | 4 | A | |
| I_{SM} | Maximum Pulsed Drain to Source Diode Forward Current | - | - | 16 | A | |
| V_{SD} | Drain to Source Diode Forward Voltage | $V_{GS} = 0\text{V}, I_{SD} = 4\text{A}$ | - | - | 1.4 | V |
| t_{rr} | Reverse Recovery Time | $V_{GS} = 0\text{V}, I_{SD} = 5\text{A}$ | - | 300 | - | ns |
| Q_{rr} | Reverse Recovery Charge | $di_F/dt = 100\text{A}/\mu\text{s}$ (Note 4) | - | 1.8 | - | μC |

Notes:

- 1: Repetitive Rating: Pulse width limited by maximum junction temperature
- 2: $L = 32\text{mH}, I_{AS} = 4\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
- 3: $I_{SD} \leq 4\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
- 4: Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
- 5: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

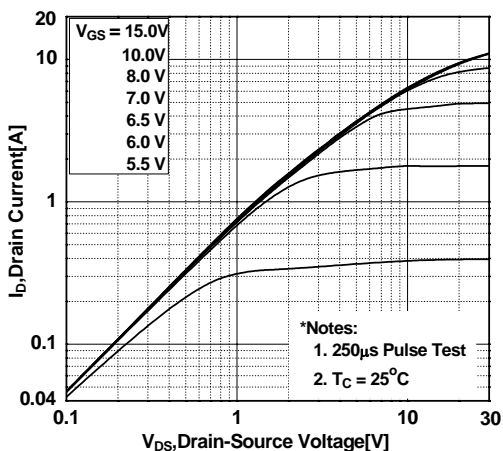


Figure 2. Transfer Characteristics

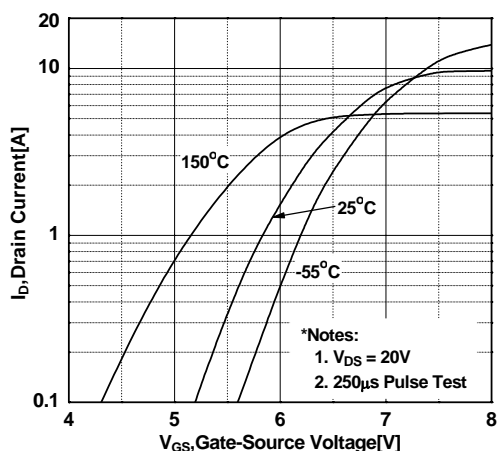


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

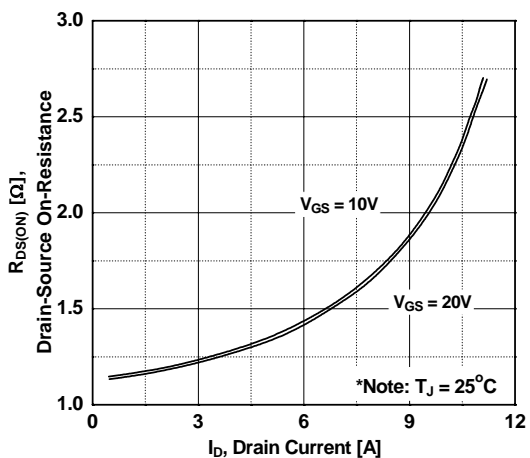


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

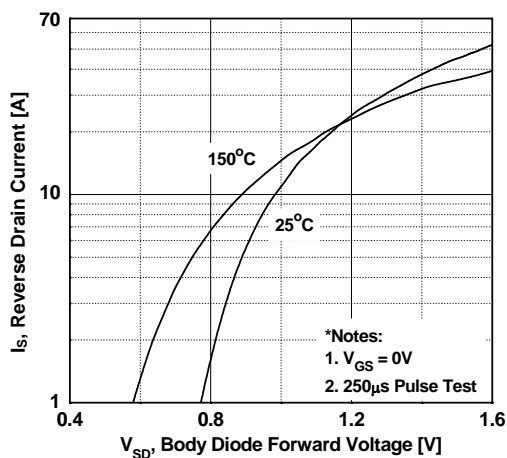


Figure 5. Capacitance Characteristics

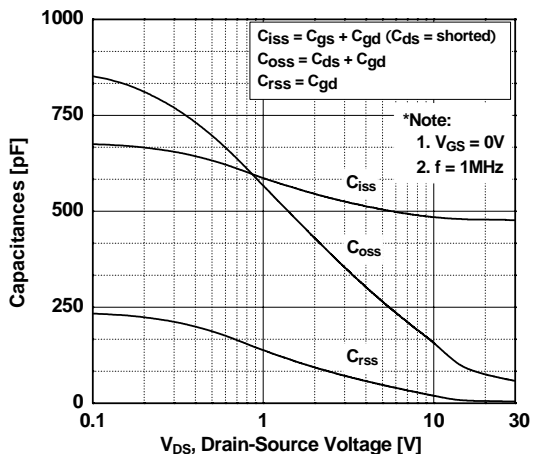
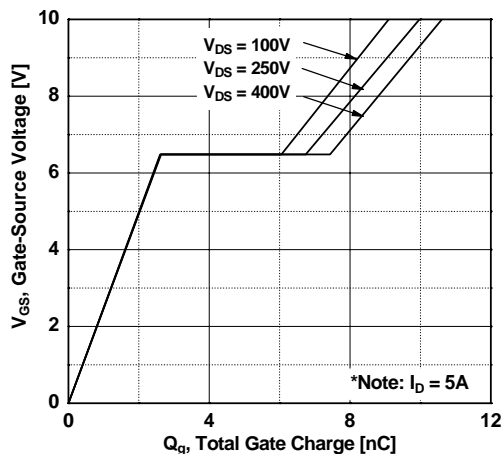


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

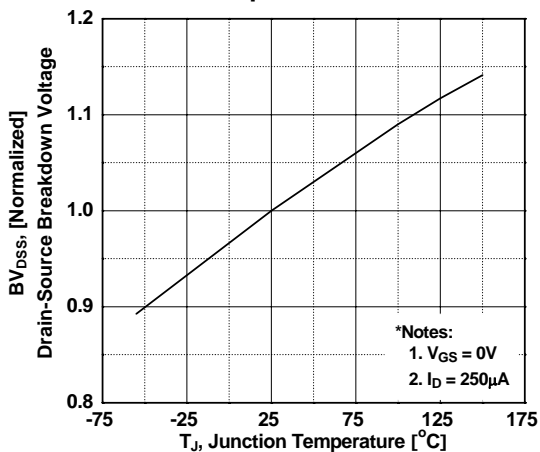


Figure 8. On-Resistance Variation vs. Temperature

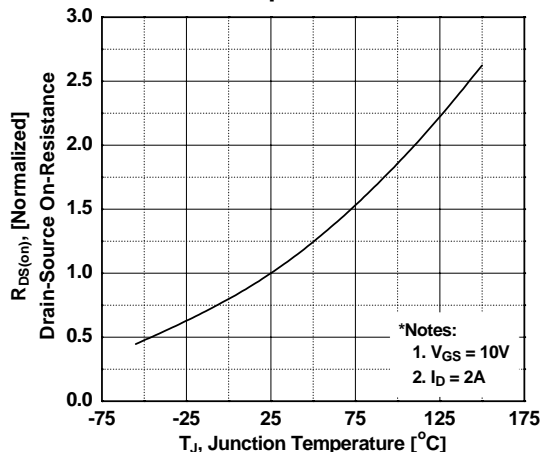


Figure 9. Maximum Safe Operating Area

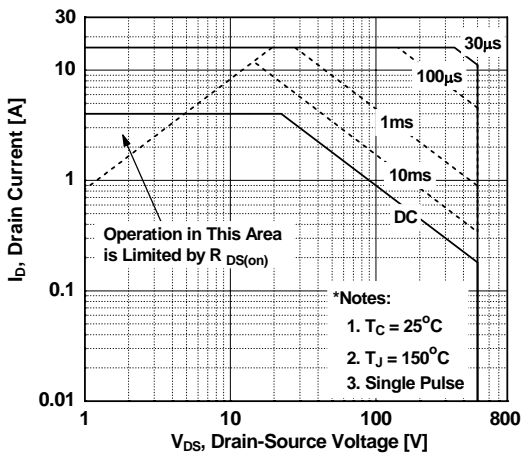


Figure 10. Maximum Drain Current vs. Case Temperature

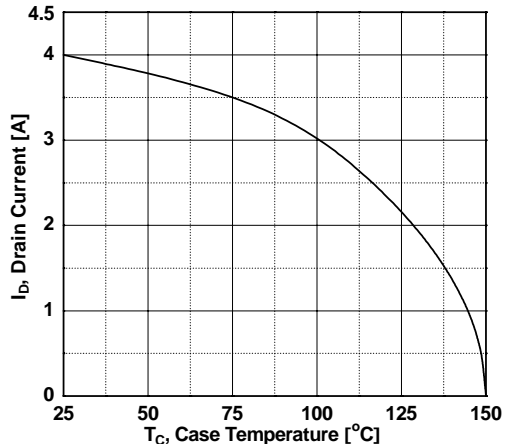
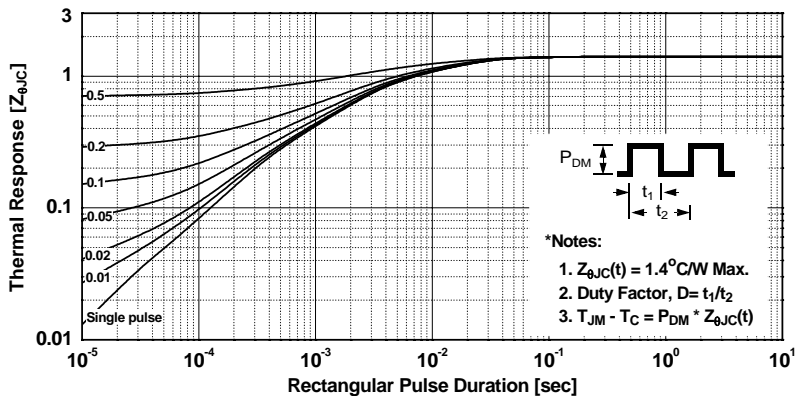
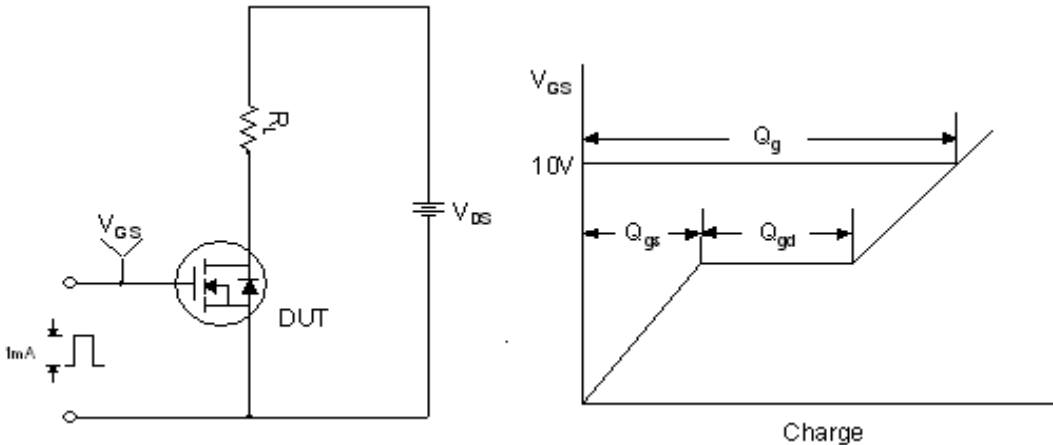


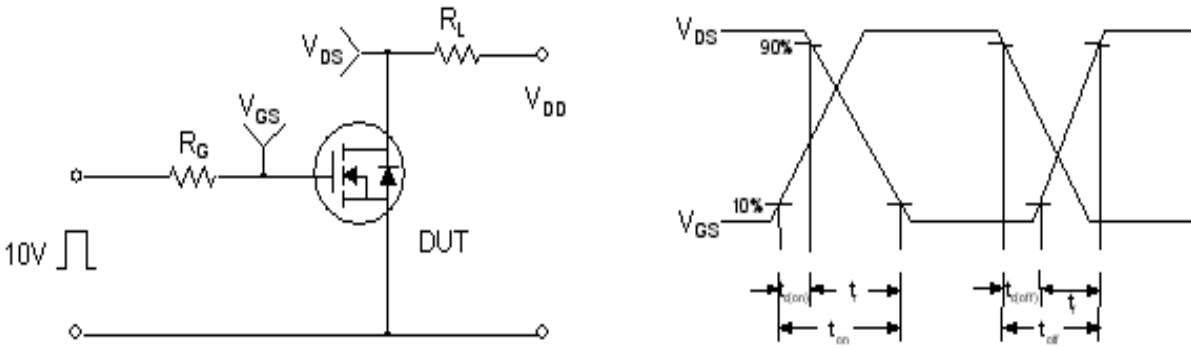
Figure 11. Transient Thermal Response Curve



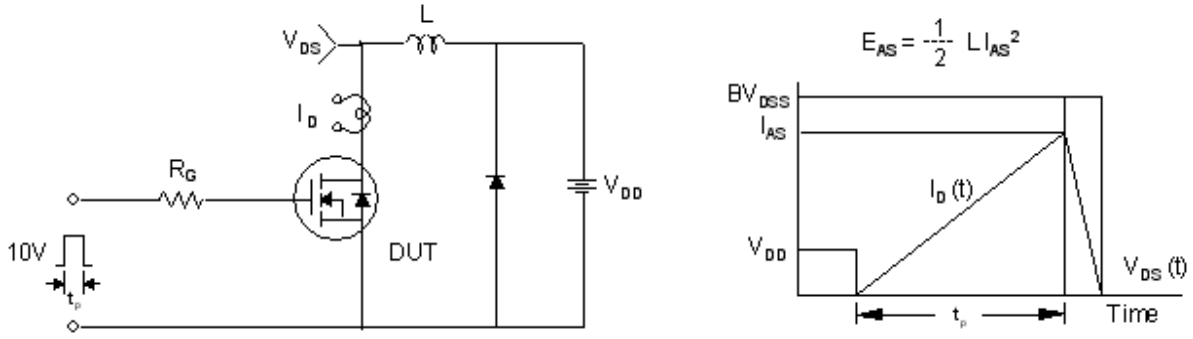
Gate Charge Test Circuit & Waveform



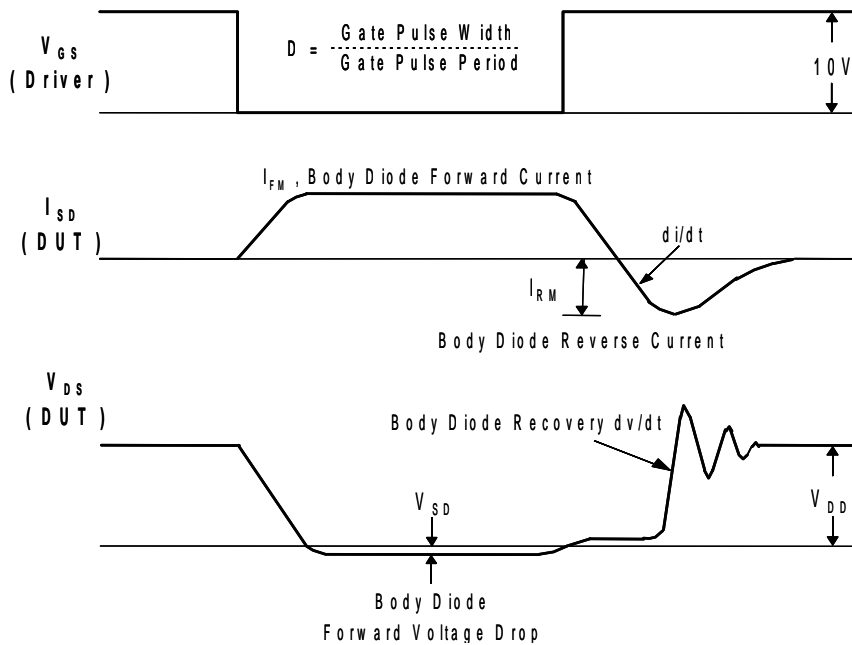
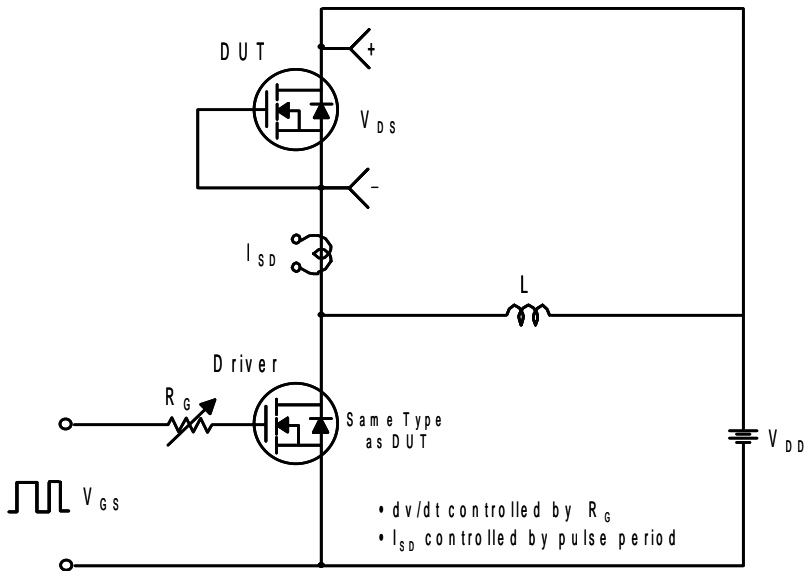
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

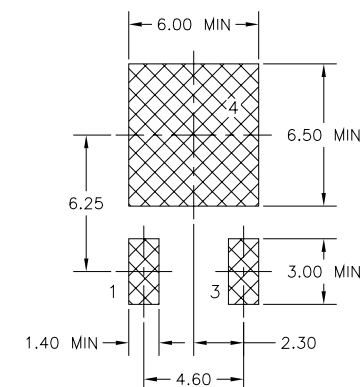
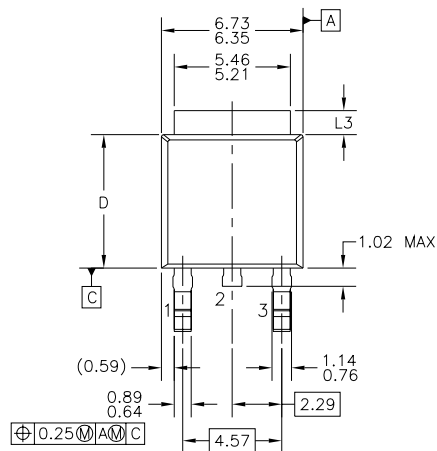


Peak Diode Recovery dv/dt Test Circuit & Waveforms

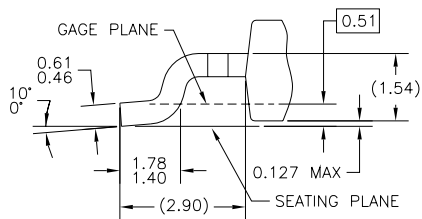
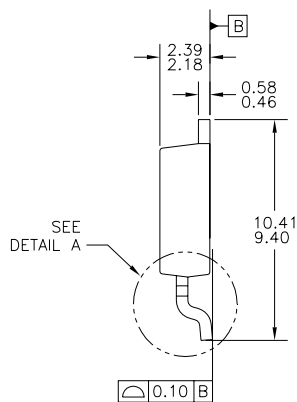
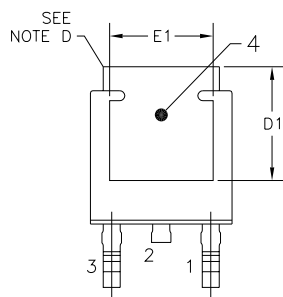


Mechanical Dimensions

D-PAK



LAND PATTERN RECOMMENDATION



DETAIL A
(ROTATED -90°)
SCALE: 12X

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) DIMENSIONS L3,D,E1&D1 TABLE:
- | | OPTION AA | OPTION AB |
|----|-----------|-----------|
| L3 | 0.89-1.27 | 1.52-2.03 |
| D | 5.97-6.22 | 5.33-5.59 |
| E1 | 4.32 MIN | 3.81 MIN |
| D1 | 5.21 MIN | 4.57 MIN |
- F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters



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| Build it Now™ | FRFET® | Power220® |  SYSTEM GENERAL® |
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| Current Transfer Logic™ | GTO™ | PowerTrench® | TinyBuck™ |
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| |  ® | SuperSOT™-6 | |
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