

2-Mbit (256K x 8) Static RAM

Features

- Pin and function compatible with CY7C1010CV33
- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - $I_{CC} = 90 \text{ mA @ } 10 \text{ ns}$
- Low CMOS standby power
 - $I_{SB2} = 10 \text{ mA}$
- 2.0V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with CE and OE features
- Available in Lead-Free 44-pin TSOP II package

Functional Description^[1]

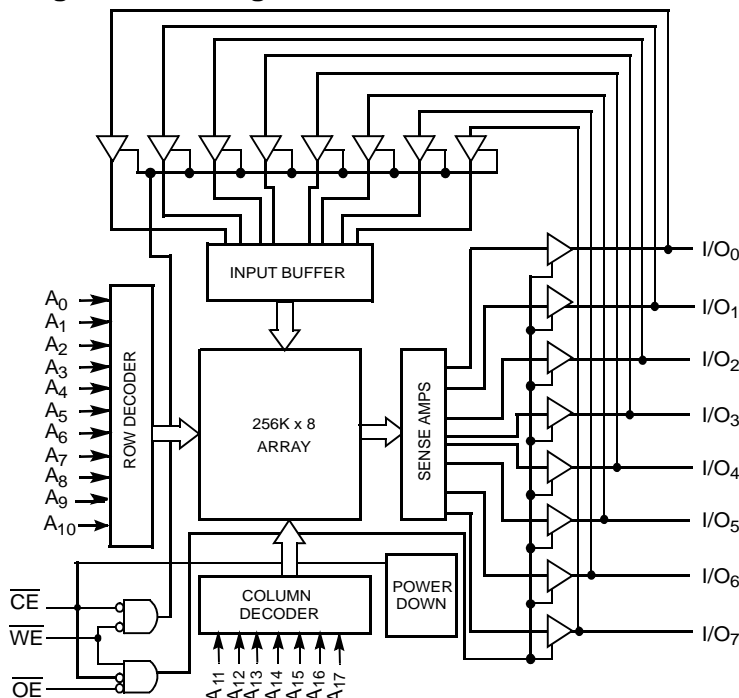
The CY7C1010DV33 is a high-performance CMOS Static RAM organized as 256K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}), and three-state drivers. Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a Write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1010DV33 is available in standard 44-pin TSOP II package with center power and ground (revolutionary) pinout.

Logic Block Diagram



Pin Configuration

TSOP II Top View

NC	1	44	NC
NC	2	43	NC
A_4	3	42	NC
A_3	4	41	A_5
A_2	5	40	A_6
A_1	6	39	A_7
A_0	7	38	A_8
\overline{CE}	8	37	\overline{OE}
I/O_0	9	36	I/O_7
I/O_1	10	35	I/O_6
V_{CC}	11	34	V_{SS}
V_{SS}	12	33	V_{CC}
I/O_2	13	32	I/O_5
I/O_3	14	31	I/O_4
\overline{WE}	15	30	A_9
A_{17}	16	29	A_{10}
A_{16}	17	28	A_{11}
A_{15}	18	27	A_{12}
A_{14}	19	26	NC
A_{13}	20	25	NC
NC	21	24	NC
NC	22	23	NC

Selection Guide

	-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	90	mA
Maximum CMOS Standby Current	10	mA

Note:

1. For guidelines on SRAM system design, please refer to the *System Design Guidelines* Cypress application note, available on the internet at www.cypress.com

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied..... -55°C to +125°C
 Supply Voltage on V_{CC} to Relative GND^[2] -0.5V to +4.6V
 DC Voltage Applied to Outputs in High-Z State^[2] -0.3V to V_{CC}+0.3V

DC Input Voltage^[2] -0.3V to V_{CC}+0.3V
 Current into Outputs (LOW)..... 20 mA
 Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)
 Latch-up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	-40°C to +85°C	3.3V ± 0.3V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-10		Unit
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min.; I _{OH} = -4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min.; I _{OL} = 8.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[2]		-0.3	0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled	-1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., f = f _{MAX} = 1/t _{RC}	100 MHz	90	mA
			83 MHz	80	
			66 MHz	70	
			40 MHz	60	
I _{SB1}	Automatic CE Power-down Current — TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} ; V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} ; f = f _{MAX}		20	mA
I _{SB2}	Automatic CE Power-down Current — CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0		10	mA

Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V	8	pF
C _{OUT}	I/O Capacitance		8	pF

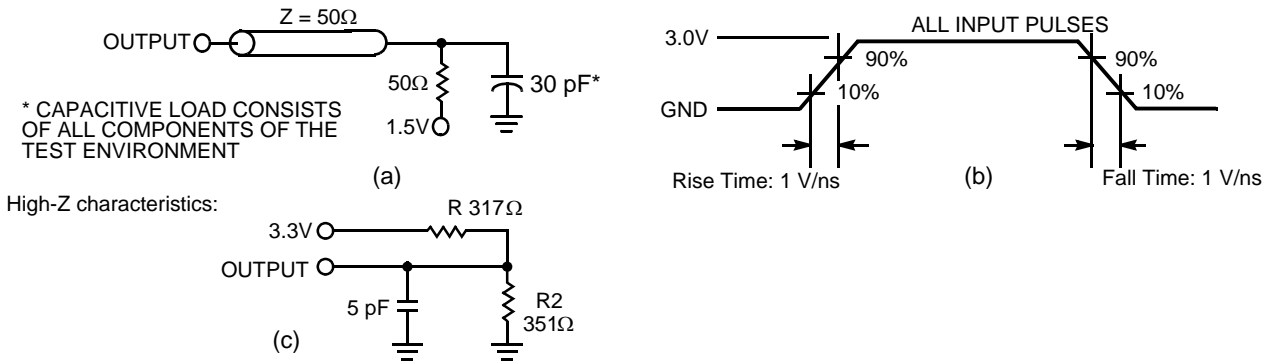
Thermal Resistance^[3]

Parameter	Description	Test Conditions	44-TSOP-II	Unit
Θ _{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	50.66	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case)		17.77	°C/W

Notes:

- V_{IL} (min.) = -2.0V and V_{IH} (max.) = V_{CC} + 2.0V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms^[4]



AC Switching Characteristics Over the Operating Range^[5]

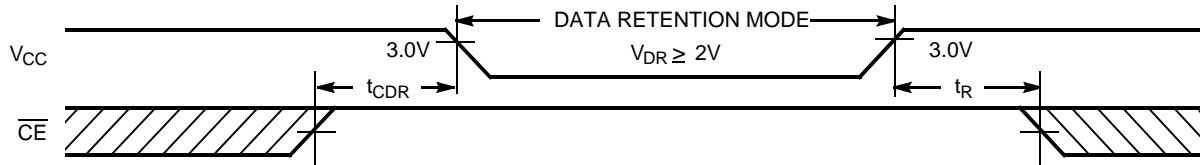
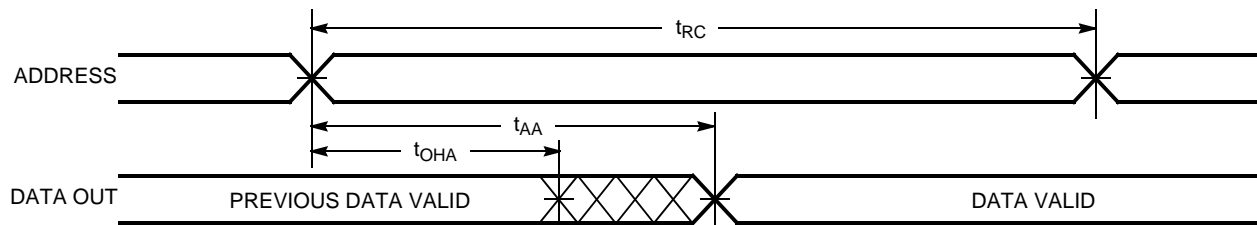
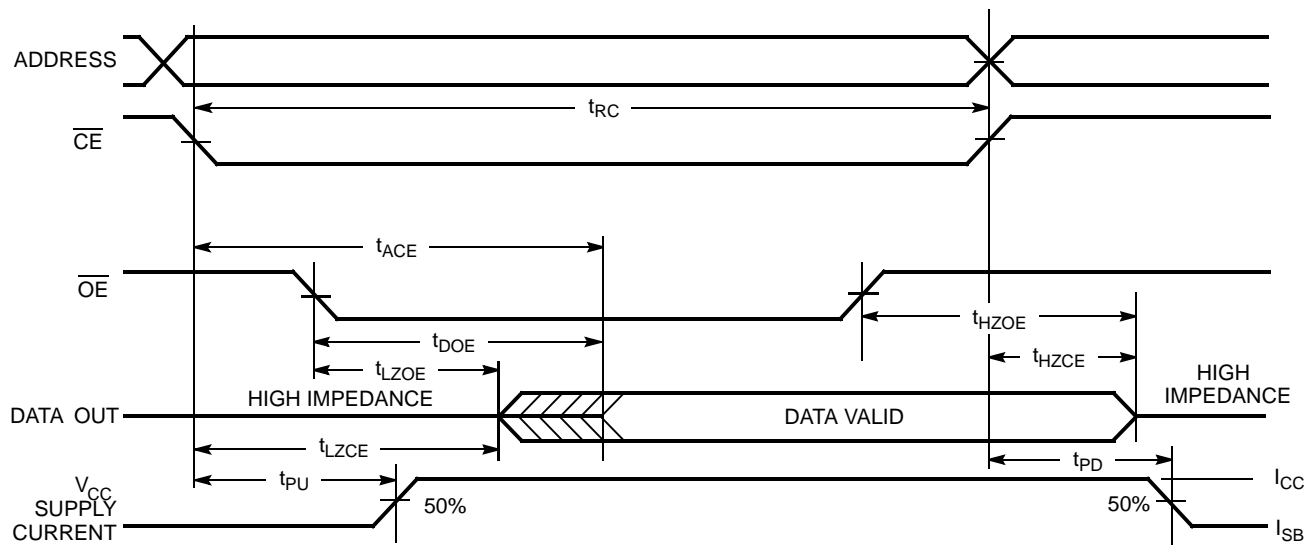
Parameter	Description	-10		Unit
		Min.	Max.	
Read Cycle				
$t_{power}^{[6]}$	V_{CC} (typical) to the first access	100		μs
t_{RC}	Read Cycle Time	10		ns
t_{AA}	Address to Data Valid		10	ns
t_{OHA}	Data Hold from Address Change	3		ns
t_{ACE}	\overline{CE} LOW to Data Valid		10	ns
t_{DOE}	\overline{OE} LOW to Data Valid		5	ns
t_{LZOE}	\overline{OE} LOW to Low-Z	0		ns
t_{HZOE}	\overline{OE} HIGH to High-Z ^[7, 8]		5	ns
t_{LZCE}	\overline{CE} LOW to Low-Z ^[8]	3		ns
t_{HZCE}	\overline{CE} HIGH to High-Z ^[7, 8]		5	ns
t_{PU}	\overline{CE} LOW to Power-up	0		ns
t_{PD}	\overline{CE} HIGH to Power-down		10	ns
Write Cycle^[9, 10]				
t_{WC}	Write Cycle Time	10		ns
t_{SCE}	\overline{CE} LOW to Write End	7		ns
t_{AW}	Address Set-up to Write End	7		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-up to Write Start	0		ns
t_{PWE}	\overline{WE} Pulse Width	7		ns
t_{SD}	Data Set-up to Write End	5		ns
t_{HD}	Data Hold from Write End	0		ns
t_{LZWE}	\overline{WE} HIGH to Low-Z ^[8]	3		ns
t_{HZWE}	\overline{WE} LOW to High-Z ^[7, 8]		5	ns

Notes:

- AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
- t_{power} gives the minimum amount of time that the power supply should be at stable, typical V_{CC} values until the first memory access can be performed.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal Write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Data Retention Characteristics Over the Operating Range^[12]

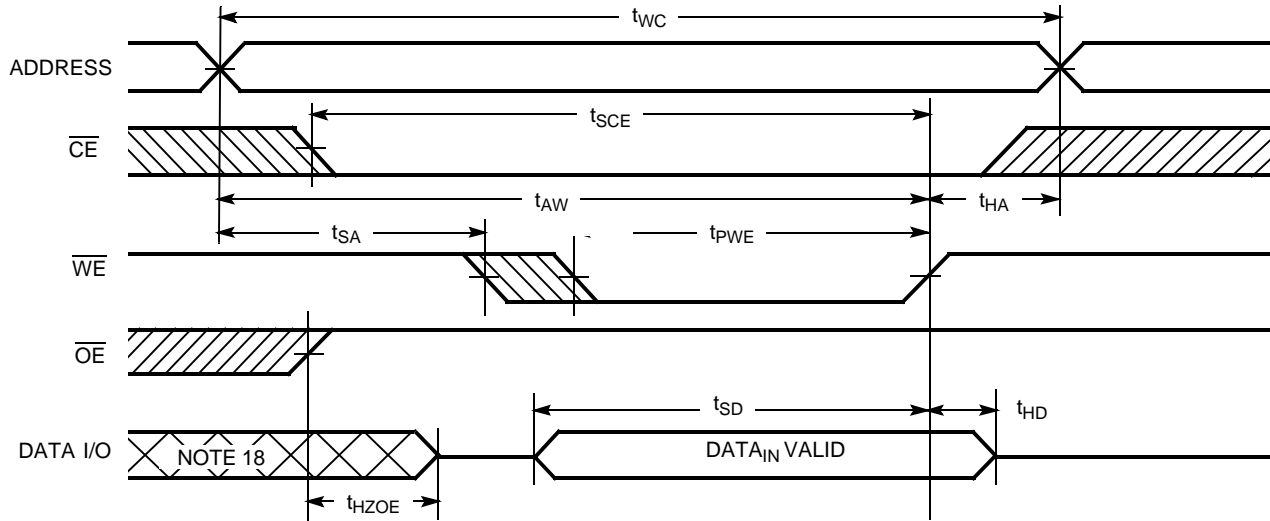
Parameter	Description	Conditions	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current			10	mA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time	$V_{CC} = V_{DR} = 2.0V, \overline{CE} \geq V_{CC} - 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
$t_R^{[11]}$	Operation Recovery Time		t_{RC}		ns

Data Retention Waveform

Switching Waveforms
Read Cycle No. 1^[13, 14]

Read Cycle No. 2 (OE Controlled)^[14, 15]

Notes:

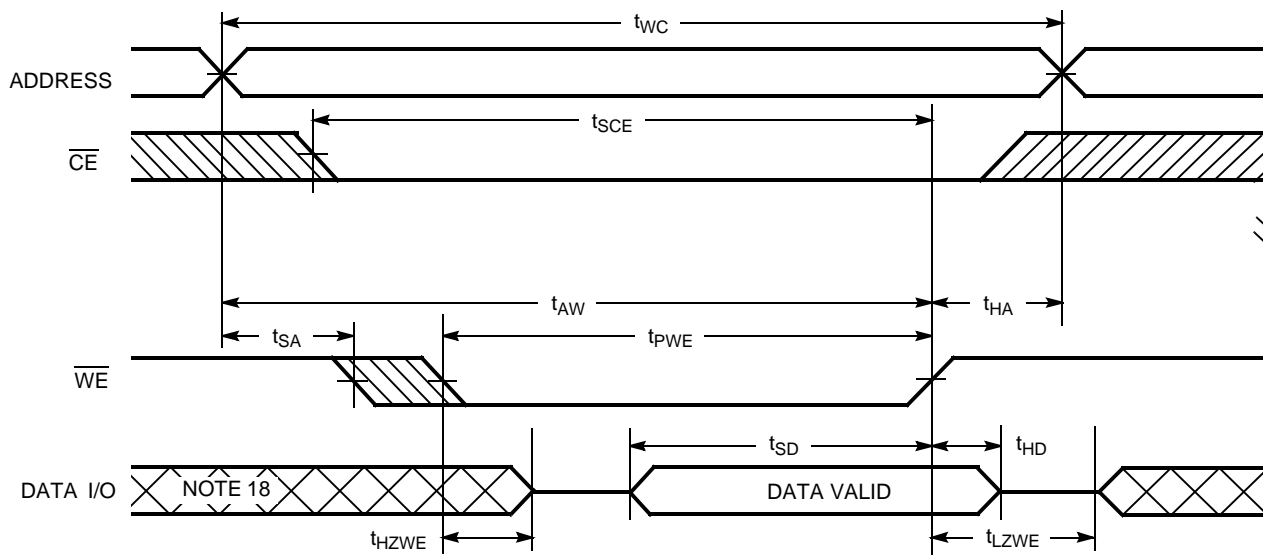
11. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50 \mu s$ or stable at $V_{CC(min.)} \geq 50 \mu s$.
12. No inputs may exceed $V_{CC} + 0.3V$.
13. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
14. \overline{WE} is HIGH for Read cycle.
15. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[16, 17]



Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} LOW)^[17]



Notes:

- 16. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
- 17. If CE goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.
- 18. During this period, the I/Os are in output state and input signals should not be applied.

Truth Table

CE	OE	WE	I/O ₀ -I/O ₇	Mode	Power
H	X	X	High-Z	Power-down	Standby (I _{SB})
L	L	H	Data Out	Read	Active (I _{CC})
L	X	L	Data In	Write	Active (I _{CC})
L	H	H	High-Z	Selected, Outputs Disabled	Active (I _{CC})

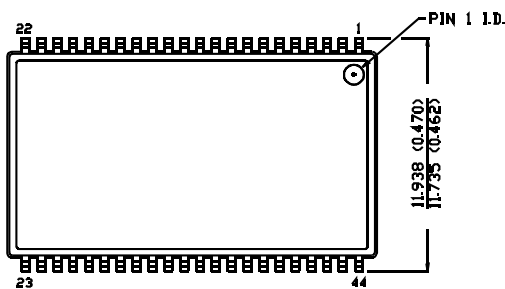
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1010DV33-10ZSXI	51-85087	44-pin TSOP II (Pb-Free)	Industrial

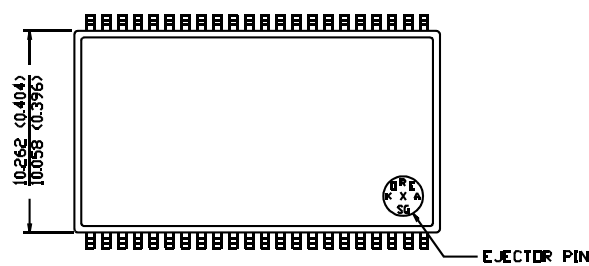
Package Diagram

44-pin TSOP II (51-85087)

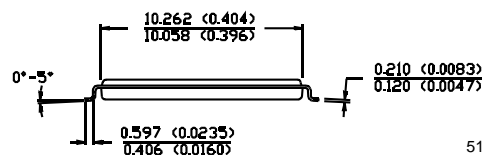
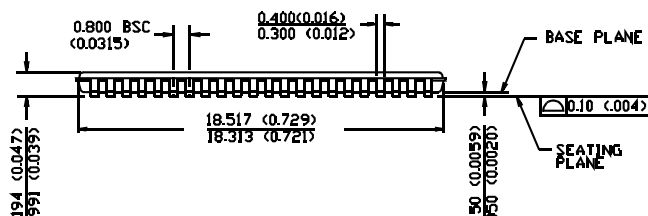
MAX
MIN



TOP VIEW



BOTTOM VIEW



51-85087-A

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Document History Page

Document Title: CY7C1010DV33 2-Mbit (256K x 8)Static RAM				
Document Number: 001-00062				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	342195	See ECN	PCI	New Data sheet
*A	459073	See ECN	NXR	Converted Preliminary to Final. Removed Commercial Operating Range from product offering. Removed -8 ns and -12 speed bin Removed the Pin definitions table. Modified Maximum Ratings for DC input voltage from -0.5V to -0.3V and $V_{CC} + 0.5V$ to $V_{CC} + 0.3V$ Changed I_{CC} max from 65 mA to 90 mA Changed the description of I_{IX} from "Input Load Current" to "Input Leakage Current" Updated the Thermal Resistance table. Updated footnote #7 on High-Z parameter measurement Added footnote #12 Updated the Ordering Information and replaced Package Name column with Package Diagram in the Ordering Information table.