AT5510

Preliminary Product Information

120mA, Current Sinking, 10-bit I²C DAC for VCM Driver

Features

- 120mA current sink.
- 2-wire (I²C-compatible) serial interface
- 10-bit resolution
- Integrated current sense resistor
- 2.7V to 3.6V power supply
- Power-down mode
- Power-down to 0.5μA typical
- Power-on reset
- DFN-8 & WLCSP package

Applications

- Auto-focus of camera modules
- Shutters
- Lens covers
- Image stabilization

General Description

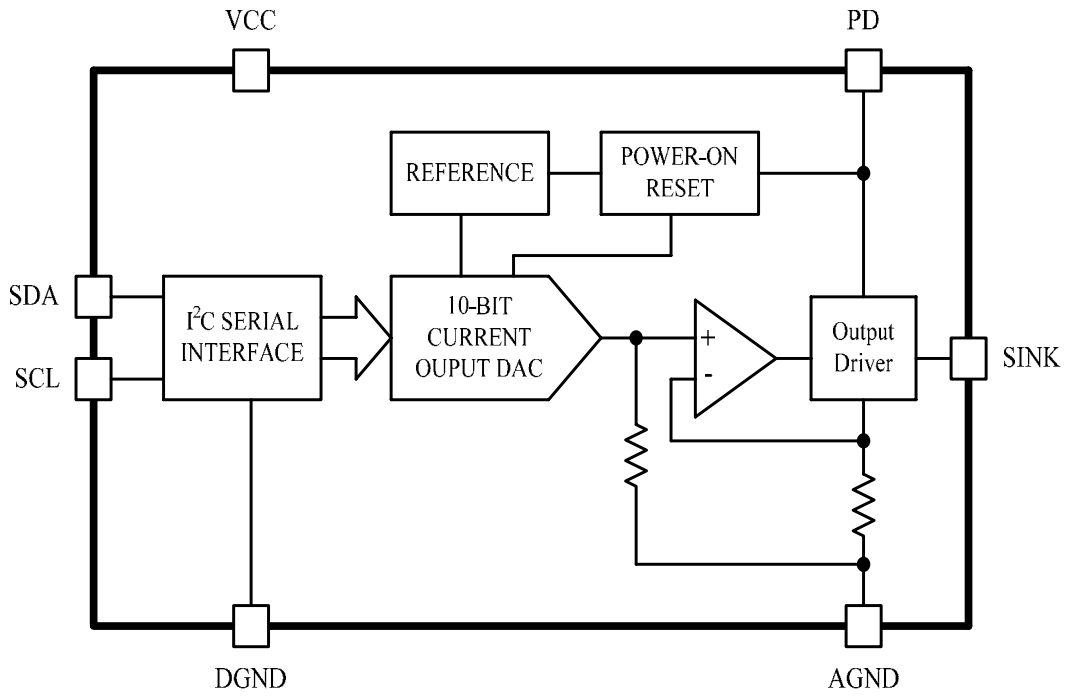
The AT5510 is a single 10-bit DAC with 120mA output current sink capability. It operates from 2.7V to 5.5V supply. The DAC is controlled via 2-wire (I²C-compatible) serial interface that operates at clock rates up to 400KHz.

The AT5510 provides a power-down mode. The power-down mode can be enabled by PD pin or I²C interface. At power-down mode, the output current reduces to 1μA maximum.

The AT5510 is designed for autofocus, image stabilization, and optical zoom applications in camera modules.

The AT5510 is available in DFN-8 or WLCSP package.

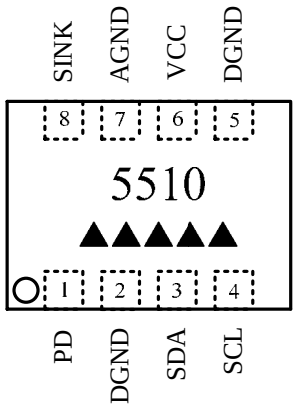
Block Diagram



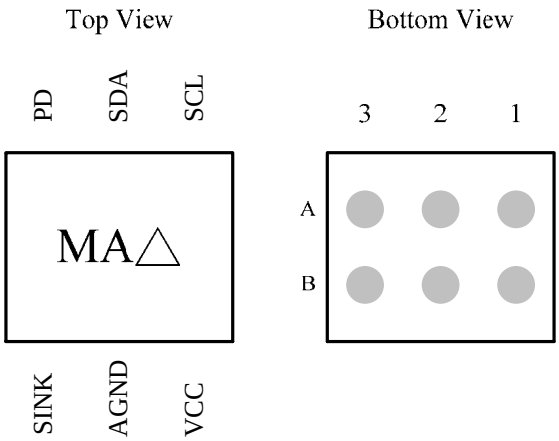
Aimtron reserves the right without notice to change this circuitry and specifications.

Pin Configuration

DFN-8



WLCSP



Ordering Information

Part number	Package	Marking
AT5510N_GRE	DFN-8, Green	5510,▲▲▲▲▲▲
AT5510G_PBF	WLCSP-6, PBF	MA△

▲▲▲▲▲▲: Date Code

△:serial number

**For more marking information, contact out sales representative directly*

Pin Description

DFN-8

Symbol	Pin No.	Descript
PD	1	Power down control pin
DGND	2	Digital power ground
SDA	3	I^2C interface signal input
SCL	4	I^2C interface signal input
DGND	5	Digital power ground
VCC	6	Power supply
AGND	7	Analog power ground
SINK	8	Output current sink

WLCSP-6

Symbol	Pin No.	Descript
PD	A1	Power down control pin
SDA	A2	I^2C interface signal input
SCL	A3	I^2C interface signal input
SINK	B1	Output current sink
AGND	B2	Analog power ground
VCC	B3	Power supply

Absolute Maximum Ratings [*1]

(Ta=+25°C)

Parameter	Condition	Rated Value		Unit
		Min.	Max.	
Power Supply Voltage, VCC	—	-0.3	+6.0	V
AGND to DGND	—	-0.3	+0.3	V
SCL, SDA to DGND	—	-0.3	VCC	V
PD to DGND	—	-0.3	VCC	V
SINK to AGND	—	-0.3	VCC+0.3	V
Output Sink Current	—	--	120	mA
Thermal Resistance from Junction to Ambient θ_{JA} [*2]	DFN-8	--	50	°C/W
	WLCSP(4-Layer PCB)	--	TBD	°C/W
Operating temperature T_A	—	-40	+85	°C
Storage temperature	—	-65	+150	°C
Junction temperature $T_{J, MAX}$	—	--	150	°C
ESD Susceptibility [*3]	HBM	2		KV
	MM	200		V

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. The accuracy of θ_{JA} will be based on PC board layout. See details of "Thermal Considerations" in Application Information.

3. Devices are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.

Recommended Operating Conditions

(Ta=+25°C)

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Power supply voltage	VCC	2.5	--	5.5	V
SCL, SDA voltage	VSCL VSDA	--	--	VCC	V
PD voltage	VPD	--	--	VCC	V
Operating temperature*	T_A	-20	+25	+85	°C

***Using X5R or X7R input capacitors.**

Electrical Characteristics

(VCC= 2.7~3.6V,T_a =+25℃ , unless otherwise noted.)

Parameter	Symbol	Condition	Values			Unit
			Min.	Typ.	Max.	
Power Supply						
Power supply *1	VCC		2.7	--	3.6	V
Input current *2	ICC			2.3	3	mA
	ICC_{PD}	PD=1		0.5	2	μA
Output Characteristics						
Min. sink current	$I_{SINK,MIN}$		--	3	--	mA
Max. sink current	$I_{SINK,MAX}$		--	120	--	mA
Output current during PD	$I_{SINK,PD}$	PD=1	--	80	--	nA
Power-up time	t_{PU}	To 10% of FS, coming out of power-down mode	--	200	--	μs
PD Input						
Input current	I_{PD}		--	--	±1	μA
H level input voltage	V_{PDH}		1.26	--	VCC +0.3	V
L level input voltage	V_{PDL}		-0.3	--	0.54	V
SCA, SDL Input *3						
H level input voltage	V_{INH}		1.26	--	VCC +0.3	V
L level input voltage	V_{INL}		-0.3	--	0.54	V
Input current	I_{IN}		--	--	±1	μA
Input hysteresis	V_{SYST}		0.05* VCC	--	--	V
Glitch rejection			--	--	50	ns
DC Performance						
Least significant bit	LSB	10 bits resolution	--	117	--	μA
Resolution	--	117uA/LSB	--	10	--	Bits
Integral nonlinearity	INL			±1.5	±4	LSB
Differential nonlinearity	DNL	Guaranteed monotonic over all codes	--	--	±1	LSB
Zero code error	--	All 0s loads to DAC	--	0	--	mA
Offset error @Code 16	Ios		--	0.5	--	mA
Gain error	--		--	±0.6	--	% of
Offset error drift *3	--		--	10	--	μA/°C
Gain error drift *3	--		--	±0.2	--	LSB/°C

1. The maximum of VCC can achieve up to 5.5V. But if VCC is over 3.6V, the total electrical characteristics may not meet the specification above.
2. ICC specification is valid for all DAC codes.
3. Guaranteed by design and characterization.

Typical Application Circuit

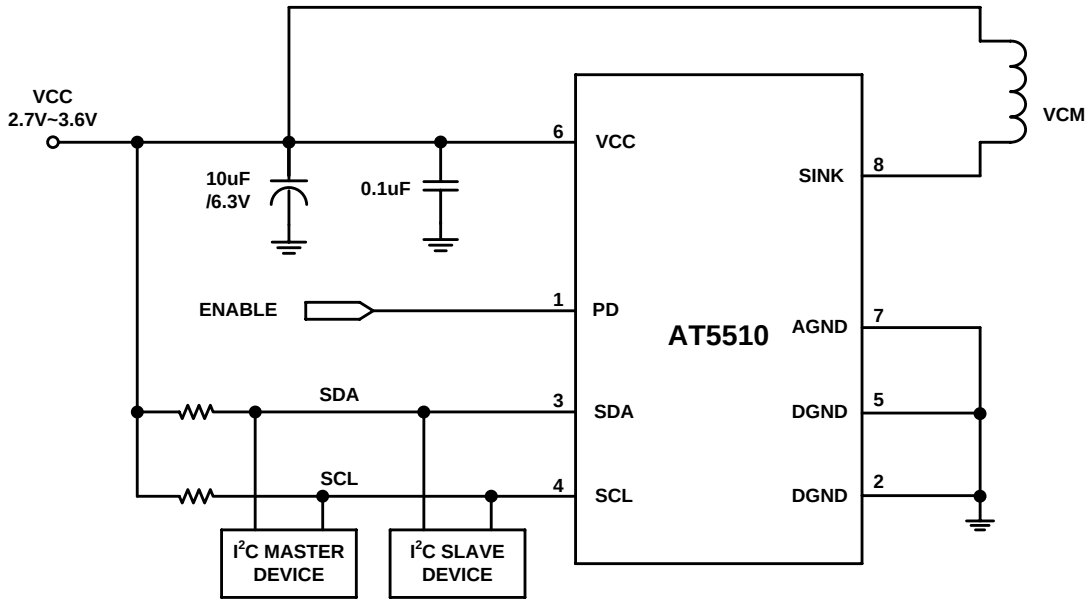


Figure 1

The output current can be set as

$$I_{SINK} = Ios + CODE * LSB,$$

where I_{SINK} is output driving current, Ios is the offset error and CODE is the data bits (D0-D9) shown in Table 2.

The popular examples are shown in Table 1.

Table 1: Code transfers to I_{SINK}

CODE	33	252	765	1023
Serial Data Bit	0x180210	0x180FC0	0x182FD0	0x183FF0
I_{SINK} (mA)	4.36	29.98	90.01	120.19

* Ios=0.5mA, LSB=117μA.

Terminology

- **Resolution**

  Resolution of DAC is the number of bits to present the analog output signal.

- **Integral nonlinearity (INL)**

  Integral nonlinearity is a measurement of the maximum deviation, in LSB, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 3.

- **Differential nonlinearity (DNL)**

  Differential nonlinearity is the difference between the measured and ideal 1 LSB change by any two adjacent code. A typical DNL vs. code plot is shown in Figure 4.

- **Zero-code error**

  Zero-code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. The zero-code error is positive in AT5510.

- **Gain error**

  Gain error is a measurement of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as percent of the full-scale range.

- **Offset error**

  Offset error is a measurement of the difference between actual output current (I_{SINK}) and ideal output current (Io). It is measured on the AT5510 with Code 16 loaded into the DAC register.

Application Information

Power-down mode

AT5510 can be operated in power-down mode when PD pin is at high voltage level (1.26V~VCC) or soft power-down enable. The PD bit (R15) of input register in serial data can be written 1 to power down or 0 to enable AT5510.

Table 2: Power-down mode

	PD = H	PD = L
DATA BYTE Bit 15 = 1	Power-down	Power-down
DATA BYTE Bit 15 = 0	Power-down	Power-up

Serial Interface Data Form

The AT5510 is controlled using I²C 2-wire serial protocol. Data can be written to or read from the DAC at data rates up to 400KHz. The address byte consists of a 7-bit address plus a read/write bit shown in Figure 5. The address of the AT5510 is 0001100. The read/write bit is 0 if data is written to the AT5510, and 1 if data is read from the AT5510.

The data byte has 16-bit shown in table 3, but not all bits of the input register data are used. The Bit 15 is power-down function; Bit 14 is unused; Bit 13 to Bit 4 correspond to the DAC data bits; Bit 3 to Bit 0 are unused.

The details about write and read operation are shown in Figure 5 and 6, respectively.

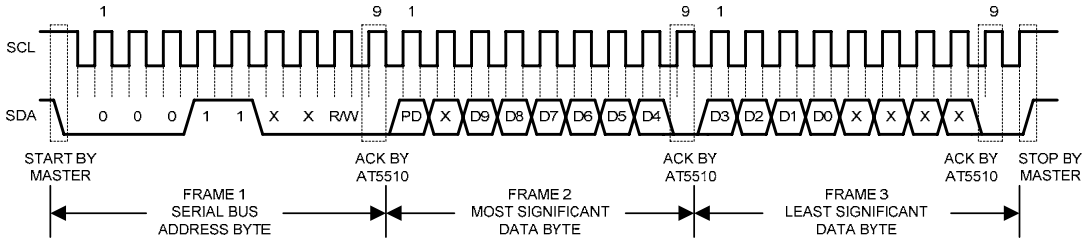


Figure 5: Write operation

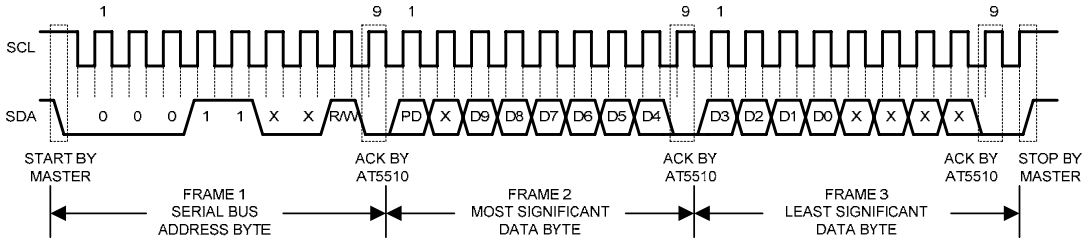


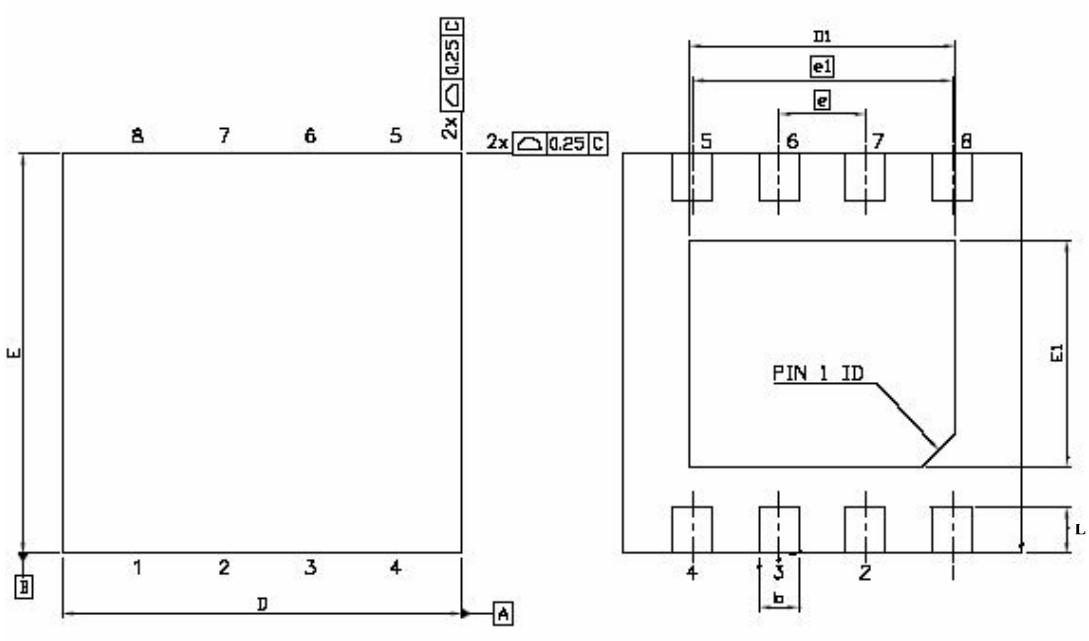
Figure 6: Read operation

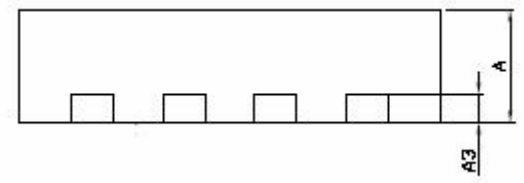
Table 3: Data format

Serial Data-Words	High Byte							
Serial Data Bits	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Input Register	R15	R14	R13	R12	R11	R10	R9	R8
Function	PD	--	D9	D8	D7	D6	D5	D4
Serial Data-Words	Low Byte							
Serial Data Bits	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Input Register	R7	R6	R5	R4	R3	R2	R1	R0
Function	D3	D2	D1	D0	--	--	--	--

* PD = soft power-down; -- = don't care; D9 to D0 =DAC data.

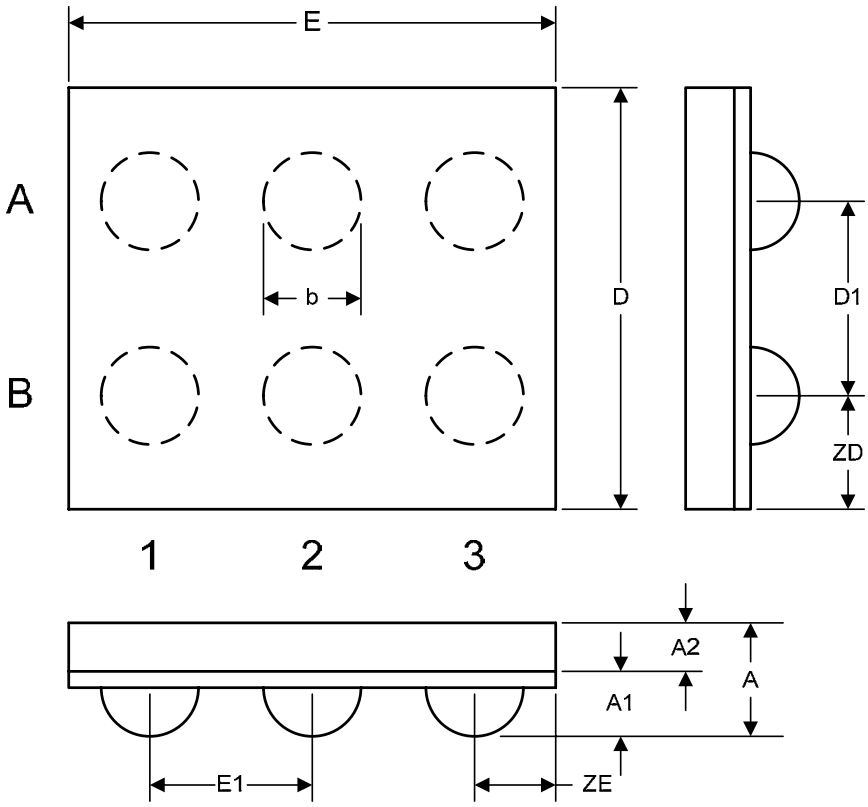
Package Outline : DFN-8





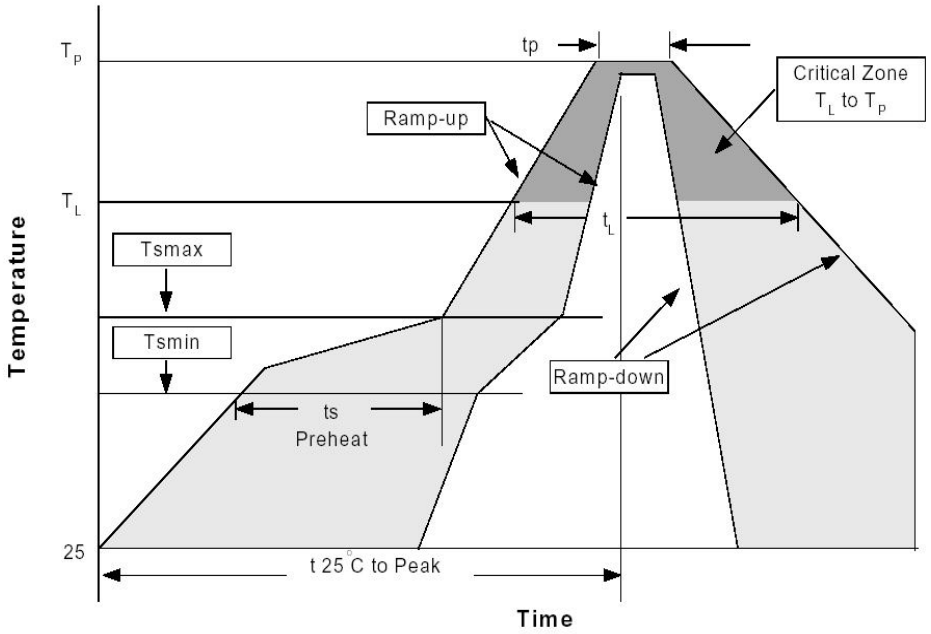
SYMBOL	MILLIMETERS		NOTES
	MIN	MAX	
A	0.75	0.90	-
A3	0.203 BSC.		-
b	0.25	0.35	-
D	3.00 BSC.		-
D1	2.20	2.40	-
E	3.00 BSC.		-
E1	1.40	1.60	-
e	0.65 BSC.		-
L	0.30	0.40	-

Package Outline : WLCSP



SYMBOL	DIMENSION(mm)			NOTES
	MIN	NOM	MAX	
A	0.45	0.5	0.55	
A1	0.09	0.1	0.11	
A2	0.35	0.4	0.45	
b	0.29	0.3	0.31	
E	1.38	1.42	1.46	
D	1.2	1.24	1.28	
D1	0.5			
E1	0.5			
ZD	0.35			
ZE	0.19			

Reflow Profiles



Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly	
	Large Body Pkg. thickness ≥2.5mm or Pkg. volume ≥350mm³	**Small Body Pkg. thickness <2.5mm or Pkg. volume <350mm³**	**Large Body Pkg. thickness ≥2.5mm or Pkg. volume ≥350mm³**	**Small Body Pkg. thickness <2.5mm or Pkg. volume <350mm³**
Average ramp-up rate (T_L to T_P)	3°C/second max.		3°C/second max.	
Preheat -Temperature Min(Tsmin) -Temperature Max (Tsmax) -Time (min to max)(ts)	100°C 150°C 60-120 seconds		150°C 200°C 60-180 seconds	
Tsmax to T_L -Ramp-up Rate			3°C/second max.	
Time maintained above: -Temperature (T_L) -Time (t_L)	183°C 60-150 seconds		217°C 60-150 seconds	
Peak Temperature(T_P)	225+0/-5°C	240+0/-5°C	245+0/-5°C	250+0/-5°C
Time within 5°C of actual Peak Temperature (t_P)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.		6°C/second max.	
Time 25°C to Peak Temperature	6 minutes max.		8 minutes max.	

***All temperatures refer to topside of the package, measured on the package body surface.**