| | | |
|---|---|---|
| $V_{SM}$ | = | 4200 V |
| $I_{TAVM}$ | = | 1920 A |
| $I_{TRMS}$ | = | 3020 A |
| $I_{TSM}$ | = | 32000 A |
| $V_{T0}$ | = | 0.96 V |
| $r_T$ | = | 0.285 mΩ |

# Bi-Directional Control Thyristor

# 5STB 18N4200

Doc. No. 5SYA1040-03 Sep. 01

- **Two thyristors integrated into one wafer**
- **Patented free-floating silicon technology**
- **Designed for traction, energy and industrial applications**
- **Optimum power handling capability**
- **Interdigitated amplifying gate.**

The electrical and thermal data are valid for one thyristor half of the device.

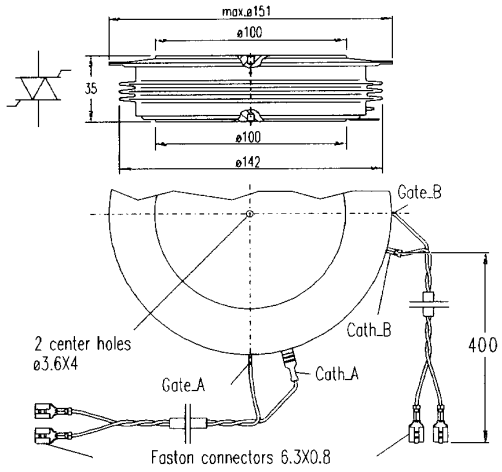
## Blocking

| **Part Number** | **5STB 18N4200** | **5STB 18N4000** | **5STB 18N3600** | Conditions | |
|---|---|---|---|---|---|
| $V_{SM}$ | 4200 V | 4000 V | 3600 V | f = 5 Hz, $t_p$ = 10ms | |
| $V_{RM}$ | 4200 V | 4000 V | 3600 V | f = 50 Hz,$t_p$ = 10ms | |
| $I_{SM}$ | ≤ 400 mA | | | $V_{SM}$ | $T_j$ = 125°C |
| $I_{RM}$ | ≤ 400 mA | | | $V_{RM}$ | |
| $dV/dt_{crit}$ | 1000 V/µs | | @ Exp. to 0.67x$V_{SM}$ | | |

$V_{RM}$ is equal to $V_{SM}$ up to $T_j$ = 110°C

## Mechanical data

| | | | |
|---|---|---|---|
| $F_M$ | Mounting force | nom. | 90 kN |
| | | min. | 81 kN |
| | | max. | 108 kN |
| a | Acceleration<br>Device unclamped<br>Device clamped | | <br>50 m/s$^2$<br>100 m/s$^2$ |
| m | Weight | | 2.9 kg |
| $D_S$ | Surface creepage distance | | 53 mm |
| $D_a$ | Air strike distance | | 22 mm |



## On-state

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $I_{TAVM}$ | Max. average on-state | 1920 A | Half sine wave, $T_C$ = 70°C | | | | |
| $I_{TRMS}$ | Max. RMS on-state current | 3020 A | | | | | |
| $I_{TSM}$ | Max. peak non-repetitive surge current | 32000 A | tp = 10 ms | $T_j$ = 125°C | | | |
| | | 35000 A | tp = 8.3 ms | After surge: | | | |
| $I^2t$ | Limiting load integral | 5120 $kA^2s$ | tp = 10 ms | $V_D = V_R$ = 0V | | | |
| | | 5000 $kA^2s$ | tp = 8.3 ms | | | | |
| $V_T$ | On-state voltage | 1.53 V | $I_T$ = 2000 A | | | | |
| $V_{T0}$ | Threshold voltage | 0.96 V | $I_T$ = 1000 - 3000 A | $T_j$ = 125°C | | | |
| $r_T$ | Slope resistance | 0.285 mΩ | | | | | |
| $I_H$ | Holding current | 50-250 mA | $T_j$ = 25°C | | | | |
| | | 25-150 mA | $T_j$ = 125°C | | | | |
| $I_L$ | Latching current | 100-500 mA | $T_j$ = 25°C | | | | |
| | | 50-300 mA | $T_j$ = 125°C | | | | |

## Switching

| | | | | | |
|---|---|---|---|---|---|
| $di/dt_{crit}$ | Critical rate of rise of on-state current | 250 A/µs | Cont. f = 50 Hz | $V_D \leq 0.67 \cdot V_{DRM}$, $T_j$ = 125°C | |
| | | 500 A/µs | 60 sec. f = 50Hz | $I_{TRM}$ = 3000 A | |
| | | | | $I_{FG}$ = 2 A, $t_r$ = 0.5 µs | |
| $t_d$ | Delay time | ≤ 3.0 µs | $V_D = 0.4 \cdot V_{DRM}$ | $I_{FG}$ = 2 A, $t_r$ = 0.5 µs | |
| $t_q$ | Turn-off time | ≤ 550 µs | $V_D \leq 0.67 \cdot V_{DRM}$ | $I_{TRM}$ = 3000 A, $T_j$ = 125°C | |
| | | | $dv_D/dt$ = 20V/µs | $V_R$ > 200 V, $di_T/dt$ = -1.5 A/µs | |
| $Q_{rr}$ | Recovery charge min | 2100 µAs | | | |
| | max | 3200 µAs | | | |

## Triggering

| | | | | |
|---|---|---|---|---|
| $V_{GT}$ | Gate trigger voltage | ≤ 2.6 V | $T_j$ = 25°C | |
| $I_{GT}$ | Gate trigger current | ≤ 400 mA | $T_j$ = 25°C | |
| $V_{GD}$ | Gate non-trigger voltage | ≥ 0.3 V | $V_D = 0.4 \cdot V_{RM}$ | $T_j$ = 125°C |
| $I_{GD}$ | Gate non-trigger current | ≥ 10 mA | $V_D = 0.4 \cdot V_{RM}$ | $T_j$ = 125°C |
| $V_{FGM}$ | Peak forward gate voltage | 12 V | | |
| $I_{FGM}$ | Peak forward gate current | 10 A | | |
| $V_{RGM}$ | Peak reverse gate voltage | 10 V | | |
| $P_G$ | Maximum gate power loss | 3 W | | |

## Thermal

| | | | |
|---|---|---|---|
| $T_j$ | Operating junction temperature range | -40…125 °C | |
| $T_{stg}$ | Storage temperature range | -40…150 °C | |
| $R_{thJC}$ | Thermal resistance junction to case | 22.8 K/kW | Anode side cooled |
| | | 22.8 K/kW | Cathode side cooled |
| | | 11.4 K/kW | Double side cooled |
| $R_{thCH}$ | Thermal resistance case to heat sink | 4 K/kW | Single side cooled |
| | | 2 K/kW | Double side cooled |

**Analytical function for transient thermal impedance:**

$$Z_{thJC}(t) = \sum_{i=1}^{n} R_i(1 - e^{-t/\tau_i})$$

| i | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| $R_i$(K/kW) | 6.77 | 2.51 | 1.34 | 0.78 |
| $\tau_i$(s) | 0.8651 | 0.1558 | 0.0212 | 0.0075 |

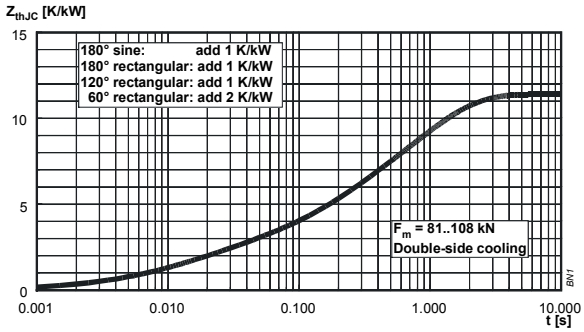



**Fig. 1 Transient thermal impedance junction to case.**

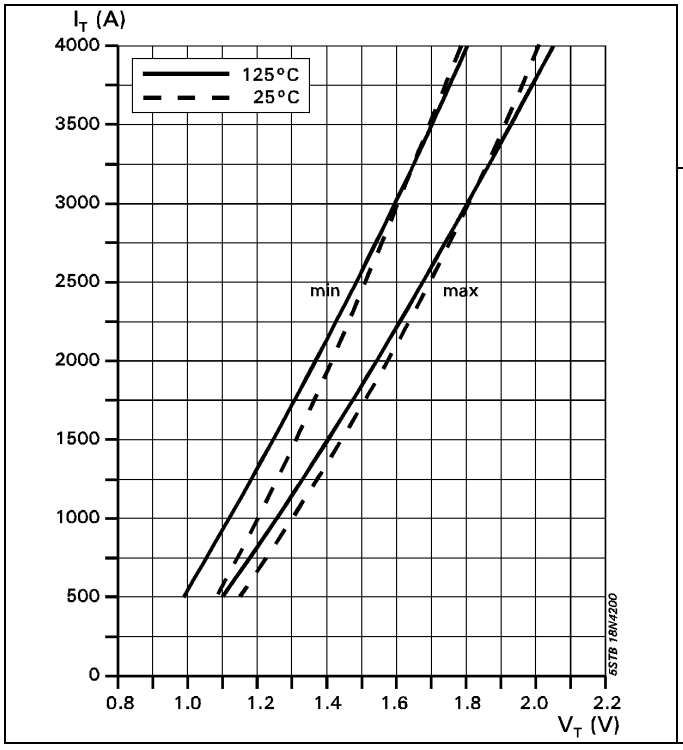



**Fig. 2 On-state characteristics.**

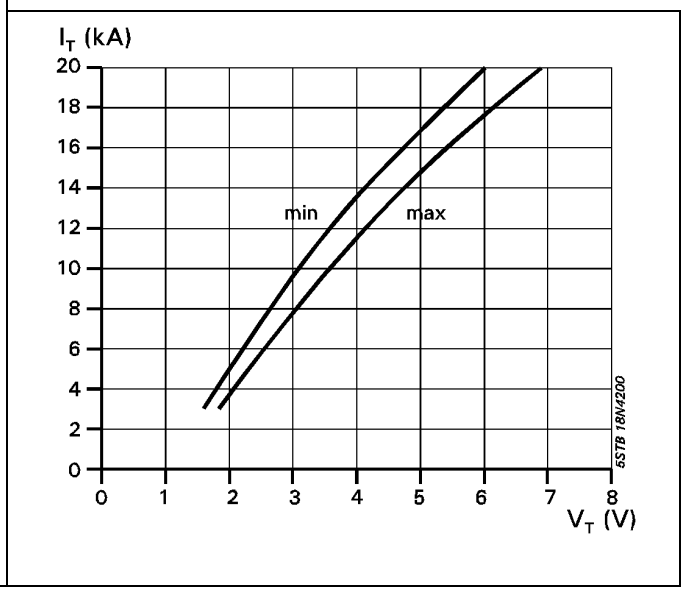



**Fig. 3 On-state characteristics.**

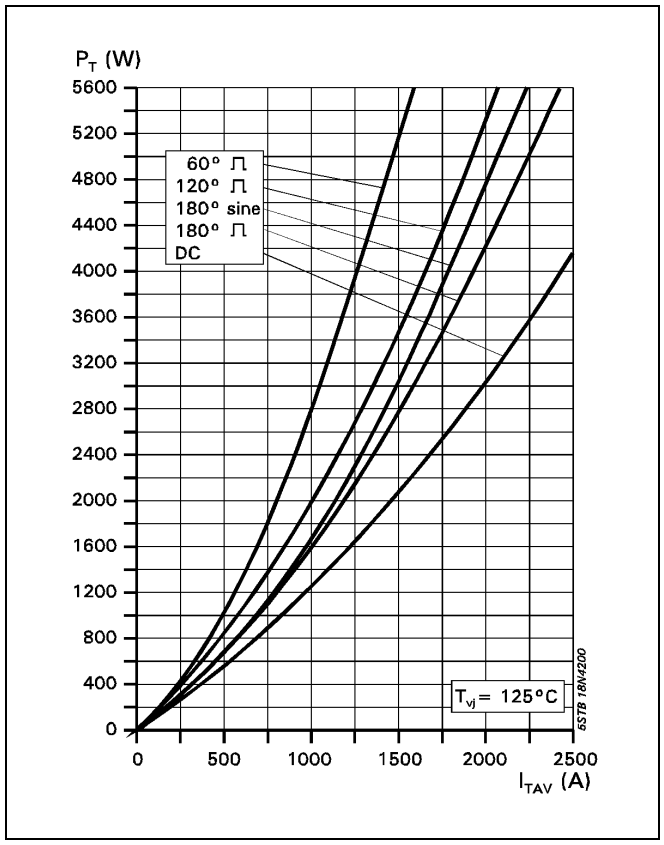



**Fig. 4 On-state power dissipation vs. mean on-state current. Turn - on losses excluded.**

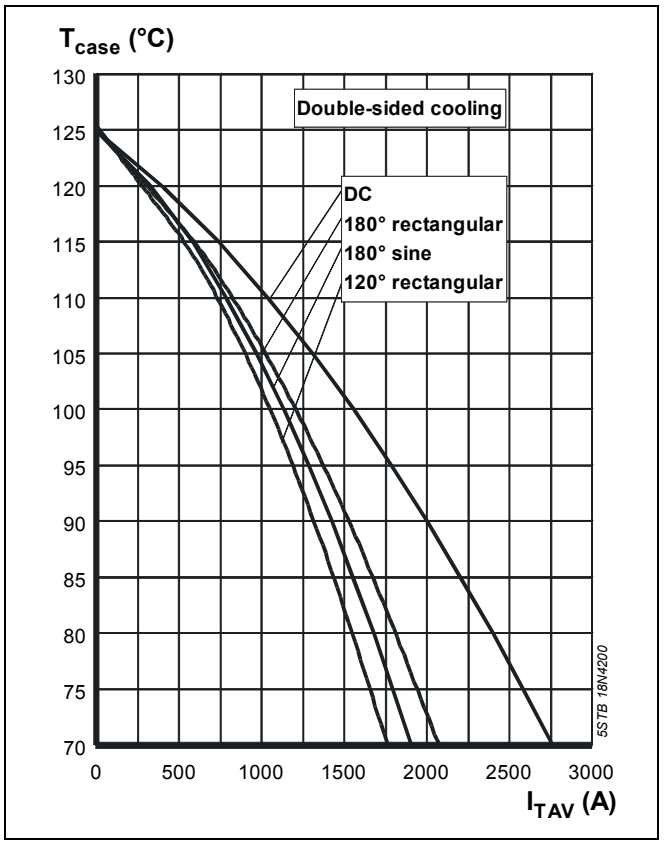



**Fig. 5 Max. permissible case temperature vs. mean on-state current.**

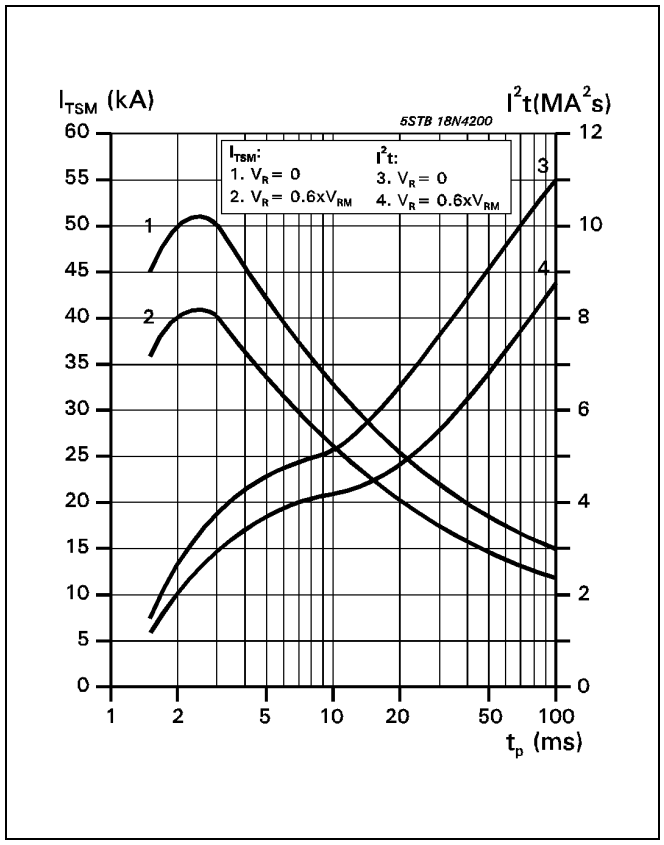



**Fig. 6 Surge on-state current vs. pulse length. Half-sine wave.**

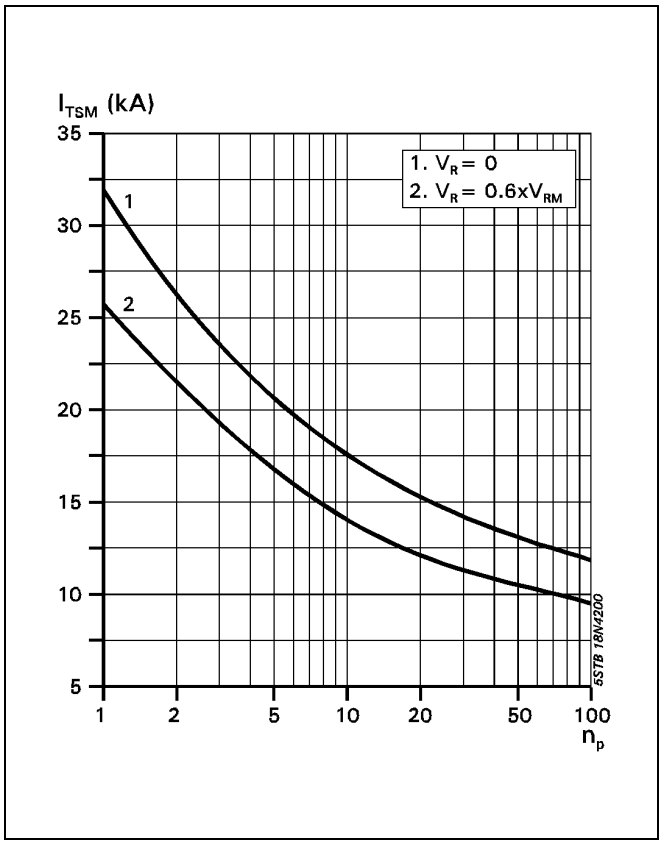



**Fig. 7 Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.**

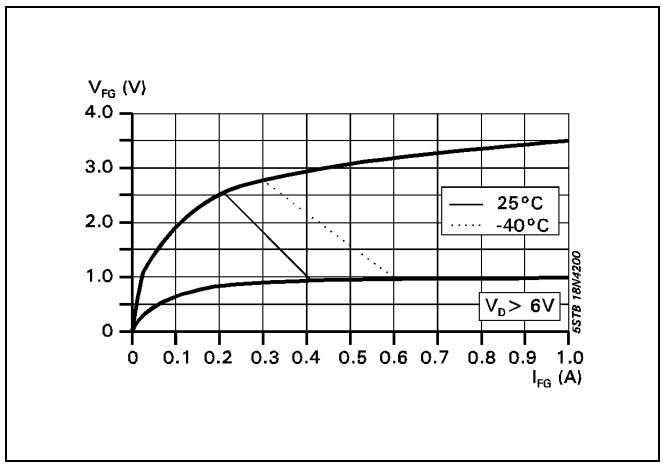



**Fig. 8 Gate trigger characteristics.**

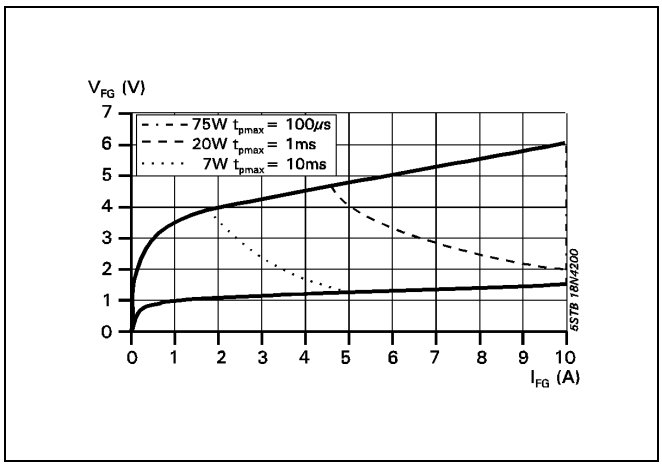



**Fig. 9 Max. peak gate power loss.**

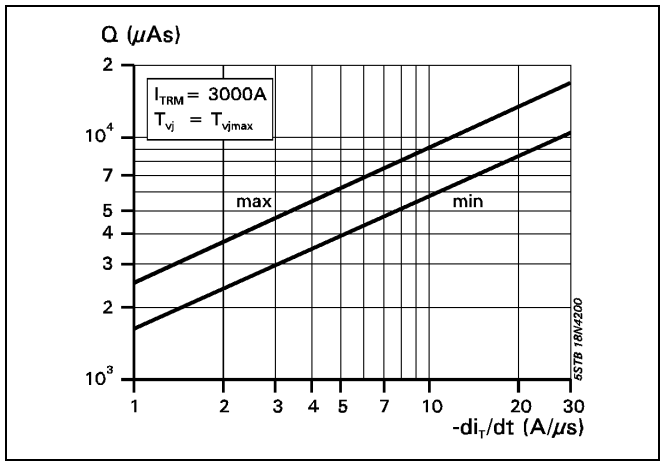



**Fig. 10 Recovery charge vs. decay rate of on-state current.**

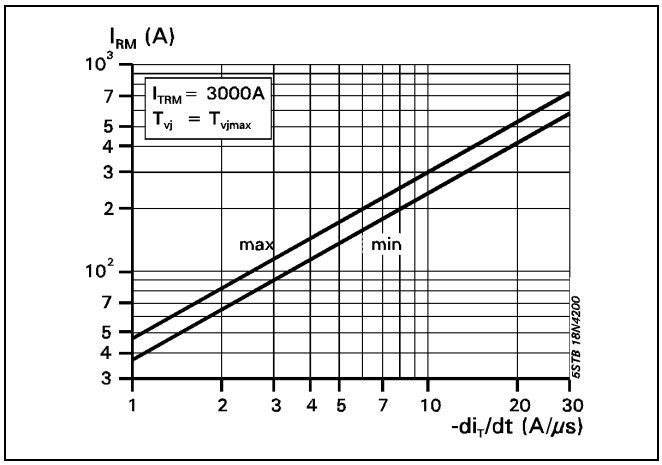



**Fig. 11 Peak reverse recovery current vs. decay rate of on-state current.**



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