To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M35074-XXXSP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DESCRIPTION

The M35074-XXXSP is a character pattern display control IC can display on the digital camera, the digital video, the digital television, the CRT display, the liquid crystal display and the plasma display.

A character color and a character background color can be chosen from 128 kinds of colors per character.

It uses a silicon gate CMOS process and it housed in a 20-pin shrink DIP package (M35074-XXXSP).

For M35074-002SP that is a standard ROM version of M35074-XXXSP respectively, the character pattern is also mentioned.

FEATURES

- Screen composition ..... 24 characters × 12 lines
- Number of characters displayed ..... 288 (Max.)
- Character composition ..... 12 × 18 dot matrix
- Characters available ..... ROM character:511 characters
- Character sizes available ..... 4 (vertical) × 4 (horizontal)
- Display locations available
  - Horizontal direction ..... 4055 locations
  - Vertical direction ..... 2047 locations
- Data input ..... By 24-bit serial input function
  ..... By the I²C-BUS serial input function (At only V_{DD} = 5V)
- Coloring for character
  - Character color ..... 128 colors (Character unit)
  - Background coloring ..... 128 colors (Character unit)
  - Border (shadow) coloring ..... 128 colors (unit of screen / character unit)
  - Raster coloring ..... 128 colors (unit of screen)
- Blanking for character
  - Character size blanking
  - Border size blanking
  - Matrix-outline blanking
  - All blanking (all raster area)
- Output ports
  8 shared output ports (toggled between CO0-CO6 and BLNK output)
- Display oscillation stop function

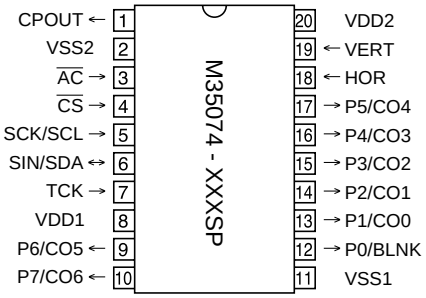
<At V_{DD} = 5V>

- Display input frequency range
  External clock mode 1 ..... Fosc = 6.3 MHz to 80 MHz
  External clock mode 2 ..... Fosc = 20 MHz to 120 MHz
  Internal clock mode ..... Fosc = 20 MH to 120 MHz
- Horizontal synchronous input frequency range
  ..... H.sync = 15 kHz to 130 kHz

<At V_{DD} = 3.3V>

- Display input frequency range
  External clock mode 1 ..... Fosc = 6.3 MHz to 40 MHz
- Horizontal synchronous input frequency range
  ..... H.sync = 15 kHz to 60 kHz

PIN CONFIGURATION (TOP VIEW)



Outline 20P4B

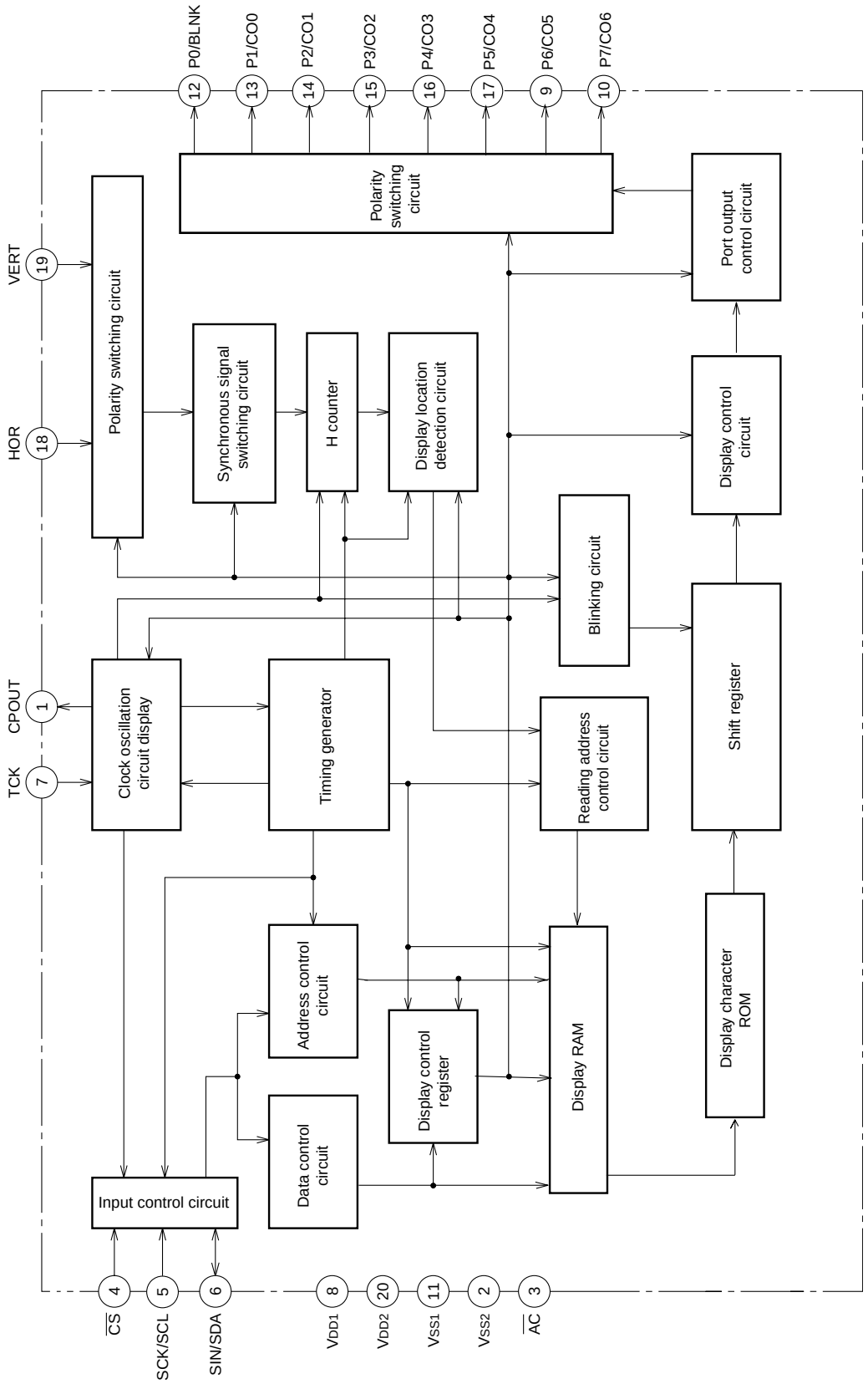
APPLICATION

Digital camera, Digital video, Digital television, CRT display, Liquid crystal display, Plasma display

PIN DESCRIPTION

Symbol	Pin name	Input/ Output	Function
CPOUT	Filter output	Output	Filter output. Connect loop filter to this pin.
V_{SS2}	Earthing pin	–	Connect to GND.
$\overline{AC}$	Auto-clear input	Input	When “L”, this pin resets the internal IC circuit. Hysteresis input. Built-in pull-up resistor.
$\overline{CS}$	Chip select input	Input	<At 24-bit serial communication> This is the pin for chip select. Set to “L” level at serial data transmission. Hysteresis input. Built-in pull-up resistor.
			<At I²C-BUS communication> Connect to “H.”
SCK/SCL	Clock input	Input	<At 24-bit serial communication> SIN pin serial data is taken in when SCK rises at $\overline{CS}$ pin “L” level. Hysteresis input.
			<At I²C-BUS communication> SDA pin serial data is taken in when SCL rises.
SIN/SDA	Data I/O	Input	<At 24-bit serial communication> This is the pin for serial input of display control register and display RAM data. Hysteresis input.
		I/O	<At I²C-BUS communication> Hysteresis input. This is the pin for serial input of display control register and display RAM data. Also, this pin output acknowledge signal.
TCK	External clock input	Input	This is the pin for external clock input.
V_{DD1}	Power pin	–	Digtal power pin. Connect to +5V with the power pin.
P6/CO5	Port P6 output	Output	This pin can be toggled between port pin output and CO5 signal pin.
P7/CO6	Port P7 output	Output	This pin can be toggled between port pin output and CO6 signal pin.
V_{SS1}	Earthing pin	–	Connect to GND using circuit earthing pin.
P0/BLNK	Port P0 output	Output	This pin can be toggled between port pin output and BLNK signal output.
P1/CO0	Port P1 output	Output	This pin can be toggled between port pin output and CO0 signal output.
P2/CO1	Port P2 output	Output	This pin can be toggled between port pin output and CO1 signal output.
P3/CO2	Port P3 output	Output	This pin can be toggled between port pin output and CO2 signal output.
P4/CO3	Port P4 output	Output	This pin can be toggled between port pin output and CO3 signal output.
P5/CO4	Port P5 output	Output	This pin can be toggled between port pin output and CO4 signal output.
HOR	Horizontal synchro-nous signal input	Input	This pin inputs the horizontal synchronous signal. Hysteresis input.
VERT	Vertical synchro-nous signal input	Input	This pin inputs the vertical synchronous signal. Hysteresis input.
V_{DD2}	Power pin	–	Analog power pin. Connect to +5V with the power pin.

BLOCK DIAGRAM



MEMORY CONSTITUTION

Address 000_{16} to $11F_{16}$ are assigned to the display RAM, address 120_{16} to 128_{16} are assigned to the display control registers. The internal circuit is reset and all display control registers (address 120_{16} to 128_{16}) are set to "0" when the $\overline{AC}$ pin level is "L". And then, RAM is not erased and be undefinited. For detail, see "DATA INPUT EXAMPLE". Memory constitution is shown in Figure 1.

Address	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
000_{16}	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	CC6	CC5	CC4	CC3	CC2	CC1	CC0	C8	C7	C6	C5	C4	C3	C2	C1	C0
001_{16}	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	CC6	CC5	CC4	CC3	CC2	CC1	CC0	C8	C7	C6	C5	C4	C3	C2	C1	C0
⋮	⋮	Background color							Character color							Character code								
$11E_{16}$	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	CC6	CC5	CC4	CC3	CC2	CC1	CC0	C8	C7	C6	C5	C4	C3	C2	C1	C0
$11F_{16}$	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	CC6	CC5	CC4	CC3	CC2	CC1	CC0	C8	C7	C6	C5	C4	C3	C2	C1	C0
120_{16}	—	—	—	—	EXCK1	EXCK0	RSEL1	RSEL0	TEST24	DIVS2	DIVS1	DIVS0	DIV11	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0
121_{16}	—	—	—	—	—	—	TEST12	TEST11	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0	PTC7	PTC6	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0
122_{16}	—	VP10	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	HP11	HP10	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
123_{16}	—	—	—	SYAD	BEAT14	—	TEST19	—	—	BLK1	BLK0	BCOL	DSP11	DSP10	DSP9	DSP8	DSP7	DSP6	DSP5	DSP4	DSP3	DSP2	DSP1	DSP0
124_{16}	—	—	—	—	—	—	—	—	LIN17	LIN16	LIN15	LIN14	LIN13	LIN12	LIN11	LIN10	LIN9	LIN8	LIN7	LIN6	LIN5	LIN4	LIN3	LIN2
125_{16}	—	—	—	—	HSZ21	HSZ20	HSZ11	HSZ10	—	—	VSZ2H1	VSZH02	VSZ2L1	VSZ2L0	V18SZ1	V18SZ0	—	—	VSZ1H1	VSZ1H0	VS1L1Z	VSZ1L0	V1SZ1	V1SZ0
126_{16}	—	—	—	—	—	—	—	—	—	FC6	FC5	FC4	FC3	FC2	FC1	FC0	—	RC6	RC5	RC4	RC3	RC2	RC1	RC0
127_{16}	—	—	—	—	—	—	—	—	—	SPACE2	SPACE1	SPACE0	RAMERS	DSPON	TEST30	TEST17	TEST16	TEST15	TEST14	TEST13	POLH	POLV	VMASK	B/$\overline{F}$
128_{16}	—	—	—	—	—	—	—	—	—	—	—	—	TEST20	TEST29	TEST22	TEST21	TEST28	TEST27	TEST26	TEST10	TEST3	TEST2	TEST1	TEST0

Fig.1 Memory constitution (Display RAM, Display Control register)

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM . The screen constitution is shown in Figure 2.

Row / Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	000_{16}	001_{16}	002_{16}	003_{16}	004_{16}	005_{16}	006_{16}	007_{16}	008_{16}	009_{16}	$00A_{16}$	$00B_{16}$	$00C_{16}$	$00D_{16}$	$00E_{16}$	$00F_{16}$	010_{16}	011_{16}	012_{16}	013_{16}	014_{16}	015_{16}	016_{16}	017_{16}
2	018_{16}	019_{16}	$01A_{16}$	$01B_{16}$	$01C_{16}$	$01D_{16}$	$01E_{16}$	$01F_{16}$	020_{16}	021_{16}	022_{16}	023_{16}	024_{16}	025_{16}	026_{16}	027_{16}	028_{16}	029_{16}	$02A_{16}$	$02B_{16}$	$02C_{16}$	$02D_{16}$	$02E_{16}$	$02F_{16}$
3	030_{16}	031_{16}	032_{16}	033_{16}	034_{16}	035_{16}	036_{16}	037_{16}	038_{16}	039_{16}	$03A_{16}$	$03B_{16}$	$03C_{16}$	$03D_{16}$	$03E_{16}$	$03F_{16}$	040_{16}	041_{16}	042_{16}	043_{16}	044_{16}	045_{16}	046_{16}	047_{16}
4	048_{16}	049_{16}	$04A_{16}$	$04B_{16}$	$04C_{16}$	$04D_{16}$	$04E_{16}$	$04F_{16}$	050_{16}	051_{16}	052_{16}	053_{16}	054_{16}	055_{16}	056_{16}	057_{16}	058_{16}	059_{16}	$05A_{16}$	$05B_{16}$	$05C_{16}$	$05D_{16}$	$05E_{16}$	$05F_{16}$
5	060_{16}	061_{16}	062_{16}	063_{16}	064_{16}	065_{16}	066_{16}	067_{16}	068_{16}	069_{16}	$06A_{16}$	$06B_{16}$	$06C_{16}$	$06D_{16}$	$06E_{16}$	$06F_{16}$	070_{16}	071_{16}	072_{16}	073_{16}	074_{16}	075_{16}	076_{16}	077_{16}
6	078_{16}	079_{16}	$07A_{16}$	$07B_{16}$	$07C_{16}$	$07D_{16}$	$07E_{16}$	$07F_{16}$	080_{16}	081_{16}	082_{16}	083_{16}	084_{16}	085_{16}	086_{16}	087_{16}	088_{16}	089_{16}	$08A_{16}$	$08B_{16}$	$08C_{16}$	$08D_{16}$	$08E_{16}$	$08F_{16}$
7	090_{16}	091_{16}	092_{16}	093_{16}	094_{16}	095_{16}	096_{16}	097_{16}	098_{16}	099_{16}	$09A_{16}$	$09B_{16}$	$09C_{16}$	$09D_{16}$	$09E_{16}$	$09F_{16}$	$0A0_{16}$	$0A1_{16}$	$0A2_{16}$	$0A3_{16}$	$0A4_{16}$	$0A5_{16}$	$0A6_{16}$	$0A7_{16}$
8	$0A8_{16}$	$0A9_{16}$	$0AA_{16}$	$0AB_{16}$	$0AC_{16}$	$0AD_{16}$	$0AE_{16}$	$0AF_{16}$	$0B0_{16}$	$0B1_{16}$	$0B2_{16}$	$0B3_{16}$	$0B4_{16}$	$0B5_{16}$	$0B6_{16}$	$0B7_{16}$	$0B8_{16}$	$0B9_{16}$	$0BA_{16}$	$0BB_{16}$	$0BC_{16}$	$0BD_{16}$	$0BE_{16}$	$0BF_{16}$
9	$0C0_{16}$	$0C1_{16}$	$0C2_{16}$	$0C3_{16}$	$0C4_{16}$	$0C5_{16}$	$0C6_{16}$	$0C7_{16}$	$0C8_{16}$	$0C9_{16}$	$0CA_{16}$	$0CB_{16}$	$0CC_{16}$	$0CD_{16}$	$0CE_{16}$	$0CF_{16}$	$0D0_{16}$	$0D1_{16}$	$0D2_{16}$	$0D3_{16}$	$0D4_{16}$	$0D5_{16}$	$0D6_{16}$	$0D7_{16}$
10	$0D8_{16}$	$0D9_{16}$	$0DA_{16}$	$0DB_{16}$	$0DC_{16}$	$0DD_{16}$	$0DE_{16}$	$0DF_{16}$	$0E0_{16}$	$0E1_{16}$	$0E2_{16}$	$0E3_{16}$	$0E4_{16}$	$0E5_{16}$	$0E6_{16}$	$0E7_{16}$	$0E8_{16}$	$0E9_{16}$	$0EA_{16}$	$0EB_{16}$	$0EC_{16}$	$0ED_{16}$	$0EE_{16}$	$0EF_{16}$
11	$0F0_{16}$	$0F1_{16}$	$0F2_{16}$	$0F3_{16}$	$0F4_{16}$	$0F5_{16}$	$0F6_{16}$	$0F7_{16}$	$0F8_{16}$	$0F9_{16}$	$0FA_{16}$	$0FB_{16}$	$0FC_{16}$	$0FD_{16}$	$0FE_{16}$	$0FF_{16}$	100_{16}	101_{16}	102_{16}	103_{16}	104_{16}	105_{16}	106_{16}	107_{16}
12	108_{16}	109_{16}	$10A_{16}$	$10B_{16}$	$10C_{16}$	$10D_{16}$	$10E_{16}$	$10F_{16}$	110_{16}	111_{16}	112_{16}	113_{16}	114_{16}	115_{16}	116_{16}	117_{16}	118_{16}	119_{16}	$11A_{16}$	$11B_{16}$	$11C_{16}$	$11D_{16}$	$11E_{16}$	$11F_{16}$

✻ The hexadecimal numbers in the boxes show the display RAM address.

Fig. 2 Screen constitution

DISPLAY RAM

Address 000_{16} to $11F_{16}$

DA	Register	Contents		Remarks
		Status	Function	
0	C0	0	Sets the displayed ROM character code. Select from 000000000_2–111111111_2 (512 types) and set up a character code.	Display character setting
		1		
1	C1	0		
		1		
2	C2	0		
		1		
3	C3	0		
		1		
4	C4	0		
		1		
5	C5	0		
		1		
6	C6	0		
		1		
7	C7	0		
		1		
8	C8	0		
		1		
9	CC0	0	128 kinds of colors are set up by CC0–CC6. CC0–CC6 correspond to P1/CO0–P7/CO6 output, respectively.	Character color (character unit) setting
		1		
A	CC1	0		
		1		
B	CC2	0		
		1		
C	CC3	0		
		1		
D	CC4	0		
		1		
E	CC5	0		
		1		
F	CC6	0		
		1		
10	BC0	0	128 kinds of colors are set up by BC0–BC6 BC0–BC6 correspond to P1/CO0–P7/CO6 output, respectively.	Character background color (character unit) setting
		1		
11	BC1	0		
		1		
12	BC2	0		
		1		
13	BC3	0		
		1		
14	BC4	0		
		1		
15	BC5	0		
		1		
16	BC6	0		
		1		
17	–	0	Fix to "0".	
		1	Can not be used.	

Note: The display RAM is undefined state at the $\overline{AC}$ pin.

REGISTERS DESCRIPTION

(1) Address 120_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>DIV0</td><td>⓪
1</td><td rowspan="12">Sets division value (multiply value) of horizontal oscillation frequency.

$N1 = \sum_{n=0}^{11} (DIV_n \times 2^n)$

N1 : division value (multiply value)</td><td rowspan="12">Sets display frequency by division value (multiply value) setting.
For detail, see "REGISTER SUPPLEMENTARY DESCRIPTION (1)".

Also, set the display frequency range by registers DIVS0, DIVS1, DIVS2, RSEL0 and RSEL1(address 120_{16}) in accordance with the display frequency.

Any of this settings above is required only when EXCK1 = 0, EXCK0 = 1 and EXCK1 = 1, EXCK0 = 1.</td></tr>
<tr><td>1</td><td>DIV1</td><td>⓪
1</td></tr>
<tr><td>2</td><td>DIV2</td><td>⓪
1</td></tr>
<tr><td>3</td><td>DIV3</td><td>⓪
1</td></tr>
<tr><td>4</td><td>DIV4</td><td>⓪
1</td></tr>
<tr><td>5</td><td>DIV5</td><td>⓪
1</td></tr>
<tr><td>6</td><td>DIV6</td><td>⓪
1</td></tr>
<tr><td>7</td><td>DIV7</td><td>⓪
1</td></tr>
<tr><td>8</td><td>DIV8</td><td>⓪
1</td></tr>
<tr><td>9</td><td>DIV9</td><td>⓪
1</td></tr>
<tr><td>A</td><td>DIV10</td><td>⓪
1</td></tr>
<tr><td>B</td><td>DIV11</td><td>⓪
1</td></tr>
<tr><td>C</td><td>DIVS0</td><td>⓪
1</td><td rowspan="3">For setting, see "REGISTER SUPPLEMENTARY DESCRIPTION (2)".</td><td rowspan="3">Sets display frequency range.</td></tr>
<tr><td>D</td><td>DIVS1</td><td>⓪
1</td></tr>
<tr><td>E</td><td>DIVS2</td><td>⓪
1</td></tr>
<tr><td>F</td><td>TEST24</td><td>⓪</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>10</td><td>RSEL0</td><td>⓪
1</td><td rowspan="2">For setting, see "REGISTER SUPPLEMENTARY DESCRIPTION (2)".</td><td rowspan="2">Sets display frequency range.</td></tr>
<tr><td>11</td><td>RSEL1</td><td>⓪
1</td></tr>
<tr><td>12</td><td>EXCK0</td><td>⓪
1</td><td rowspan="2"><table><tr><th>EXCK1</th><th>EXCK0</th><th>Display clock input</th></tr><tr><td>0</td><td>0</td><td>External clock mode 1</td></tr><tr><td>0</td><td>1</td><td>Internal clock mode</td></tr><tr><td>1</td><td>0</td><td>Can not be used.</td></tr><tr><td>1</td><td>1</td><td>External clock mode 2</td></tr></table></td><td rowspan="2">Display clock setting
See "REGISTER SUPPLEMENTARY DESCRIPTION (1)".</td></tr>
<tr><td>13</td><td>EXCK1</td><td>⓪
1</td></tr>
<tr><td>14</td><td>–</td><td>⓪</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>15</td><td>–</td><td>⓪</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>16</td><td>–</td><td>⓪</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>17</td><td>–</td><td>⓪</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
</table>

Note: The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

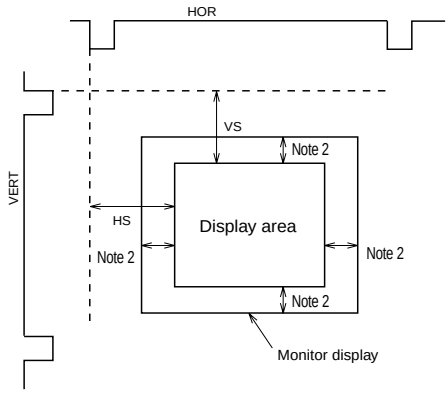
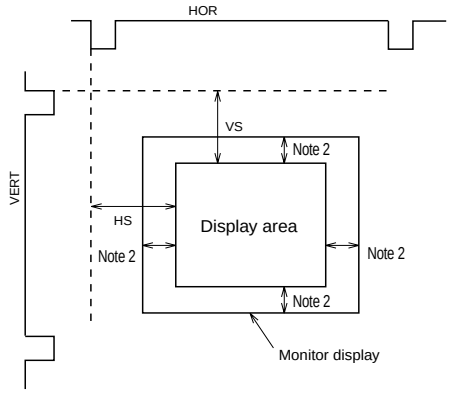
(2) Address 121_{16}

DA	Register	Contents		Remarks
		Status	Function	
0	PTC0	⓪	P0 output (port P0).	P0 pin output control.
		1	BLNK output	
1	PTC1	⓪	P1 output (port P1).	P1 pin output control.
		1	CO0 output	
2	PTC2	⓪	P2 output (port P2).	P2 pin output control.
		1	CO1 output	
3	PTC3	⓪	P3 output (port P3).	P3 pin output control.
		1	CO2 output	
4	PTC4	⓪	P4 output (port P4).	P4 pin output control.
		1	CO3 output	
5	PTC5	⓪	P5 output (port P5).	P5 pin output control.
		1	CO4 output	
6	PTC6	⓪	P6 output (port P6).	P6 pin output control.
		1	CO5 output	
7	PTC7	⓪	P7 output (port P7).	P7 pin output control.
		1	CO6 output	
8	PTD0	⓪	At the port output, it is "L" fixed. At the BLNK signal output, it is negative polarity.	P0 pin data control.
		1	At the port output, it is "L" fixed. At the BLNK signal output, it is negative polarity.	
9	PTD1	⓪	At the port output, it is "L" fixed. At the CO0 signal output, it is negative polarity.	P1 pin data control.
		1	At the port output, it is "L" fixed. At the CO0 signal output, it is negative polarity.	
A	PTD2	⓪	At the port output, it is "L" fixed. At the CO1 signal output, it is negative polarity.	P2 pin data control.
		1	At the port output, it is "L" fixed. At the CO1 signal output, it is negative polarity.	
B	PTD3	⓪	At the port output, it is "L" fixed. At the CO2 signal output, it is negative polarity.	P3 pin data control.
		1	At the port output, it is "L" fixed. At the CO2 signal output, it is negative polarity.	
C	PTD4	⓪	At the port output, it is "L" fixed. At the CO3 signal output, it is negative polarity.	P4 pin data control.
		1	At the port output, it is "L" fixed. At the CO3 signal output, it is negative polarity.	
D	PTD5	⓪	At the port output, it is "L" fixed. At the CO4 signal output, it is negative polarity.	P5 pin data control.
		1	At the port output, it is "L" fixed. At the CO4 signal output, it is negative polarity.	
E	PTD6	⓪	At the port output, it is "L" fixed. At the CO5 signal output, it is negative polarity.	P6 pin data control.
		1	At the port output, it is "L" fixed. At the CO5 signal output, it is negative polarity.	
F	PTD7	⓪	At the port output, it is "L" fixed. At the CO6 signal output, it is negative polarity.	P7 pin data control.
		1	At the port output, it is "L" fixed. At the CO6 signal output, it is negative polarity.	
10	TEST11	⓪	Set it as "0" at the time of the internal clock mode.	
		1	Set it as "0" at the time of the external clock mode1, 2.	
11	TEST12	⓪	Fix to "0".	
		1	Can not be used.	
12	–	⓪	Fix to "0".	
		1	Can not be used.	
13	–	⓪	Fix to "0".	
		1	Can not be used.	
14	–	⓪	Fix to "0".	
		1	Can not be used.	
15	–	⓪	Fix to "0".	
		1	Can not be used.	
16	–	⓪	Fix to "0".	
		1	Can not be used.	
17	–	⓪	Fix to "0".	
		1	Can not be used.	

Note: The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(3) Address 122_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>HP0</td><td>⓪
1</td><td rowspan="12">If HS is the horizontal display start location,
$HS = T \times \left(\sum_{n=0}^{11} 2^n HPn + m \right)$
T: Period of display frequency

4055 settings are possible.
m : offset value differ for the setting of the register EXCK0 and EXCK1. It shown below.
<table><tr><td>EXCK1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>EXCK0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>m</td><td>13</td><td>13</td><td>Do not set</td><td>19</td></tr></table>  </td><td rowspan="12">Horizontal display start location is specified using the 12 bits from HP11 to HP0.
HP11 to HP0 = (000000000000_2) and (000000100111_2) setting is forbidden.</td></tr>
<tr><td>1</td><td>HP1</td><td>⓪
1</td></tr>
<tr><td>2</td><td>HP2</td><td>⓪
1</td></tr>
<tr><td>3</td><td>HP3</td><td>⓪
1</td></tr>
<tr><td>4</td><td>HP4</td><td>⓪
1</td></tr>
<tr><td>5</td><td>HP5</td><td>⓪
1</td></tr>
<tr><td>6</td><td>HP6</td><td>⓪
1</td></tr>
<tr><td>7</td><td>HP7</td><td>⓪
1</td></tr>
<tr><td>8</td><td>HP8</td><td>⓪
1</td></tr>
<tr><td>9</td><td>HP9</td><td>⓪
1</td></tr>
<tr><td>A</td><td>HP10</td><td>⓪
1</td></tr>
<tr><td>B</td><td>HP11</td><td>⓪
1</td></tr>
<tr><td>C</td><td>VP0</td><td>⓪
1</td><td rowspan="12">If VS is the vertical display start location,
$VS = H \times \sum_{n=0}^{10} 2^n VPn$
H : Cycle with the horizonal synchronizing pulse
2047 settings are possible.
  </td><td rowspan="12">The vertical start location is specified using the 11 bits from VP10 to VP0.
VP10 to VP0 = (00000000000_2) setting is forbidden.

HS*(shown left) shows horizontal display start location this is register B/$\overline{F}$ (address 127_{16}) = "0" is set.</td></tr>
<tr><td>D</td><td>VP1</td><td>⓪
1</td></tr>
<tr><td>E</td><td>VP2</td><td>⓪
1</td></tr>
<tr><td>F</td><td>VP3</td><td>⓪
1</td></tr>
<tr><td>10</td><td>VP4</td><td>⓪
1</td></tr>
<tr><td>11</td><td>VP5</td><td>⓪
1</td></tr>
<tr><td>12</td><td>VP6</td><td>⓪
1</td></tr>
<tr><td>13</td><td>VP7</td><td>⓪
1</td></tr>
<tr><td>14</td><td>VP8</td><td>⓪
1</td></tr>
<tr><td>15</td><td>VP9</td><td>⓪
1</td></tr>
<tr><td>16</td><td>VP10</td><td>⓪
1</td></tr>
<tr><td>17</td><td>–</td><td>⓪</td><td>Fix to "0".</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td><td></td></tr>
</table>

Note 1: The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.
2: Set up the horizontal and vertical display start location so that display range may not exceed it.
Set the character code "$1FF_{16}$" (blank without background) for the display RAM of the part which the display range exceeds.

(4) Address 123_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>DSP0</td><td>⓪
1</td><td rowspan="12">The display modes of display screen inside n+1 line by DSPn (n=0 to 11)

The display mode decided by the combination with registers BLK1 and BLK0 (address 123_{16}).
Settings are given below.
<table><tr><th>BLK1</th><th>BLK0</th><th>DSPn="0"</th><th>DSPn="1"</th></tr><tr><td>0</td><td>0</td><td>Matrix-outline border</td><td>Matrix-outline</td></tr><tr><td>0</td><td>1</td><td>Character</td><td>Border</td></tr><tr><td>1</td><td>0</td><td>Border</td><td>Matrix-outline</td></tr><tr><td>1</td><td>1</td><td>Matrix-outline</td><td>Charcter</td></tr></table>(At register BCOL="0")

For detail, see "DISPLAY FORM 1 (1)".</td><td>Display mode settting of line 1.</td></tr>
<tr><td>1</td><td>DSP1</td><td>⓪
1</td><td>Display mode settting of line 2.</td></tr>
<tr><td>2</td><td>DSP2</td><td>⓪
1</td><td>Display mode settting of line 3.</td></tr>
<tr><td>3</td><td>DSP3</td><td>⓪
1</td><td>Display mode settting of line 4.</td></tr>
<tr><td>4</td><td>DSP4</td><td>⓪
1</td><td>Display mode settting of line 5.</td></tr>
<tr><td>5</td><td>DSP5</td><td>⓪
1</td><td>Display mode settting of line 6.</td></tr>
<tr><td>6</td><td>DSP6</td><td>⓪
1</td><td>Display mode settting of line 7.</td></tr>
<tr><td>7</td><td>DSP7</td><td>⓪
1</td><td>Display mode settting of line 8.</td></tr>
<tr><td>8</td><td>DSP8</td><td>⓪
1</td><td>Display mode settting of line 9.</td></tr>
<tr><td>9</td><td>DSP9</td><td>⓪
1</td><td>Display mode settting of line 10.</td></tr>
<tr><td>A</td><td>DSP10</td><td>⓪
1</td><td>Display mode settting of line 11.</td></tr>
<tr><td>B</td><td>DSP11</td><td>⓪
1</td><td>Display mode settting of line 12.</td></tr>
<tr><td>C</td><td>BCOL</td><td>⓪
1</td><td>The blanking of BLK1 and BLK0
Sets all blanking (raster area)</td><td>All blanking (raster area) settting</td></tr>
<tr><td>D</td><td>BLK0</td><td>⓪
1</td><td rowspan="2"><table><tr><th>BLK1</th><th>BLK0</th><th>Blanking mode</th></tr><tr><td>0</td><td>0</td><td>Matrix-outline size</td></tr><tr><td>0</td><td>1</td><td>Character size</td></tr><tr><td>1</td><td>0</td><td>Border size</td></tr><tr><td>1</td><td>1</td><td>Matrix-outline size</td></tr></table></td><td rowspan="2">Display mode (blanking mode) settting
See "DISPLAY FORM 1 (1)".</td></tr>
<tr><td>E</td><td>BLK1</td><td>⓪
1</td></tr>
<tr><td>F</td><td>—</td><td>⓪
1</td><td>Fix to "0".
Can not be used.</td><td></td></tr>
<tr><td>10</td><td>—</td><td>⓪
1</td><td>Fix to "0".
Can not be used.</td><td></td></tr>
<tr><td>11</td><td>TEST19</td><td>⓪
1</td><td>Fix to "0".
Can not be used.</td><td></td></tr>
<tr><td>12</td><td>—</td><td>⓪
1</td><td>Fix to "0".
Can not be used.</td><td></td></tr>
<tr><td>13</td><td>BETA14</td><td>⓪
1</td><td>Matrix-outline display (12 × 18 dot)
Matrix-outline display (14 × 18 dot)</td><td>Effective at the time of Matrix-outline displays and Matrix-outline border displays in the display mode.</td></tr>
<tr><td>14</td><td>SYAD</td><td>⓪
1</td><td>Border display of character
Shadow display of character</td><td></td></tr>
<tr><td>15</td><td>—</td><td>⓪
1</td><td>Fix to "0".
Can not be used.</td><td></td></tr>
<tr><td>16</td><td>—</td><td>⓪
1</td><td>Fix to "0".
Can not be used.</td><td></td></tr>
<tr><td>17</td><td>—</td><td>⓪
1</td><td>Fix to "0".
Can not be used.</td><td></td></tr>
</table>

Note: The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(5) Address 124_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>LINE2</td><td>⓪
1</td><td rowspan="18">The vertical dot size for line n in the character dot lines (18 vertical lines) is set using LINn (n = 2 to 17).

Dot size can be selected between 2 types for each dot line.

For dot size, see the below registers. Line 1 and lines 2 to 2 can be set independent of one another.

<table><tr><th></th><th>LINn = "0"</th><th>LINn = "1"</th></tr><tr><td>1st line</td><td>Refer to VSZ1L0 and VSZ1L1</td><td>Refer to VSZ1H0 and VSZ1H1</td></tr><tr><td>2nd to 12th line</td><td>Refer to VSZ2L0 and VSZ2L1</td><td>Refer to VSZ2H0 and VSZ2H1</td></tr></table></td><td>Character dot size setting in the vertical direction for the 2nd line.</td></tr>
<tr><td>1</td><td>LINE3</td><td>⓪
1</td><td>Character dot size setting in the vertical direction for the 3rd line.</td></tr>
<tr><td>2</td><td>LINE4</td><td>⓪
1</td><td>Character dot size setting in the vertical direction for the 4th line.</td></tr>
<tr><td>3</td><td>LINE5</td><td>⓪
1</td><td>Character dot size setting in the vertical direction for the 5th line.</td></tr>
<tr><td>4</td><td>LINE6</td><td>⓪
1</td><td>Character dot size setting in the vertical direction for the 6th line.</td></tr>
<tr><td>5</td><td>LINE7</td><td>⓪
1</td><td>Character dot size setting in the vertical direction for the 7th line.</td></tr>
<tr><td>6</td><td>LINE8</td><td>⓪
1</td><td>Character dot size setting in the vertical direction for the 8th line.</td></tr>
<tr><td>7</td><td>LINE9</td><td>⓪
1</td><td>Character dot size setting in the vertical direction for the 9th line.</td></tr>
<tr><td>8</td><td>LINE10</td><td>⓪
1</td><td>Character dot size setting in the vertical direction for the 10th line.</td></tr>
<tr><td>9</td><td>LINE11</td><td>⓪
1</td><td>Character dot size setting in the vertical direction for the 11th line.</td></tr>
<tr><td>A</td><td>LINE12</td><td>⓪
1</td><td>Character dot size setting in the vertical direction for the 12th line.</td></tr>
<tr><td>B</td><td>LINE13</td><td>⓪
1</td><td>Character dot size setting in the vertical direction for the 13th line.</td></tr>
<tr><td>C</td><td>LINE14</td><td>⓪
1</td><td>Character dot size setting in the vertical direction for the 14th line.</td></tr>
<tr><td>D</td><td>LINE15</td><td>⓪
1</td><td>Character dot size setting in the vertical direction for the 15th line.</td></tr>
<tr><td>E</td><td>LINE16</td><td>⓪
1</td><td>Character dot size setting in the vertical direction for the 16th line.</td></tr>
<tr><td>F</td><td>LINE17</td><td>⓪
1</td><td>Character dot size setting in the vertical direction for the 17th line.</td></tr>
<tr><td>10</td><td>—</td><td>⓪
1</td><td>Fix to "0".
Can not be used.</td><td></td></tr>
<tr><td>11</td><td>—</td><td>⓪
1</td><td>Fix to "0".
Can not be used.</td><td></td></tr>
<tr><td>12</td><td>—</td><td>⓪
1</td><td>Fix to "0".
Can not be used.</td><td></td></tr>
<tr><td>13</td><td>—</td><td>⓪
1</td><td>Fix to "0".
Can not be used.</td><td></td></tr>
<tr><td>14</td><td>—</td><td>⓪
1</td><td>Fix to "0".
Can not be used.</td><td></td></tr>
<tr><td>15</td><td>—</td><td>⓪
1</td><td>Fix to "0".
Can not be used.</td><td></td></tr>
<tr><td>16</td><td>—</td><td>⓪
1</td><td>Fix to "0".
Can not be used.</td><td></td></tr>
<tr><td>17</td><td>—</td><td>⓪
1</td><td>Fix to "0".
Can not be used.</td><td></td></tr>
</table>

Note: The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(6) Address 125$_{16}$

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>V1SZ0</td><td>Ⓞ
1</td><td>H: Cycle with the horizontal synchronizing pulse
<table><tr><th>V1SZ1</th><th>V1SZ0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character dot size setting in the vertical direction for the 1st line.
(common to all lines)</td></tr>
<tr><td>1</td><td>V1SZ1</td><td>Ⓞ
1</td></tr>
<tr><td>2</td><td>VSZ1L0</td><td>Ⓞ
1</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ1L1</th><th>VSZ1L0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character dot size setting in the vertical direction for the first line.
(effective only at LINn = "0").</td></tr>
<tr><td>3</td><td>VSZ1L1</td><td>Ⓞ
1</td></tr>
<tr><td>4</td><td>VSZ1H0</td><td>Ⓞ
1</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ1H1</th><th>VSZ1H0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character dot size setting in the vertical direction for the first line.
(effective only at LINn = "1").</td></tr>
<tr><td>5</td><td>VSZ1H1</td><td>Ⓞ
1</td></tr>
<tr><td>6</td><td>–</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>7</td><td>–</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>8</td><td>V18SZ0</td><td>Ⓞ
1</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>V18Z1</th><th>V18Z0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character dot size setting in the vertical direction for the 18th line.
(common to all lines)</td></tr>
<tr><td>9</td><td>V18SZ1</td><td>Ⓞ
1</td></tr>
<tr><td>A</td><td>VSZ2L0</td><td>Ⓞ
1</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ2L1</th><th>VSZ2L0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character dot size setting in the vertical direction (display monitor for 2nd to 12th line)
(effective only at LINn = "0").</td></tr>
<tr><td>B</td><td>VSZ2L1</td><td>Ⓞ
1</td></tr>
<tr><td>C</td><td>VSZ2H0</td><td>Ⓞ
1</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ2H1</th><th>VSZ2H0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character dot size setting in the vertical direction (display monitor for 2nd to 12th line)
(effective only at LINn = "0").</td></tr>
<tr><td>D</td><td>VSZ2H1</td><td>Ⓞ
1</td></tr>
<tr><td>E</td><td>–</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>F</td><td>–</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>10</td><td>HSZ10</td><td>Ⓞ
1</td><td rowspan="2"><table><tr><th>HSZ11</th><th>HSZ10</th><th>horizontal direction size</th></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr><tr><td>0</td><td>1</td><td>2T/dot</td></tr><tr><td>1</td><td>0</td><td>3T/dot</td></tr><tr><td>1</td><td>1</td><td>4T/dot</td></tr></table></td><td rowspan="2">Character size setting in the horizontal direction for the first line.
T: Display frequency cycle.</td></tr>
<tr><td>11</td><td>HSZ11</td><td>Ⓞ
1</td></tr>
<tr><td>12</td><td>HSZ20</td><td>Ⓞ
1</td><td rowspan="2"><table><tr><th>HSZ21</th><th>HSZ20</th><th>horizontal direction size</th></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr><tr><td>0</td><td>1</td><td>2T/dot</td></tr><tr><td>1</td><td>0</td><td>3T/dot</td></tr><tr><td>1</td><td>1</td><td>4T/dot</td></tr></table></td><td rowspan="2">Charcter size setting in the horizontal direction for the 2nd line to 12th line.
T: Display frequency cycle.</td></tr>
<tr><td>13</td><td>HSZ21</td><td>Ⓞ
1</td></tr>
<tr><td>14</td><td>–</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>15</td><td>–</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>16</td><td>–</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>17</td><td>–</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
</table>

Note: The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(7) Address 126_{16}

DA	Register	Contents		Remarks
		Status	Function	
0	RC0	⓪	RO0–RO6 correspond to CO0–CO6 output, respectively.	Raster color setting of all blankings.
		1		
1	RC1	⓪		
		1		
2	RC2	⓪		
		1		
3	RC3	⓪		
		1		
4	RC4	⓪		
		1		
5	RC5	⓪		
		1		
6	RC6	⓪		
		1		
7	–	⓪	Fix to "0".	
		1	Can not be used.	
8	–	⓪	Fix to "0".	
		1	Can not be used.	
9	FC0	⓪	FO0–FO6 correspond to CO0–CO6 output, respectively.	Color setting of the border display or the shadow display.
		1		
A	FC1	⓪		
		1		
B	FC2	⓪		
		1		
C	FC3	⓪		
		1		
D	FC4	⓪		
		1		
E	FC5	⓪		
		1		
F	FC6	⓪		
		1		
10	–	⓪	Fix to "0".	
		1	Can not be used.	
11	–	⓪	Fix to "0".	
		1	Can not be used.	
12	–	⓪	Fix to "0".	
		1	Can not be used.	
13	–	⓪	Fix to "0".	
		1	Can not be used.	
14	–	⓪	Fix to "0".	
		1	Can not be used.	
15	–	⓪	Fix to "0".	
		1	Can not be used.	
16	–	⓪	Fix to "0".	
		1	Can not be used.	
17		⓪	Fix to "0".	
		1	Can not be used.	

Note: The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(8) Address 127_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">B/$\overline{F}$</td><td>Ⓞ</td><td>Synchronize with the leading edge of horizontal synchronization.</td><td rowspan="2">Synchronize with the front porch or back porch of the horizontal synchronization signal.</td></tr>
<tr><td>1</td><td>Synchronize with the trailing edge of horizontal synchronization.</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">VMASK</td><td>Ⓞ</td><td>Do not mask by VERT input signal.</td><td rowspan="2">Sets mask at phase comparison operating.</td></tr>
<tr><td>1</td><td>Mask by VERT input signal.</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">POLV</td><td>Ⓞ</td><td>VERT pin is negative polarity.</td><td rowspan="2">VERT pin polarity setting.</td></tr>
<tr><td>1</td><td>VERT pin is positive polarity.</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">POLH</td><td>Ⓞ</td><td>HOR pin is negative polarity.</td><td rowspan="2">HOR pin polarity setting.</td></tr>
<tr><td>1</td><td>HOR pin is positive polarity.</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">TEST13</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">TEST14</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">TEST15</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">TEST16</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">TEST17</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">TEST30</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">DSPON</td><td>Ⓞ</td><td>Display OFF</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Display ON</td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">RAMERS</td><td>Ⓞ</td><td>RAM not erased</td><td rowspan="2">When register RAMERS is set to "1", do not stop the display clock. There is no need to reset because there is no register for this bit.</td></tr>
<tr><td>1</td><td>RAM erased</td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">SPACE0</td><td>Ⓞ</td><td rowspan="6"><table><tr><th>SPACE2</th><th>SPACE1</th><th>SPACE0</th><th>Number of Lines and Space<(S) represents space></th></tr><tr><td>0</td><td>0</td><td>0</td><td>12</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1 (S) 10 (S) 1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>2 (S) 8 (S) 2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>3 (S) 6 (S) 3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>4 (S) 4 (S) 4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>5 (S) 2 (S) 5</td></tr><tr><td>1</td><td>1</td><td>0</td><td>6 (S) 6</td></tr><tr><td>1</td><td>1</td><td>1</td><td>6 (S)(S) 6</td></tr></table>(S) represents one line worth of space</td><td rowspan="6">Leave one line worth of space in the vertical direction.
For example, 6 (S) 6 indicates two sets of 6 lines with a line of spaces between lines 6 and 7.
A line is 18 × N horizontal scan lines.
N is determined by the character size in the vertical direction</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">D</td><td rowspan="2">SPACE1</td><td>Ⓞ</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">E</td><td rowspan="2">SPACE2</td><td>Ⓞ</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">F</td><td rowspan="2">–</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">10</td><td rowspan="2">–</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">11</td><td rowspan="2">–</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">12</td><td rowspan="2">–</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">13</td><td rowspan="2">–</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">14</td><td rowspan="2">–</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">15</td><td rowspan="2">–</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">16</td><td rowspan="2">–</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">17</td><td rowspan="2">–</td><td>Ⓞ</td><td>Fix to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
</table>

Note: The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(9) Address 128_{16}

DA	Register	Contents		Remarks
		Status	Function	
0	TEST0	⓪	Fix to "0".	
		1	Can not be used.	
1	TEST1	⓪	Fix to "0".	
		1	Can not be used.	
2	TEST2	⓪	Fix to "0".	
		1	Can not be used.	
3	TEST3	⓪	Fix to "0".	
		1	Can not be used.	
4	TEST10	⓪	Fix to "0".	
		1	Can not be used.	
5	TEST26	⓪	Fix to "0".	
		1	Can not be used.	
6	TEST27	⓪	Fix to "0".	
		1	Can not be used.	
7	TEST28	⓪	Fix to "0".	
		1	Can not be used.	
8	TEST21	⓪	Fix to "0".	
		1	Can not be used.	
9	TEST22	⓪	Fix to "0".	
		1	Can not be used.	
A	TEST29	⓪	Fix to "0".	
		1	Can not be used.	
B	TEST20	⓪	Fix to "0".	
		1	Can not be used.	
C	—	⓪	Fix to "0".	
		1	Can not be used.	
D	—	⓪	Fix to "0".	
		1	Can not be used.	
E	—	⓪	Fix to "0".	
		1	Can not be used.	
F	—	⓪	Fix to "0".	
		1	Can not be used.	
10	—	⓪	Fix to "0".	
		1	Can not be used.	
11	—	⓪	Fix to "0".	
		1	Can not be used.	
12	—	⓪	Fix to "0".	
		1	Can not be used.	
13	—	⓪	Fix to "0".	
		1	Can not be used.	
14	—	⓪	Fix to "0".	
		1	Can not be used.	
15	—	⓪	Fix to "0".	
		1	Can not be used.	
16	—	⓪	Fix to "0".	
		1	Can not be used.	
17	—	⓪	Fix to "0".	
		1	Can not be used.	

Note: The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

REGISTER SUPPLEMENTARY DESCRIPTION

(1) Setting external clock input and display frequency mode Setting external clock input and display frequency mode (by use of EXCK0, EXCK1 and DIV11 to DIV0 (120_{16}), as explained here following.

(a) When (EXCK1, EXCK0) = (0, 0) ..... External clock mode 1
Fosc = 6.3 to 80 MHz (VDD = 4.75V to 5.25V)
Fosc = 6.3 to 40 MHz (VDD = 3.00V to 3.60V)
Input from the TCK pin a constant-period continuous external clock that synchronizes with the horizontal synchronous signal. And input from HOR pin a constant period continuous horizontal synchronous signal.
Never stop inputting the clock while displaying.
Do not have to set a display frequency because the clock just as it is entered from outside is used as the display clock.

(b) When (EXCK1, EXCK0) = (0, 1) .....Internal clock mode
Fosc = 20 to 120 MHz (VDD = 4.75V to 5.25V)
Clock input from the TCK pin is unnecessary. The multiply clock of the internally generated horizontal synchronous signal is used as the display clock.
The display frequency is set by setting the multiply value of the horizontal synchronous frequency (of the display frequency) in DIV11 to DIV0 (address 120_{16}). Also, set the display frequency range. (See the next page.)
Display frequency is calculated using the below expression.

Display frequency = Horizontal synchronous frequency × Multiply value

(c) When (EXCK1, EXCK0) = (1, 0) ..... Setting disabled

(d) When (EXCK1, EXCK0) = (1, 1) ..... External clock mode 2
Fosc = 20 to 120 MHz (VDD = 4.75V to 5.25V)
Input from the TCK pin a constant-period continuous external clock that synchronizes with the horizontal synchronous signal. And input from HOR pin a constant-period continuous horizontal synchronous signal.
Never stop inputting the clock while displaying.
An internal clock which is in sync with the external input clock is used as the display clock.
Because the display frequency equals the external clock frequency, set N1 (division value) that satisfies the below expressions to DIV11 to DIV0 (address 120_{16}) for make the display frequency is equal to the external clock frequency.

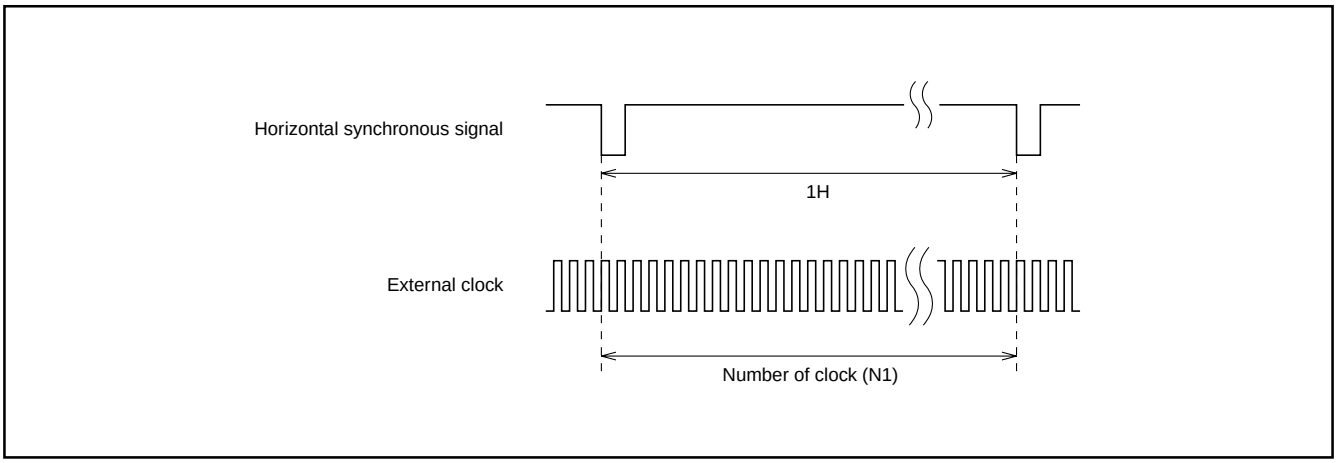


Fig. 3 Example of external clock input

(2) To set display frequency range

Whenever setting display frequency (when EXCK1 = "0", EXCK0 = "1", or EXCK1 = "1", EXCK0 = "1"), always set the display frequency range in accordance with the display frequency. This range is set from DIVS0, DIVS1, DIVS2, RSEL0 and RSEL1 (address 120_{16}). Frequency ranges are given here below.

RSEL1	RSEL0	DIVS2	DIVS1	DIVS0	Display frequency range MHz
1	1	0	0	0	112.0 to 120.0
1	0	0	0	0	104.0 to 112.0
0	1	0	0	0	93.0 to 104.0
0	0	0	0	0	80.0 to 93.0
1	1	0	0	1	75.0 to 80.0
1	0	0	0	1	69.5 to 75.0
0	1	0	0	1	62.0 to 69.5
0	0	0	0	1	55.0 to 62.0
1	1	0	1	0	—
1	0	0	1	0	52.0 to 55.0
0	1	0	1	0	46.5 to 52.0
0	0	0	1	0	40.0 to 46.5
1	1	0	1	1	37.5 to 40.0
1	0	0	1	1	35.0 to 37.5
0	1	0	1	1	31.0 to 35.0
0	0	0	1	1	27.5 to 31.0
1	1	1	0	0	—
1	0	1	0	0	26.0 to 27.5
0	1	1	0	0	23.5 to 26.0
0	0	1	0	0	20.0 to 23.5

(3) Notes on setting display frequency

To change external clock (display) frequency or horizontal synchronization frequency, always use the following procedures.

To set EXCK1 = "0", EXCK0 = "1"

(a) Turn the display OFF. … DSPON (address 127_{16}) = "0"
(b) Set the display frequency. … Set from DIV11 to DIV0, DIVS0, DIVS1, DIVS2, RSEL0 and RSEL1 (address 120_{16}).
(c) Wait 20 ms while the horizontal synchronization signal is being input.
(d) Turn the display ON. … DSPON (address 127_{16}) = "1"

To set EXCK1 = "1", EXCK0 = "1"

(a) Turn the display OFF. … DSPON (address 127_{16}) = "0"
(b) Set the display frequency. … Set from DIV11 to DIV0, DIVS0, DIVS1, DIVS2, RSEL0 and RSEL1 (address 120_{16}).
(c) Wait 20 ms while the horizontal synchronization signal and external clock are being input.
(d) Turn the display ON. … DSPON (address 127_{16}) = "1"

DISPLAY FORM 1

(1) blanking mode

Character size

: Blanking same as the character size.

Border size

: Blanking the background as a size from character.

Matrix-outline size

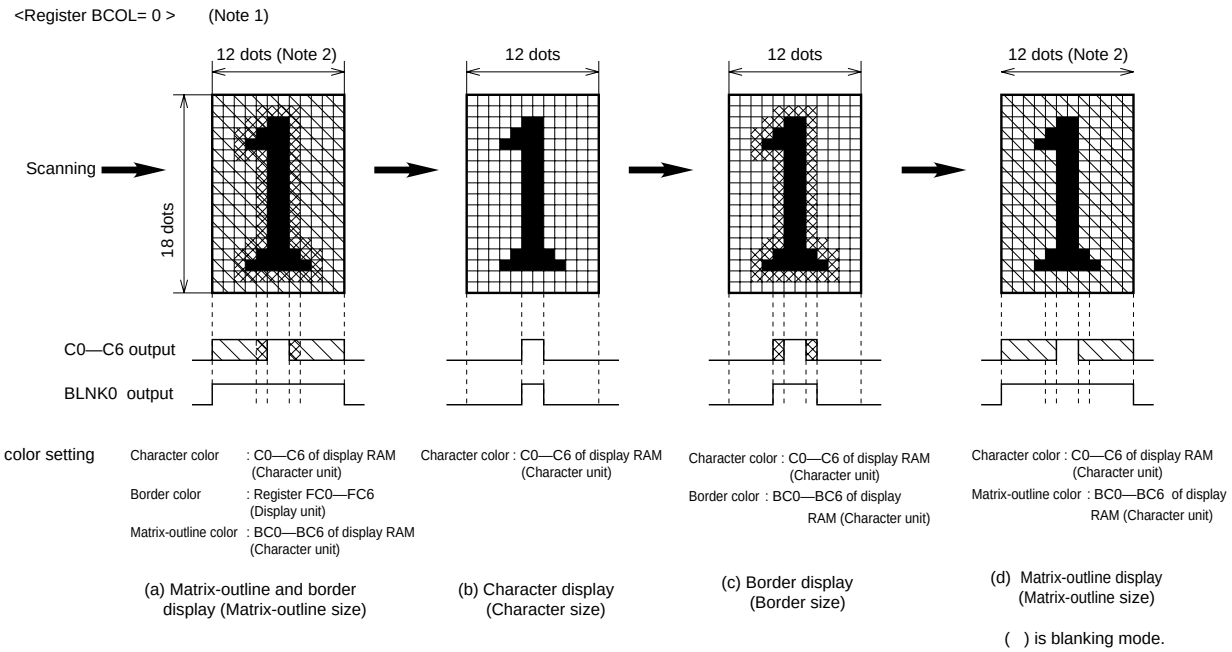
: Blanking the background 12 × 18 dot.

All blanking size

: When set register BCOL to "1", all raster area is blanking.

The display mode and blanking mode can be set line-by-line, as follows, from registers BCOL, BLK1, BLK0, DSP0 to DSP11 (address 123_{16}).

BCOL	BLK1	BLK0	Line of DSPn = "0"		Line of DSPn = "1"	
			Display mode	Blanking mode	Display mode	Blanking mode
0	0	0	Matrix-outline border display	Matrix-outline size	Matrix-outline display	Matrix-outline size
	0	1	Character display	Character size	Border display	Border size
	1	0	Border display	Border size	Matrix-outline display	Matrix-outlinesize
	1	1	Matrix-outline display	Matrix-outline size	Character display	Character size
1	0	0	Matrix-outline border display	All blanking size	Matrix-outline display	All blanking size
	0	1	Character display		Border display	
	1	0	Border display		Matrix-outline display	
	1	1	Matrix-outline display		Character display	



Note 1: When register BCOL is set to "1", the raster range of the display modes set respectively by BLK1 and BLK0 are colored by registers RC0—RC6 (address 126_{16}). And the blanking mode is set all blanking size (all raster size) regardless of the BLK1 and BLK0 settings.

2: The horizontal size of the full matrix-outline size can be set to 14 dots by register BETA14 (address 123_{16}). BLNK0 can also be output at 14 dots.

Fig. 4 Display form

(2) Shadow display

When border display mode, if set SYAD (address 123_{16}) = "0" to "1", it change to shadow display mode.
Border and shadow display are shown below.
Set shadow display color by BR, BG and BB of display RAM or by register FR, FG and FB.

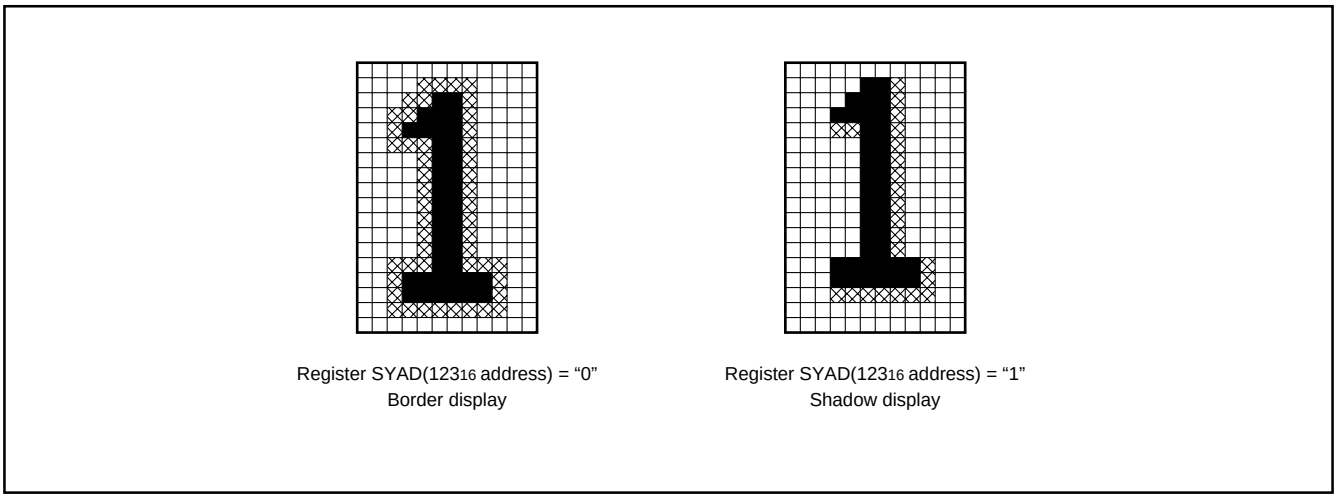


Fig.5 Shadow display

CHARACTER FONT

Images are composed on a 12 × 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.
Character code FF_{16} is fixed as a blank without background. Therefore, cannot register a character font in this code.

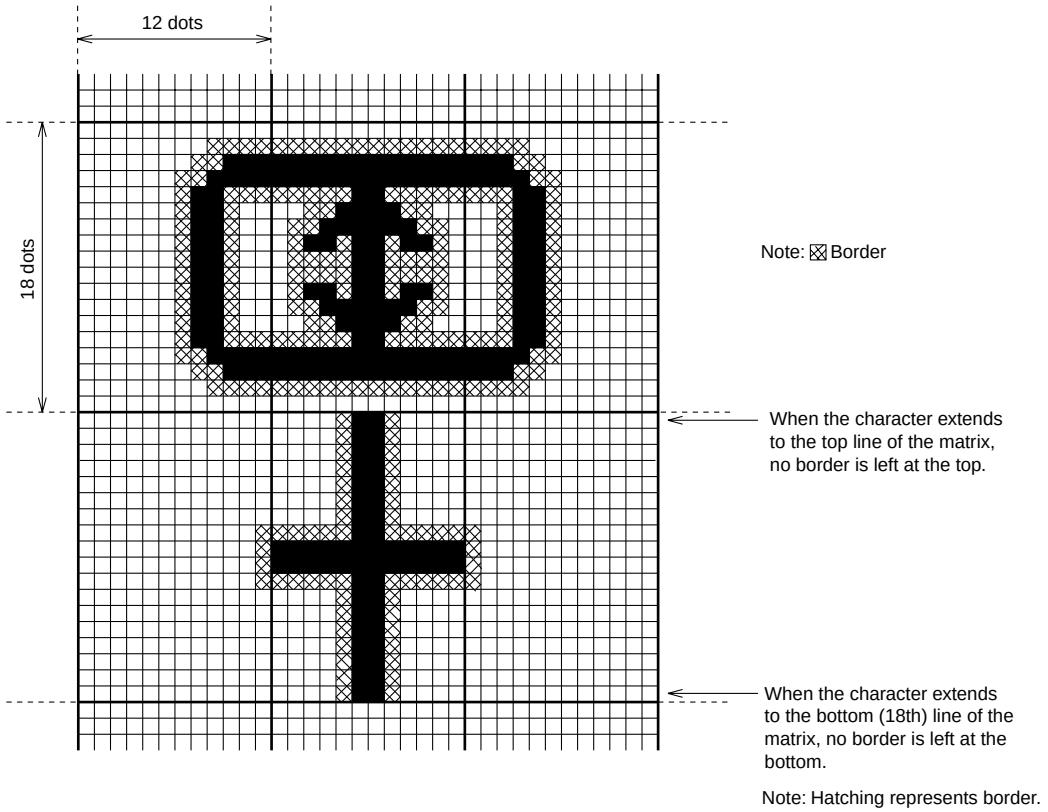


Fig.6 Example of border display

DATA INPUT EXAMPLE

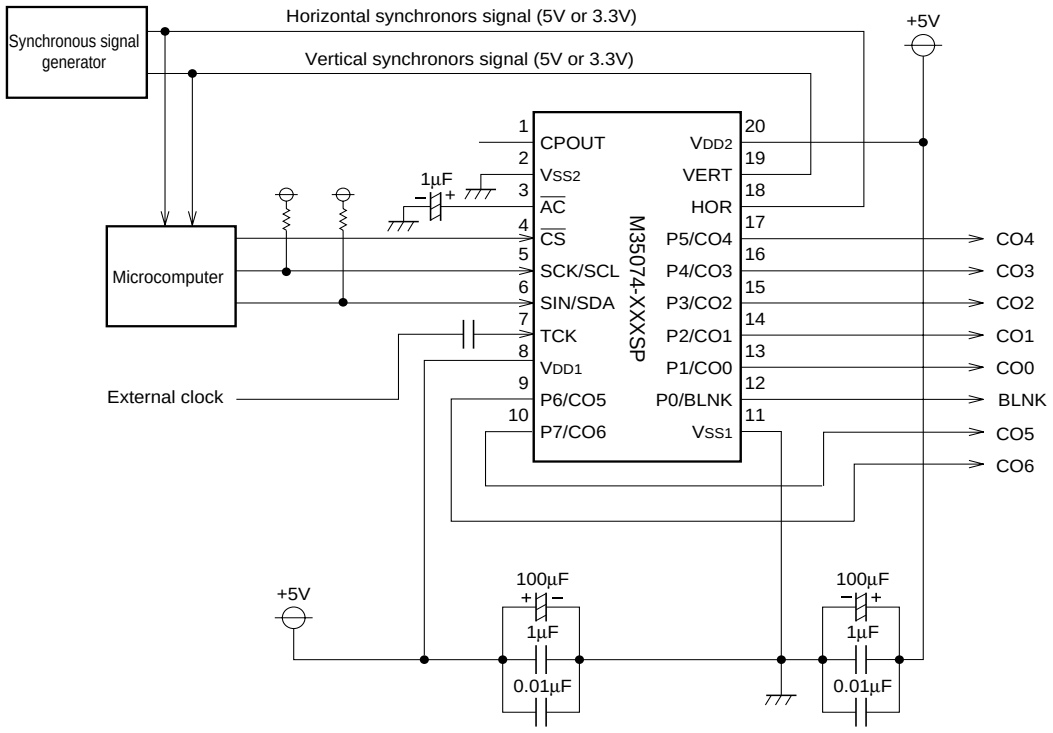
Data of display RAM and display control registers can be set by the 24-bit serial input function or the I²C-BUS serial input function. Example of data setting is shown in Figure 7 (at EXCK0 = "1", EXCK1 = "0" setting).

Example of the M35074-XXXSP Data input setting (at EXCK0 ="1", EXCK1 ="0")

Address/data		DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Remarks
		200 m sec hold																								System set up (Note 3)
Address	120_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	Address setting
data	120_{16}	0	0	0	0	0	1	0	0	0	DIVS2	DIVS1	DIV50	DIV11	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0	Frequency value setting Frequency range setting
data	121_{16}	0	0	0	0	0	0	0	0	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0	PTC7	PTC6	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0	Output set
data	122_{16}	0	VP10	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	HP11	HP10	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display location setting Vertical display location setting
data	123_{16}	0	0	0	SYAD	BEAT14	0	0	0	0	1	1	BCOL	0	0	0	0	0	0	0	0	0	0	0	0	Display form setting
data	124_{16}	0	0	0	0	0	0	0	0	LIN17	LIN16	LIN15	LIN14	LIN13	LIN12	LIN11	LIN10	LIN9	LIN8	LIN7	LIN6	LIN5	LIN4	LIN3	LIN2	Character size setting
data	125_{16}	0	0	0	0	HSZ21	HSZ20	HSZ11	HSZ10	0	0	VSZ2H1	VSZ2H0	VSZ2L1	VSZ2L0	V18SZ1	V18SZ0	0	0	VSZ1H1	VSZ1H0	VSZ1L1	VSZ1L0	V1SZ1	V1SZ0	Character size setting
data	126_{16}	0	0	0	0	0	0	0	0	0	FC6	FC5	FC4	FC3	FC2	FC1	FC0	0	RC6	RC5	RC4	RC3	RC2	RC1	RC0	Color, character size setting
data	127_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	POLH	POLV	0	0	Display OFF
		200 m sec hold																								Be stable/Waiting time
Address	000_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Address setting
data	000_{16}	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	C6	C5	C4	C3	C2	C1	C0	C8	C7	C6	C5	C4	C3	C2	C1	C0	Character setting
.....		.....	Background coloring							Character color									Character code							
data	$11F_{16}$	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	C6	C5	C4	C3	C2	C1	C0	C8	C7	C6	C5	C4	C3	C2	C1	C0	
Address	127_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	1	1	Address setting
data	127_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	POLH	POLV	0	0	Display ON

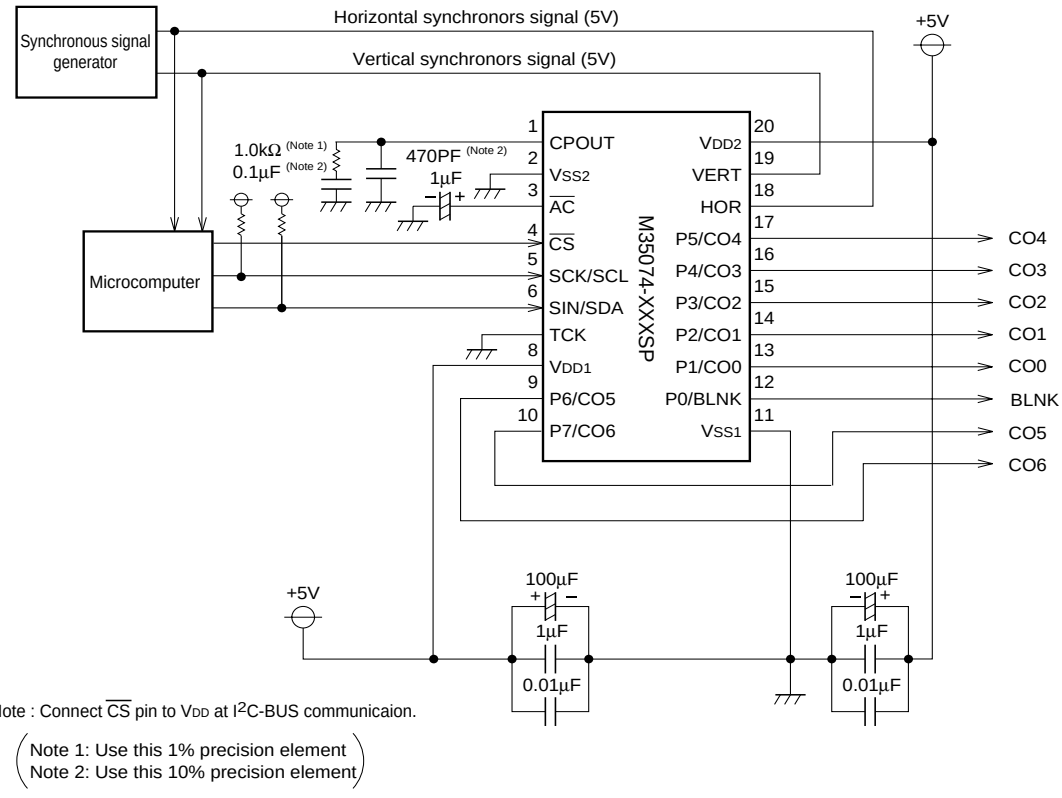
Notes 1 : Input a horizontal synchronous signal into the HOR pin and a vertical synchronous signal into the VERT pin.
2 : Matrix-outline display in this data.
3 : Secure the waiting time of 200ms after releasing $\overline{AC}$, and set data from setting the display frequency (setting of the register).
4 : Set data to Display RAM at internal clock (display clock) is stabilized.

Fig. 7 Example of data setting



Notes 1: CPOUT pin can be opened when use only EXCK1 = "0" and EXCK0 = "0".
2: Connect $\overline{CS}$ pin to V_{DD} at I^2C-BUS communicaion.

Fig.8 Example of the M35074-XXXSP peripheral circuit (External clock mode 1. At EXCK1 = "0", EXCK0 = "0")



Note : Connect $\overline{CS}$ pin to V_{DD} at I^2C-BUS communicaion.

(Note 1: Use this 1% precision element
Note 2: Use this 10% precision element)

Fig.9 Example of the M35074-XXXSP peripheral circuit (Internal clock mode. At EXCK1 = "0", EXCK0 = "1")

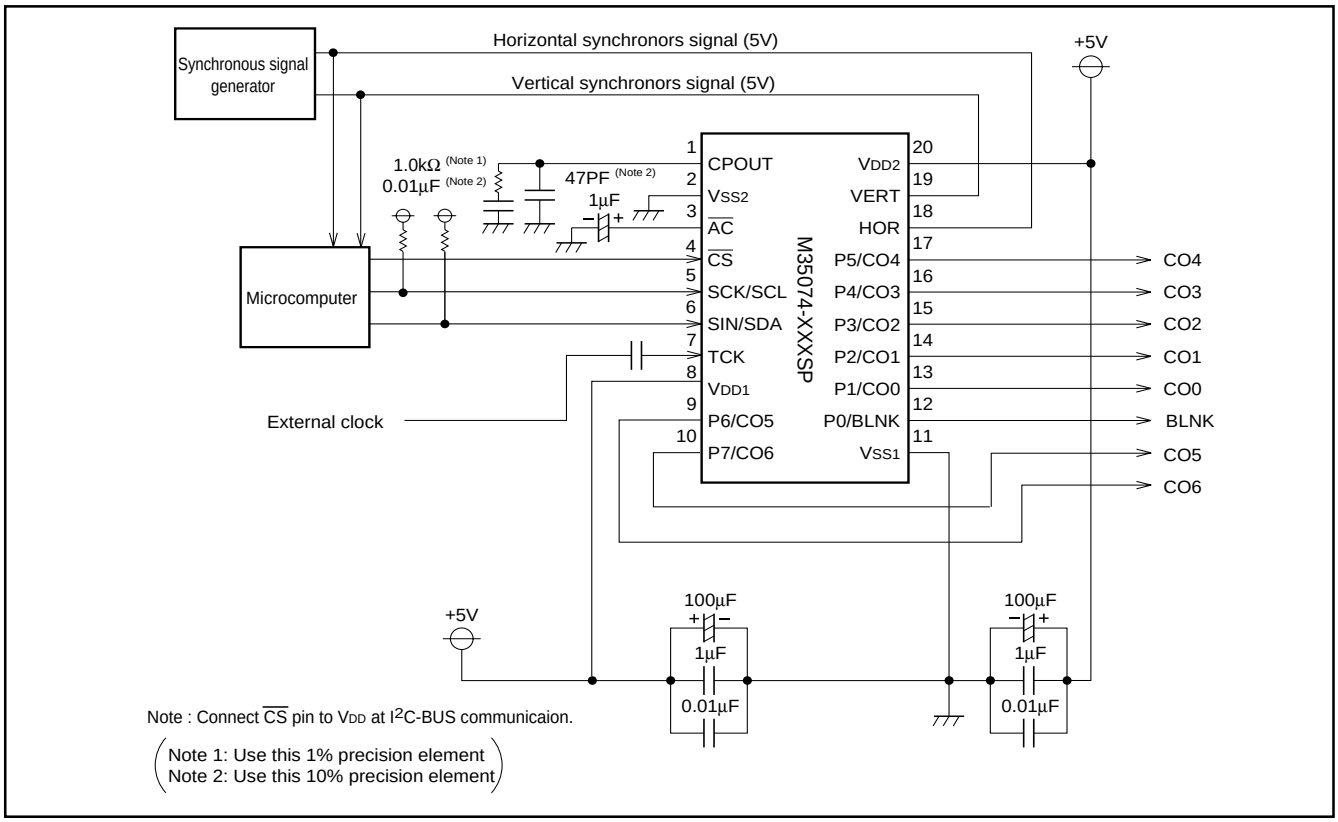


Fig.10 Example of the M35074-XXXSP peripheral circuit (External clock mode2. At EXCK1 = "1", EXCK0 = "1")

DATA INPUT 1

(1) SERIAL DATA INPUT TIMING

(a) Serial data should be input with the LSB first.

(b) The address consists of 24 bits.

(c) The data consists of 24 bits.

(d) The 24 bits in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 24 bits. Therefore, it is not necessary to input the address from the second data.

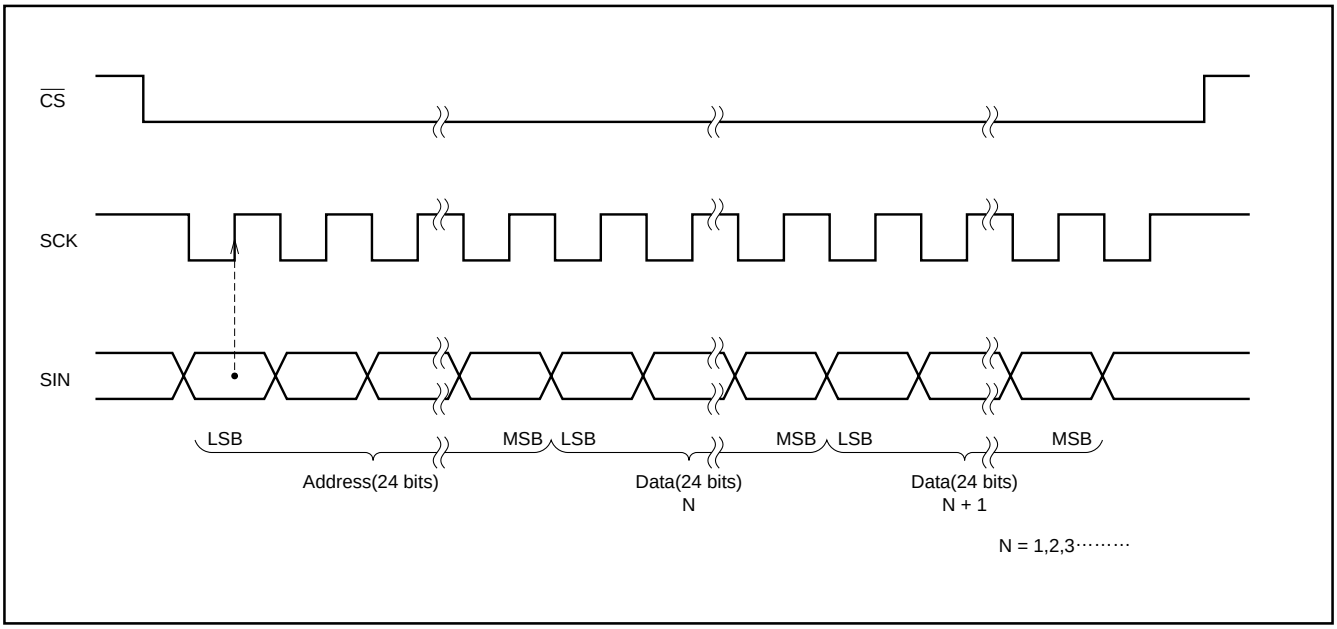


Fig.11 Serial input timing

(2) TIMING REQUIREMENTS
Data input

Symbol	Parameter	Limits			Unit	Remarks
		Min.	Typ.	Max.		
$t_{w(SCK)}$	SCK width	200	—	—	ns	See Figure 12
$t_{su(\overline{CS})}$	$\overline{CS}$ setup time	200	—	—	ns	
$t_{h(\overline{CS})}$	$\overline{CS}$ hold time	2	—	—	µs	
$t_{su(SIN)}$	SIN setup time	200	—	—	ns	
$t_{h(SIN)}$	SIN hold time	200	—	—	ns	
t_{word}	1 word writing time	14	—	—	µs	

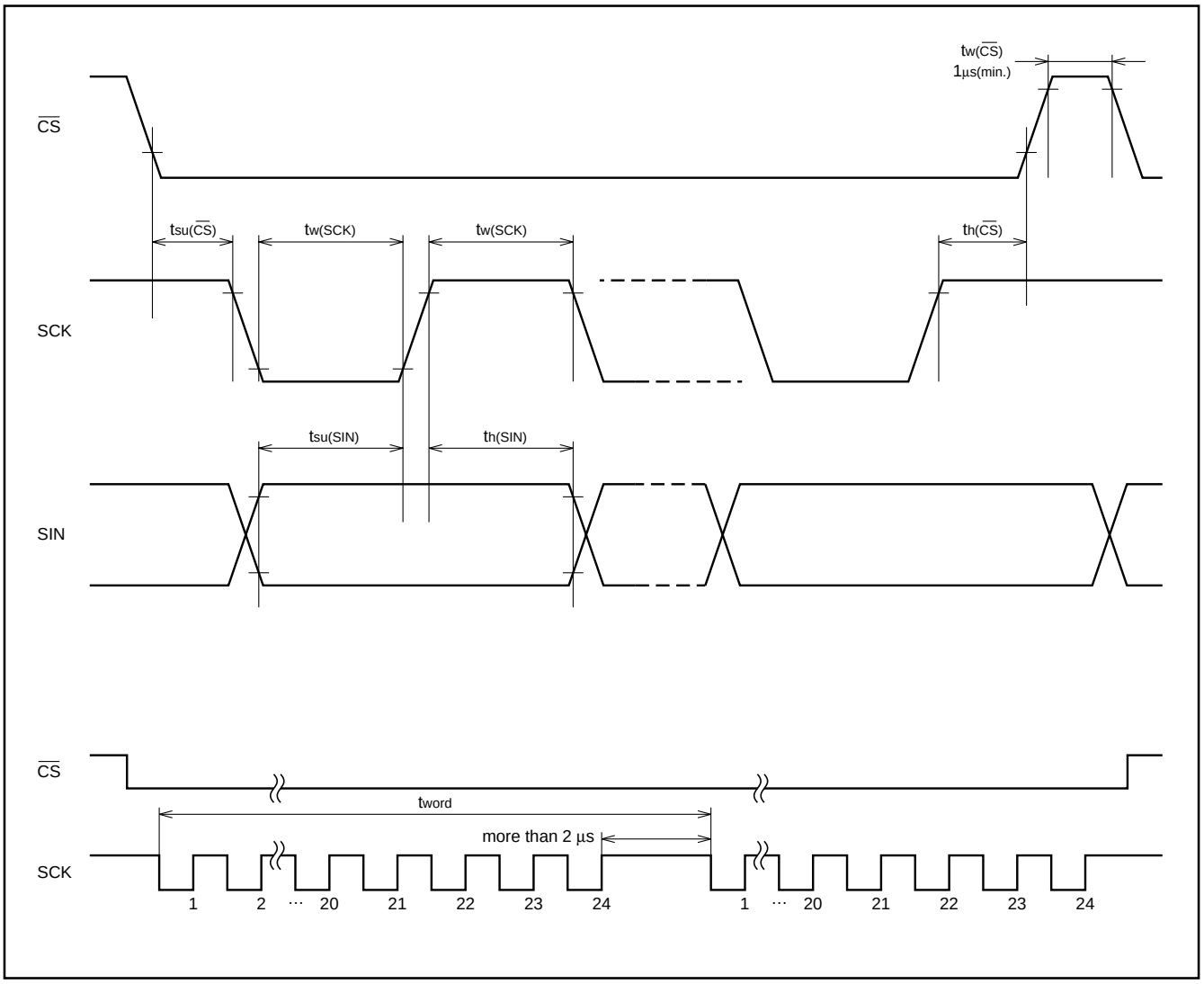


Fig. 12 Serial input timing requirements

DATA INPUT 2

(1) I^2C-Bus communication function (At only VDD = 5V)

This IC has a built-in data transmission interface which utilizes 2 unidirectional buses. In communications, this IC functions as a slave reception device.

The IC is synchronized with the serial clock (SCL) sent from the master device and receives the data (SDA).

Communications are controlled from the start/stop states.

Also, always in put the control byte after attaining the start state.

The below chart shows the start/stop state and control byte configuration.

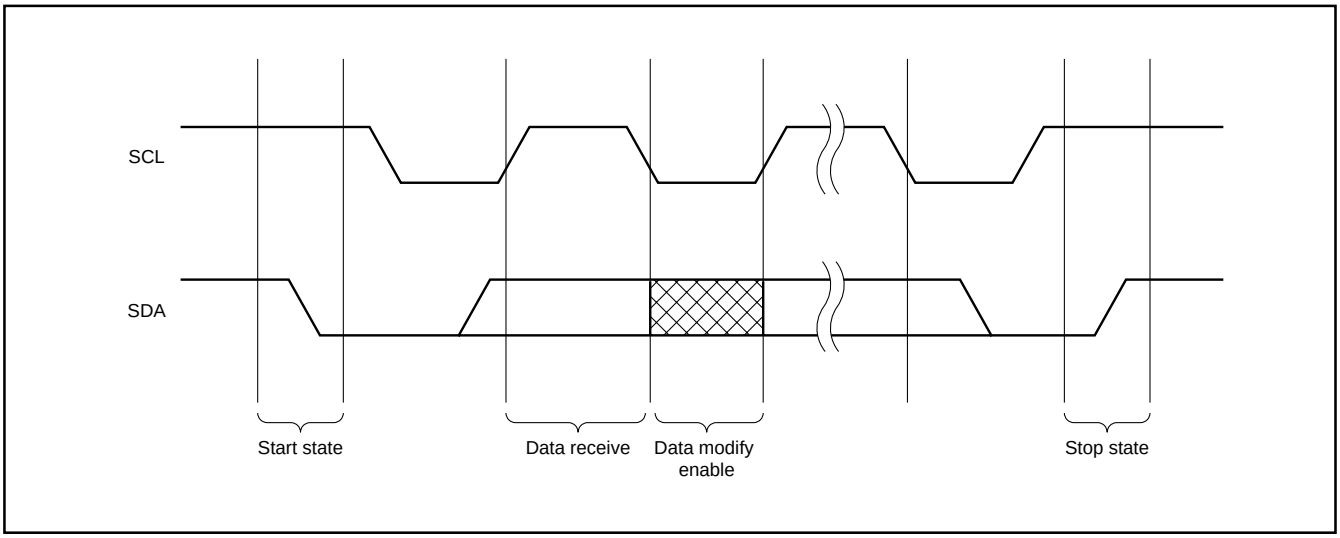


Fig.13 Start state / Stop state

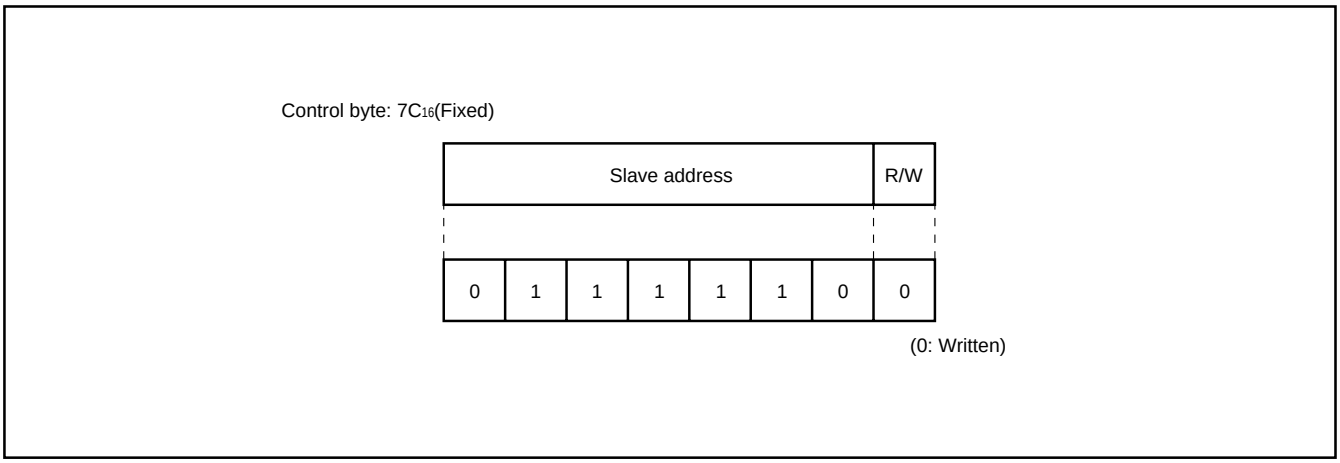
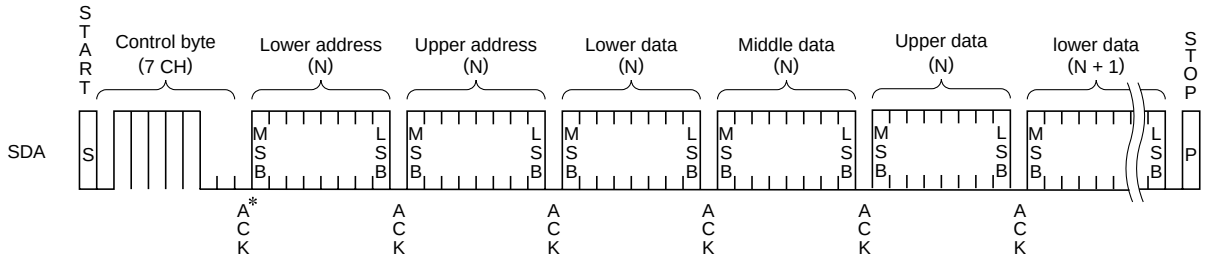


Fig.14 Control byte configuration

(2) Data input (Sequence)

(a) Addresses are consists of 16 bits.
(b) Data is consists of 24 bits.
(c) Addresses and data are communicated in 8-bit units. Input the lower 8 bits before the upper 8 bits. Make input from the MSB side.
(d) After the start state has been attained and the control byte (7CH) received, the next 16 bits (2 bytes) are for inputting the address. Addresses are increased in increments for every 24 bits (3 bytes) of data input thereafter. As a result, it is not necessary to input the address from the second data.

Note:During external synchronous , do not stop the external clock input from the TCK pin while inputting data.



ACK* (Acknowledge) : Output the acknowledge signal whenever one byte input after the start state. Output the acknowledge signal and recieve the data thereafter when match the slave address (7CH).

Fig.15 Data input sequence

(3) TIMING REQUIREMENTS
Data input

Symbol	Parameter	Limits				Unit	Remarks
		Typ. mode		High-speed mode			
		Min.	Max.	Min.	Max.		
f_{CLK}	Clock frequency	0	100	0	400	KHz	
t_{HIGH}	HIGH period of Clock	4000	–	600	–	ns	
t_{LOW}	LOW period of Clock	4700	–	1300	–	ns	
t_R	SDA & SCL rise time	–	1000	20+(Note) 0.1C_B	300	ns	
t_F	SDA & SCL fall time	–	300	20+(Note) 0.1C_B	300	ns	
t_{HD} : STA	Hold time at START status	4000	–	600	–	ns	
t_{SU} : STA	Set up time at START status	4700	–	600	–	ns	Only at START state repeating generation
t_{HD} : DAT	Data input hold time	0	–	0	–	ns	
t_{SU} : DAT	Data input setup time	250	–	100	–	ns	
t_{SU} : STO	Set up time at STOP state	4000	–	600	–	ns	
t_{BUF}	Bus release time	4700	–	1300	–	ns	Time must be released bus before next transmission
t_{SP}	Input filter / spike suppress (SDA & SCL pin)	N/A	N/A	0	50	ns	

Note: CB = total capacitance of 1 bus line.

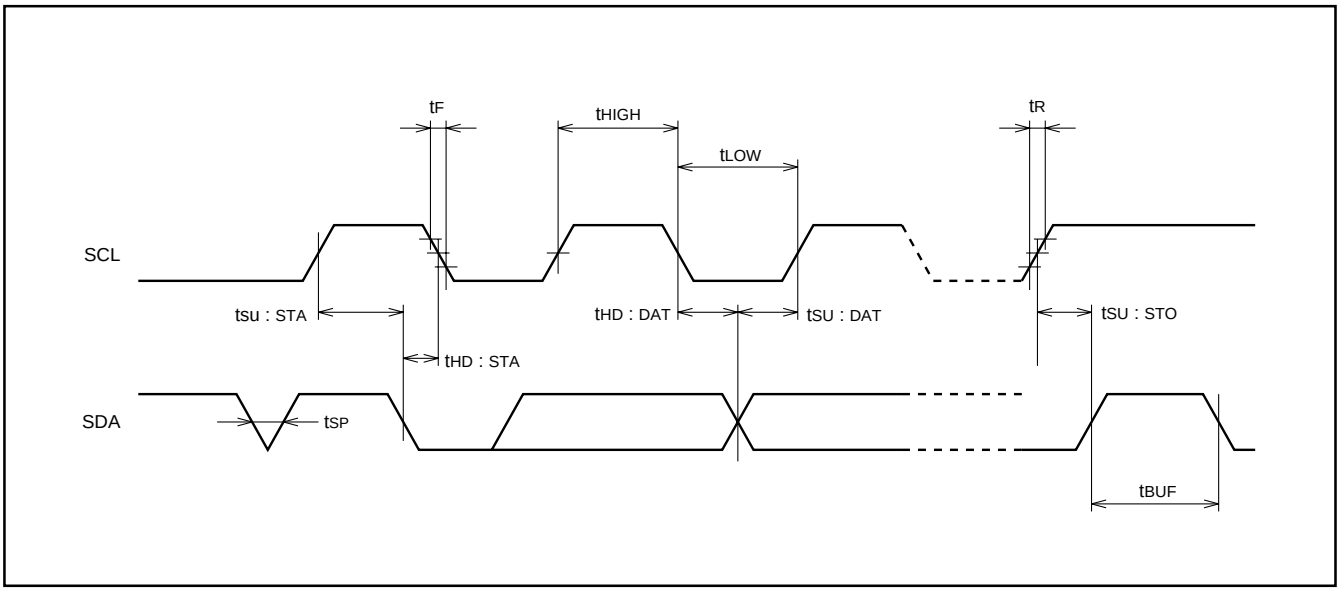


Fig.16 Data input timing

ABSOLUTE MAXIMUM RATINGS (V_{DD} = 5.00V, Ta = –20 to +85°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to V_{SS}.	–0.3 to +6.0	V
V_I	Input voltage		V_{SS} –0.3 ≤ V_I ≤ V_{DD} +0.3	V
V_O	Output voltage		V_{SS} ≤ V_O ≤ V_{DD}	V
P_d	Power dissipation	Ta = +25 °C	+300	mW
T_{opr}	Operating temperature		–20 to +85	°C
T_{stg}	Storage temperature		–40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (V_{DD} = 5.00V, Ta = –20 to +85°C, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min.	Typ.	Max.	
V_{DD}	Supply voltage	5V		4.75	5.00	5.25	V
		3.3V		3.00	3.30	3.60	V
V_{IH}	"H" level input voltage	$\overline{AC}$, $\overline{CS}$, HOR, VERT		0.8 × V_{DD}	V_{DD}	V_{DD}	V
		SCK/SCL, SIN/SDA		0.7 × V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	"L" level input voltage	$\overline{AC}$, $\overline{CS}$, HOR, VERT		0	0	0.2 × V_{DD}	V
		SCK/SCL, SIN/SDA		0	0	0.3 × V_{DD}	V
F_{OSC}	Oscillating frequency for display	External clock mode 1	V_{DD}=4.75 to 5.25V	6.3	–	80.0	MHz
			V_{DD}=3.00 to 3.60V	6.3	–	40.0	MHz
		External clock mode 2	V_{DD}=4.75 to 5.25V	20.0	–	120.0	MHz
		Internal clock mode	V_{DD}=4.75 to 5.25V	20.0	–	120.0	MHz
H.sync	Horizontal synchronous signal input frequeney		V_{DD}=4.75 to 5.25V	15.0	–	130.0	kHz
			V_{DD}=3.00 to 3.60V	15.0	–	60.0	kHz

ELECTRICAL CHARACTERISTICS 1 V_{DD} = 5V (V_{DD} = 5.00V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{DD}	Supply voltage		Ta = –20 to +85°C	4.75	5.0	5.25	V
I_{DD}	Supply current		V_{DD} = 5.00V	—	40	60	mA
V_{OH}	"H" level output voltage	P0 to P7 (Note1)	V_{DD} = 4.75V, I_{OH} = -0.4mA	3.5	—	—	V
		CPOUT	V_{DD} = 4.75V, I_{OH} = -0.05mA				
V_{OL}	"L" level output voltage	P0 to P7 (Note2)	V_{DD} = 4.75V, I_{OL} = 0.4mA	—	—	0.4	V
		CPOUT	V_{DD} = 4.75V, I_{OL} = 0.05mA				
		SIN/SDA	V_{DD} = 4.75V, I_{OL} = 3.0mA				
R_I	Pull-up resistance $\overline{AC}$, $\overline{CS}$		V_{DD} = 5.00V	10	30	100	kΩ
V_{TCK}	External clock input width		4.75V ≤ V_{DD} ≤ 5.25V	0.6 X V_{DD}	—	0.9 X V_{DD}	V

Notes 1: The current from the IC must not exceed – 0.4 mA/port at any of the port pins (P0 to P7).
2: The current flowing into the IC must not exceed 0.4 mA/port at any of port pins (P0 to P7).

ELECTRICAL CHARACTERISTICS 2 V_{DD} = 3.3V (V_{DD} = 3.30V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	Ta = –20 to +85°C	3.00	3.30	3.60	V
I_{DD}	Supply current	V_{DD} = 3.30V	—	20	30	mA
V_{OH}	"H" level output voltage P0 to P7 (Note1)	V_{DD} = 3.00V, I_{OH} = -0.1mA	2.60	—	—	V
V_{OL}	"L" level output voltage P0 to P7 (Note2)	V_{DD} = 3.00V, I_{OL} = 0.1mA	—	—	0.4	V
R_I	Pull-up resistance $\overline{AC}$, $\overline{CS}$	V_{DD} = 3.30V	30	—	150	kΩ
V_{TCK}	External clock input width	3.00V ≤ V_{DD} ≤ 3.60V	0.9 X V_{DD}	—	V_{DD}	V

Notes 1: The current from the IC must not exceed – 0.1 mA/port at any of the port pins (P0 to P7).
2: The current flowing into the IC must not exceed 0.1 mA/port at any of port pins (P0 to P7).

NOTE FOR SUPPLYING POWER

(1) Timing of power supplying to $\overline{AC}$ pin

The internal circuit of M35074-XXXSP is reset when the level of the auto clear input pin $\overline{AC}$ is "L". This pin in hysteresis input with the pull-up resistor.

The timing about power supplying of $\overline{AC}$ pin is shown in Figure 15.

After supplying the power (V_{DD} and V_{SS}) to M35074-XXXSP and the supply voltage becomes more than 0.8 × V_{DD}, it needs to keep V_{IL} time; tw of the $\overline{AC}$ pin for more than 1ms.

Start inputting from microcomputer after $\overline{AC}$ pin supply voltage becomes more than 0.8 × V_{DD} and keeping 200ms wait time.

(2) Timing of power supplying to V_{DD1} and V_{DD2}.

Supply power to V_{DD1} and V_{DD2} at the same time.

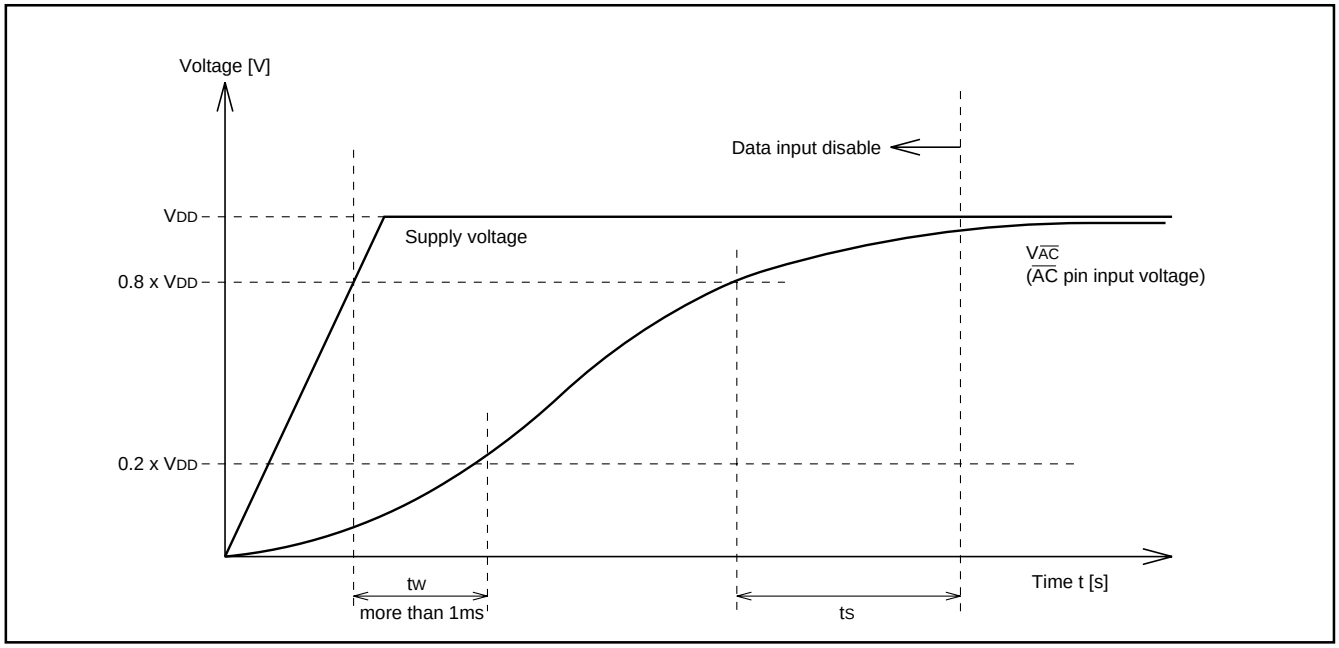


Fig.17 Timing of power supplying to $\overline{AC}$ pin

PRECAUTION FOR USE

Notes on noise and latch-up

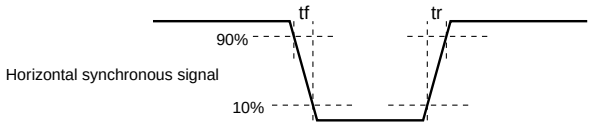
In order to avoid noise and latch-up, connect a bypass capacitor (≈0.1µF) directly between the V_{DD1} pin and V_{SS1} pin, and the V_{DD2} pin and V_{SS2} pin using a heavy wire.

Note for waveform timing of the horizontal signals to the HOR pin

Set horizontal synchronous signal edge* waveform timing to under 5ns and input to HOR pin.

Set only the side which set by B/$\overline{F}$ register waveform timing under 5ns and input to HOR pin.

*: Set front porch edge or back porch edge by B/$\overline{F}$ register (address 127_{16}) .



DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

(1) M35074-XXXSP mask ROM order confirmation form

(2) 20P4B mark specification form

(3) ROM data : EPROMs or floppy disks

*In the case of EPROMs, thres sets of EPROMs are required per pattern.

*In the case of floppy disks, 3.5-inch 2HD disk (1BM format) is required per pattern.

STANDARD ROM TYPE : M35074-002SP

M35074-002SP is a standard ROM type of M35074-XXXSP.
The character patterns are fixed to the contents of Figure 18 to 25.

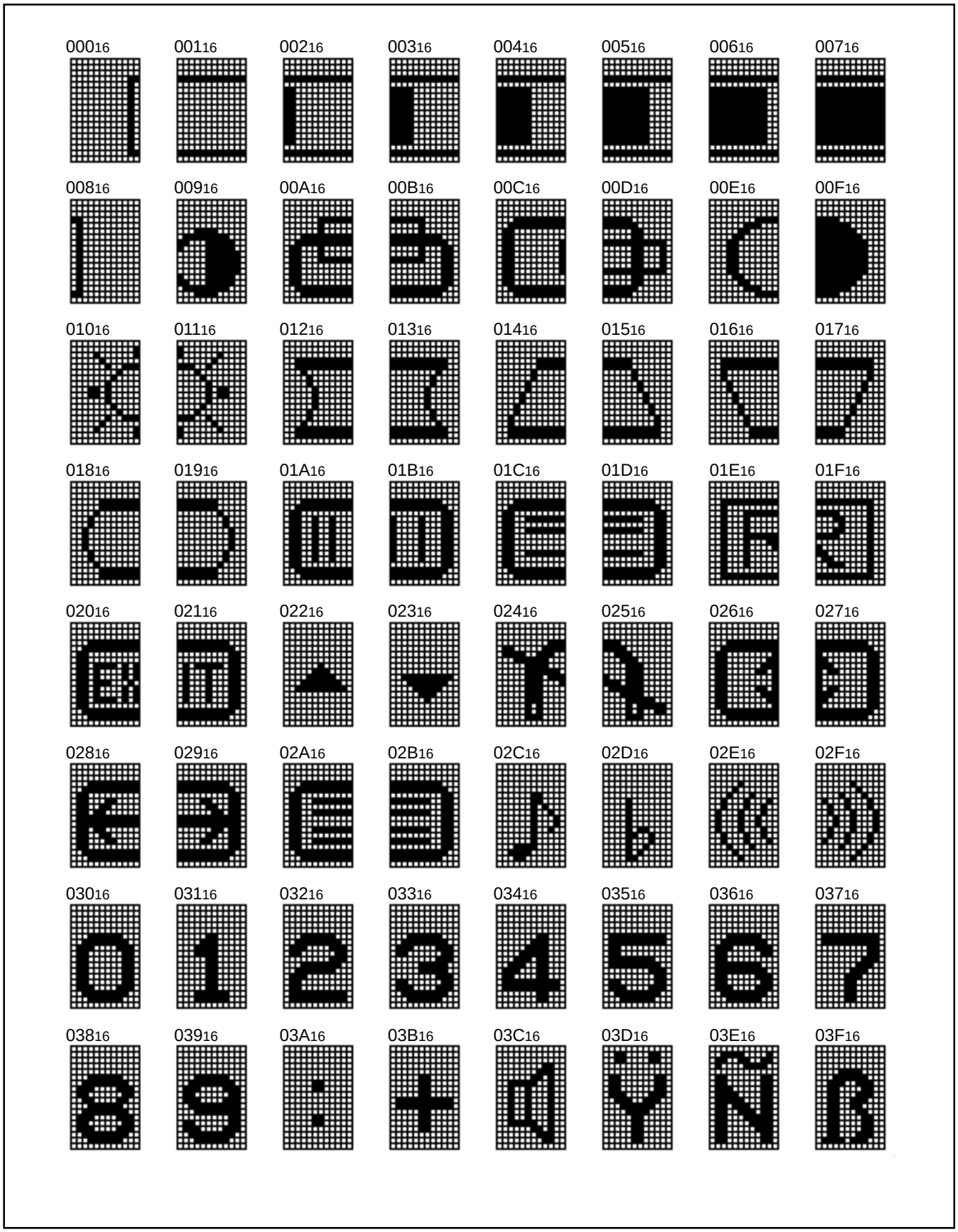


Fig.18 M35074-002SP character patterns (1)

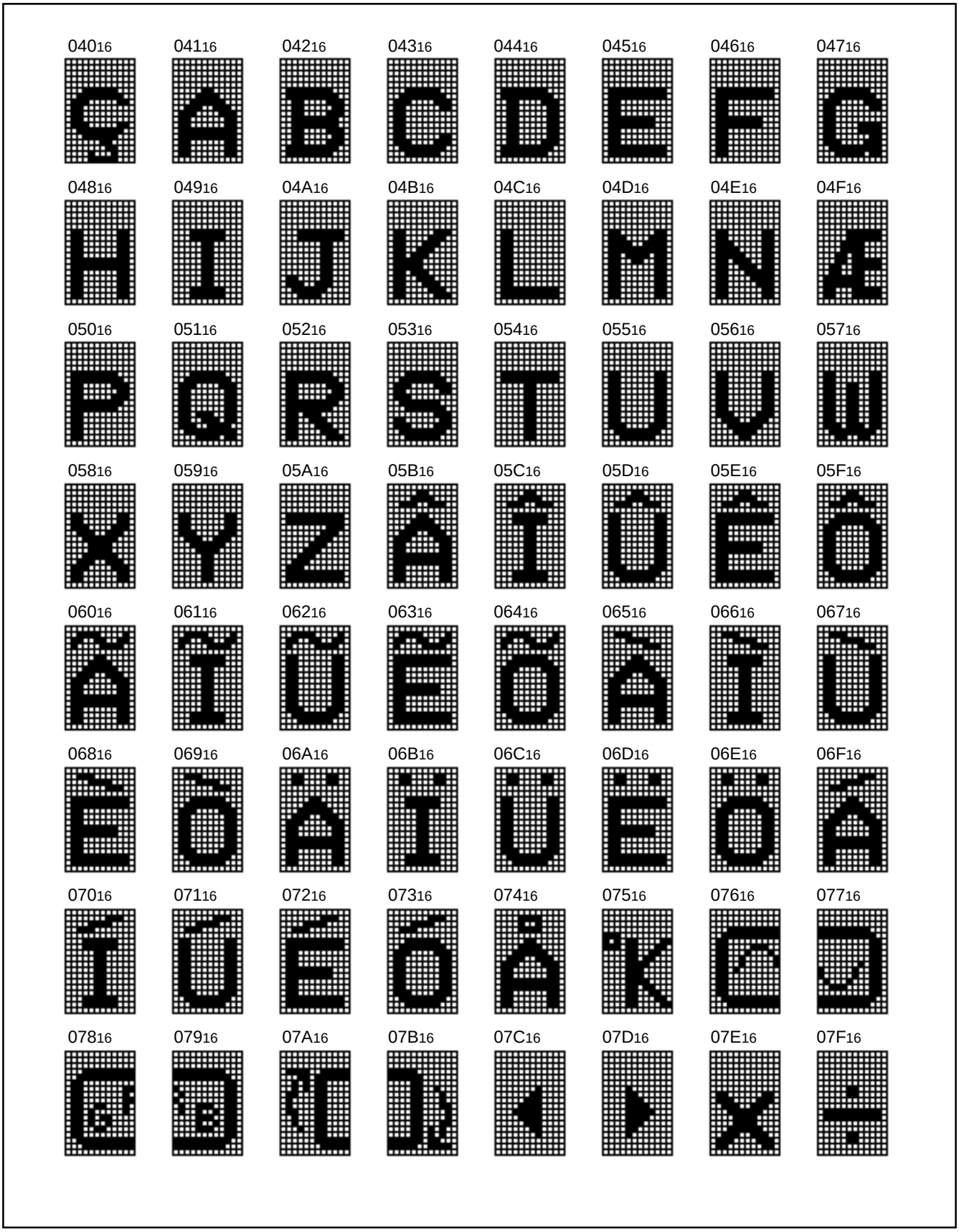


Fig.19 M35074-002SP character patterns (2)

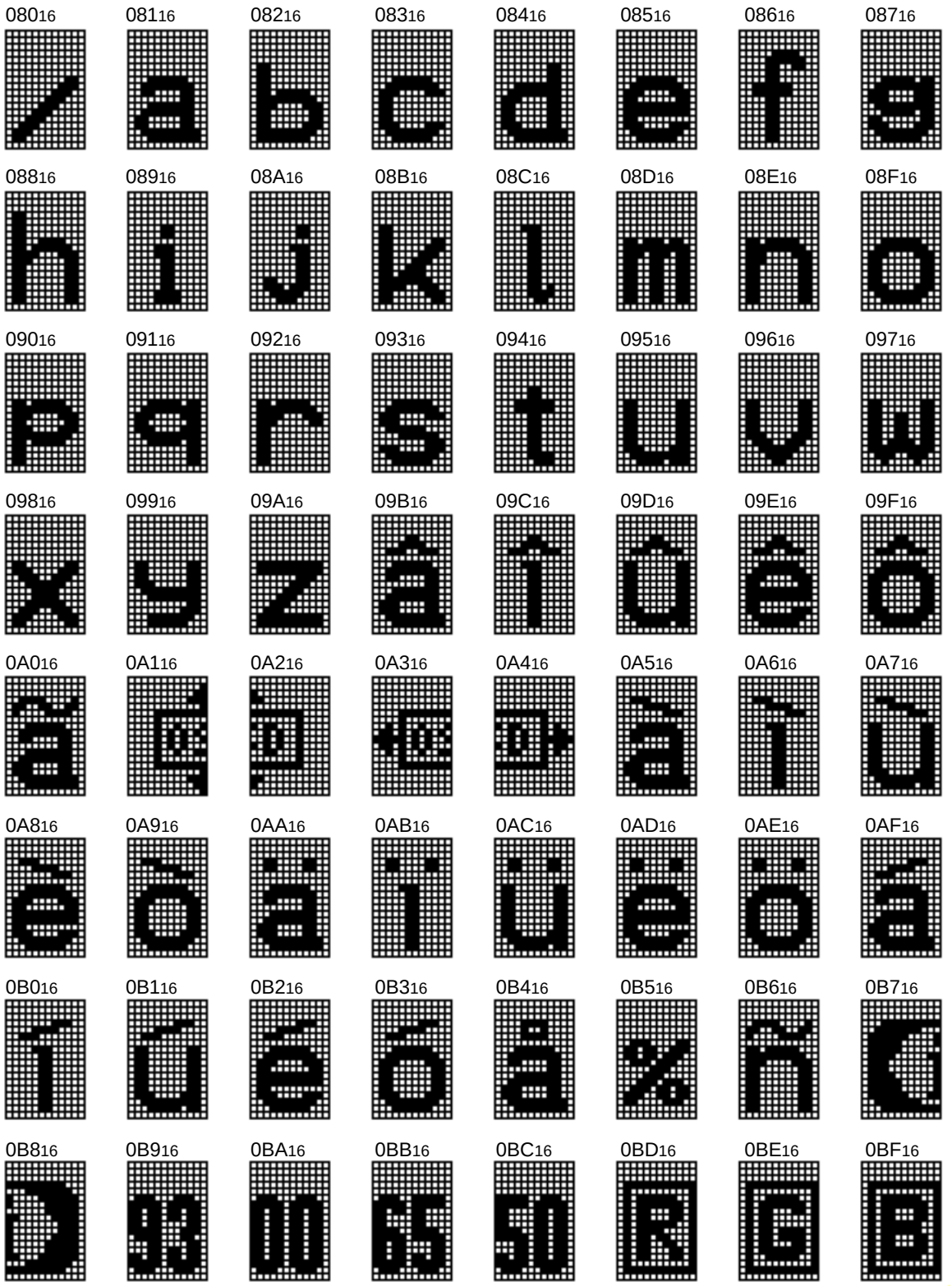


Fig.20 M35074-002SP character patterns (3)

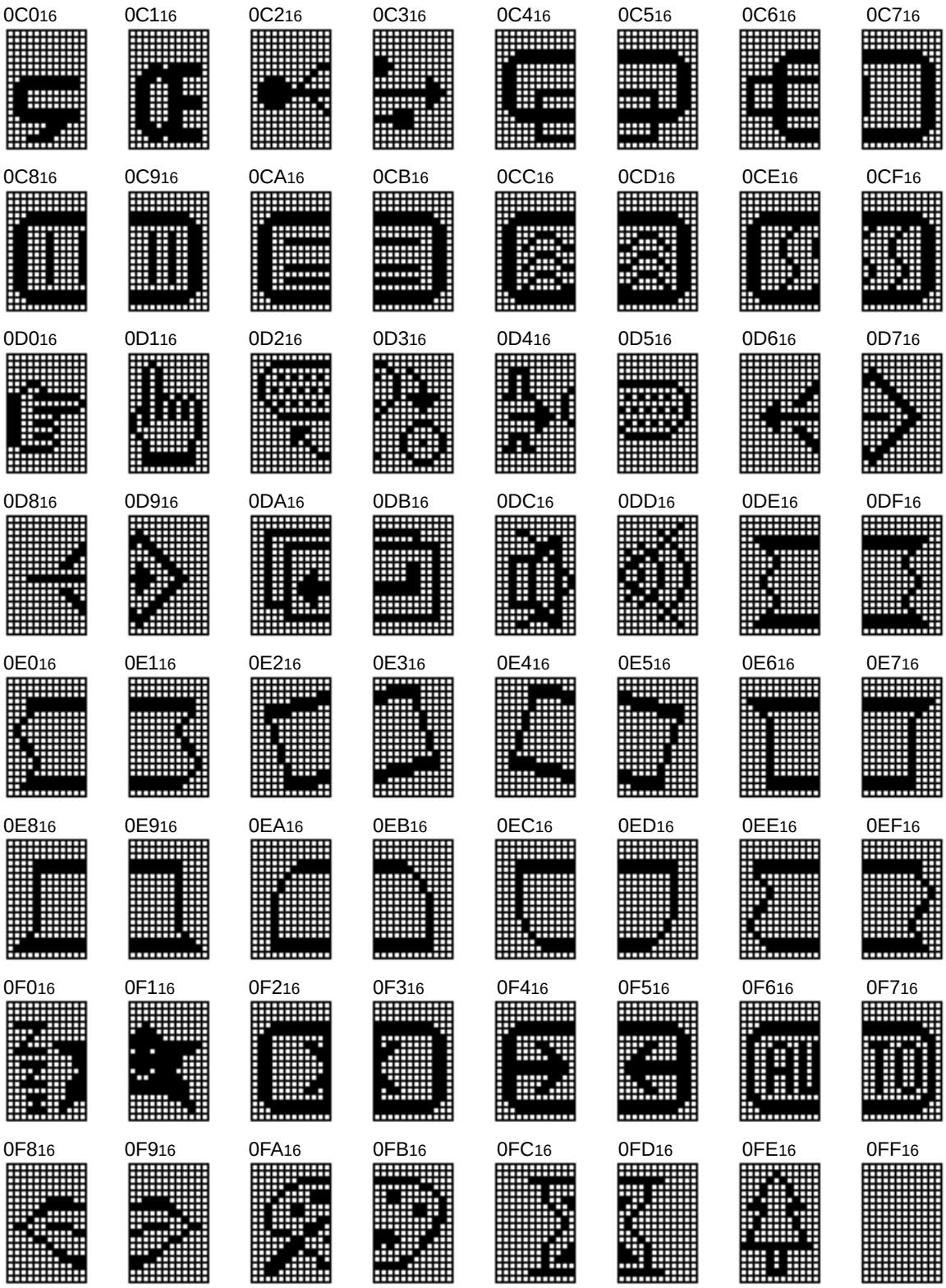


Fig.21 M35074-002SP character patterns (4)

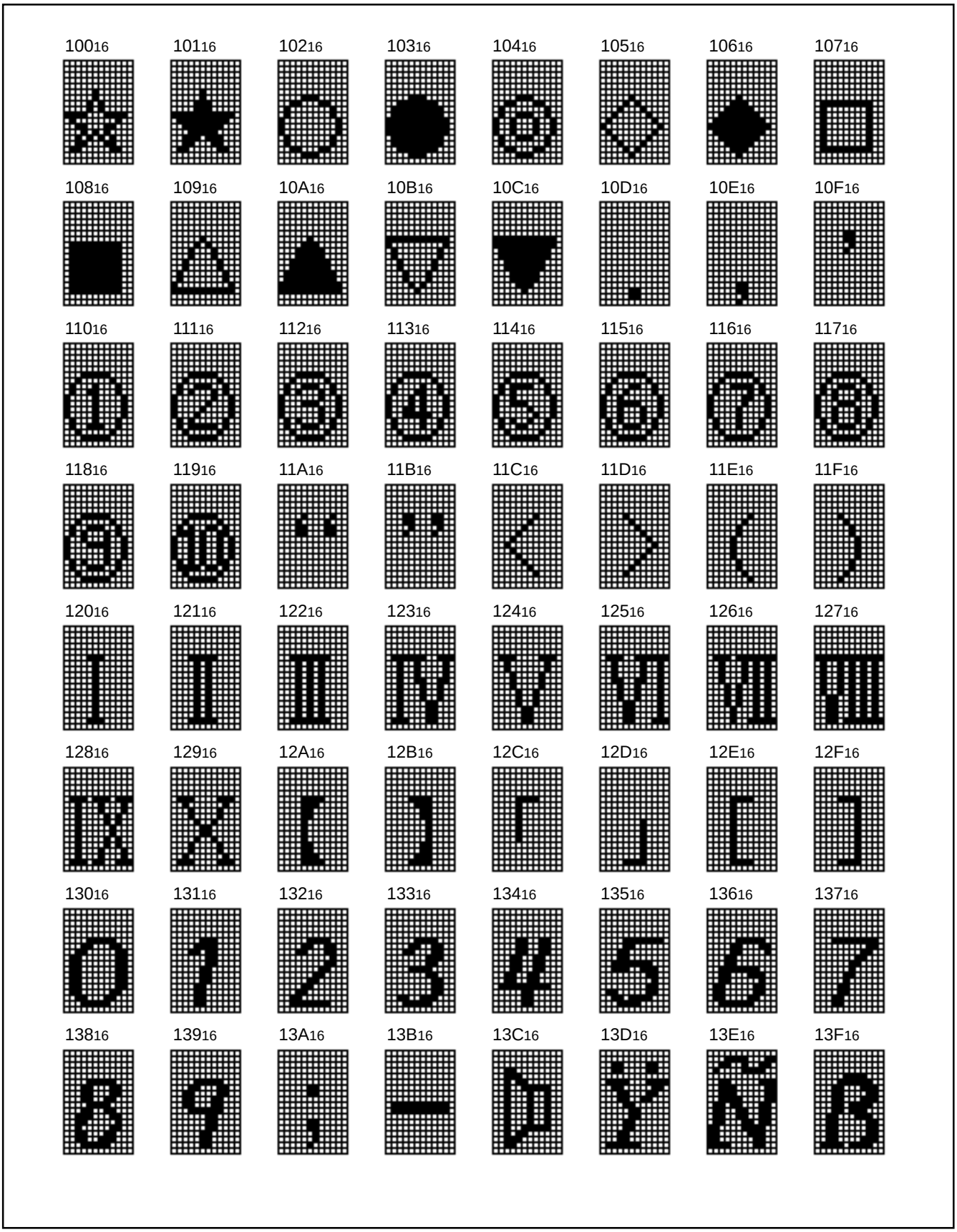


Fig.22 M35074-002SP character patterns (5)

Fig.23 M35074-002SP character patterns (6)

Fig.24 M35074-002SP character patterns (7)

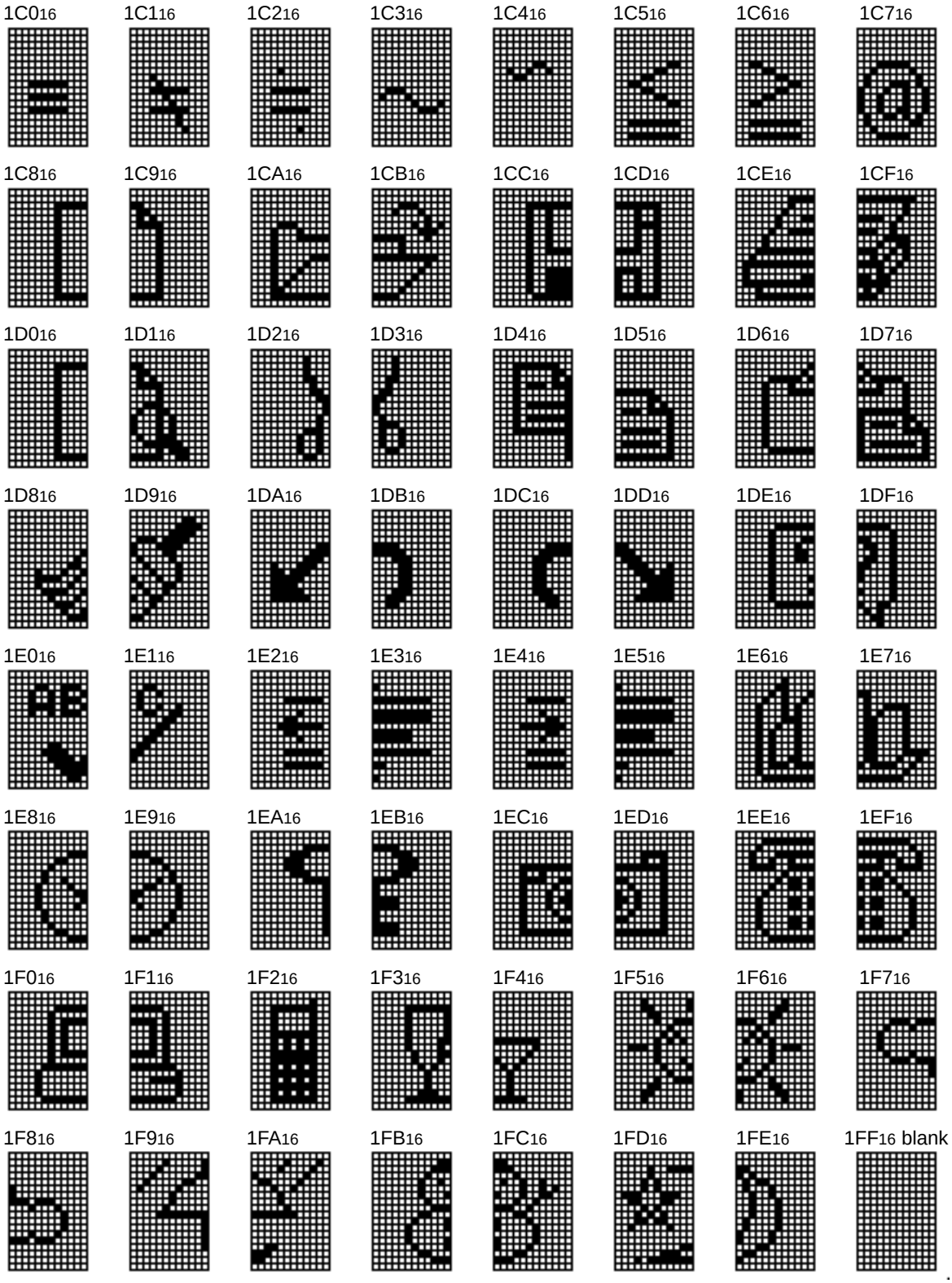


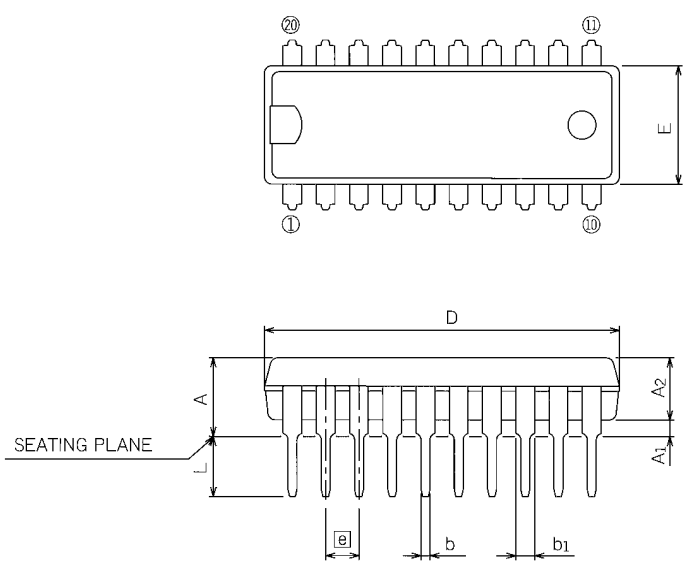
Fig.25 M35074-002SP character patterns (8)

PACKAGE OUTLINE

20P4B — Plastic 20pin 300mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP20-P-300-1.78	—	1.0	

Scale : 2.5/1



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b	0.38	0.48	0.58
b_1	0.9	1.0	1.3
c	0.22	0.27	0.34
D	18.8	19.0	19.2
E	6.15	6.3	6.45
e	—	1.778	—
e1	—	7.62	—
L	3.0	—	—
θ	0°	—	15°

MITSUBISHI MICROCOMPUTERS

M35074-XXXSP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

Renesas Technology Corp.
Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

RENESAS
Renesas Technology Corp.

REVISION DESCRIPTION LIST	M35074-XXXSP Data Sheet

<table>
<tr><th>Rev. No.</th><th>Revision Description</th><th>Rev. date</th></tr>
<tr><td>1.0</td><td>First Edition</td><td>0111</td></tr>
<tr><td>1.1</td><td>2nd Edition
p10
BEFORE
<table>
<tr><th>BLK0</th><th>BLK1</th><th>DSPn="0"</th><th>DSPn="1"</th></tr>
<tr><td>0</td><td>0</td><td>Matrix-outline border</td><td>Matrix-outline</td></tr>
<tr><td>0</td><td>1</td><td>Character</td><td>Border</td></tr>
<tr><td>1</td><td>0</td><td>Border</td><td>Matrix-outline</td></tr>
<tr><td>1</td><td>1</td><td>Matrix-outline</td><td>Charcter</td></tr>
</table>
(At register BCOL="0")
AFTER
<table>
<tr><th>BLK1</th><th>BLK0</th><th>DSPn="0"</th><th>DSPn="1"</th></tr>
<tr><td>0</td><td>0</td><td>Matrix-outline border</td><td>Matrix-outline</td></tr>
<tr><td>0</td><td>1</td><td>Character</td><td>Border</td></tr>
<tr><td>1</td><td>0</td><td>Border</td><td>Matrix-outline</td></tr>
<tr><td>1</td><td>1</td><td>Matrix-outline</td><td>Charcter</td></tr>
</table>
(At register BCOL="0")
BEFORE
<table>
<tr><th>BLK0</th><th>BLK1</th><th>Blanking mode</th></tr>
<tr><td>0</td><td>0</td><td>Matrix-outline size</td></tr>
<tr><td>0</td><td>1</td><td>Character size</td></tr>
<tr><td>1</td><td>0</td><td>Border size</td></tr>
<tr><td>1</td><td>1</td><td>Matrix-outline size</td></tr>
</table>
AFTER
<table>
<tr><th>BLK1</th><th>BLK0</th><th>Blanking mode</th></tr>
<tr><td>0</td><td>0</td><td>Matrix-outline size</td></tr>
<tr><td>0</td><td>1</td><td>Character size</td></tr>
<tr><td>1</td><td>0</td><td>Border size</td></tr>
<tr><td>1</td><td>1</td><td>Matrix-outline size</td></tr>
</table>
</td><td>0202</td></tr>
<tr><td>1.2</td><td>3nd Edition
p1 FEATURES Data input By 16-bit → By 24-bit
p2 PIN DESCRIPTION $\overline{CS}$, SCK/SCL, SIN/SDA Function <At 16-bit....> → <At 24-bit....>
p14 (8) Address 127_{16} B Remarks “Refer to REGISTER.....” → Deletion
p21 DATA INPUT EXAMPLE “the 24-bit serial input function or” → Insertion
p24 DATA INPUT 1 (d) “16 bits” → “24 bits”, Fig.11 (16 bits) → (24 bits)
SERIAL DATA INPUT TIMING (d) “16 bits” → “24 bits”
p25 Table Data input t_{word} Limits “10” → “14”,
Fig.12 SCK “12,13,14,15,16” → “20,21,22,23,24”
p27 (2) Data input (Sequence) (d) “16 bits” → “24 bits”</td><td>0204</td></tr>
<tr><td></td><td></td><td></td></tr>
</table>