

## 64-Kbit (8K x 8) nvSRAM

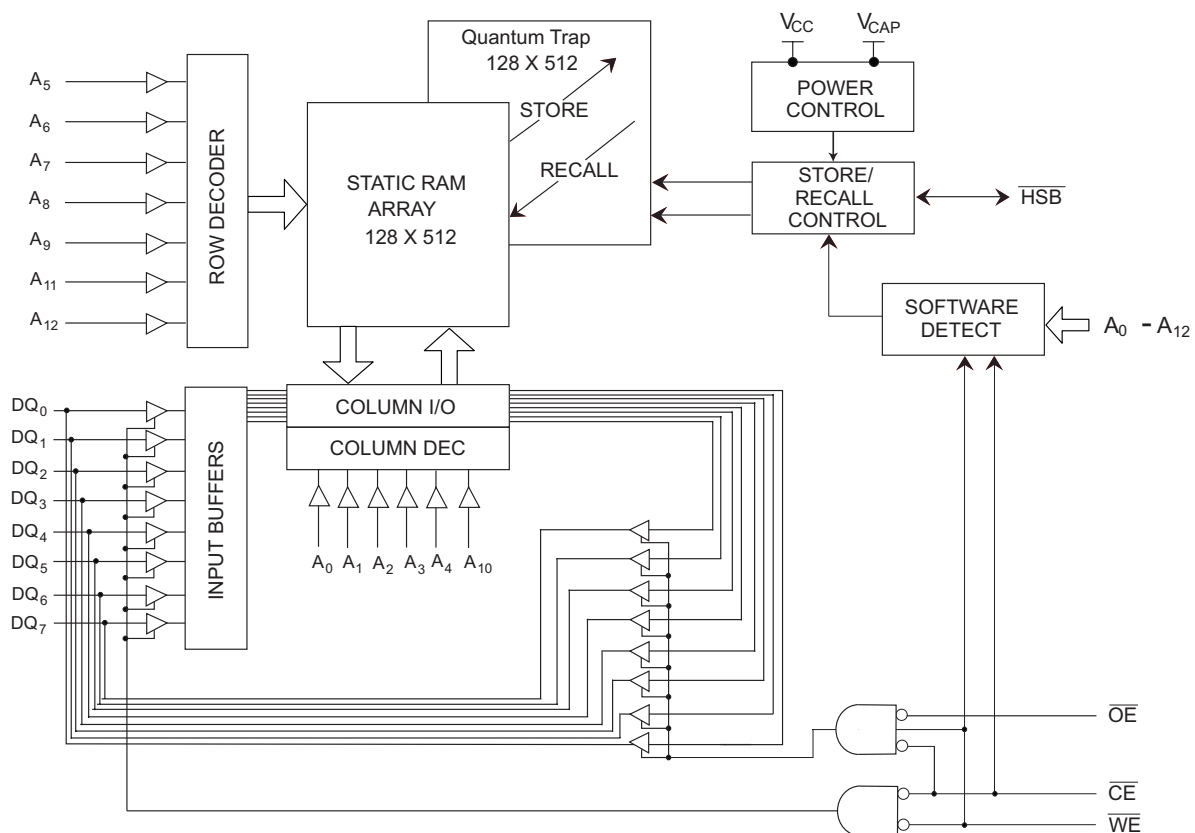
### Features

- 25 ns and 45 ns Access Times
- “Hands-off” Automatic *STORE* on Power Down with external 68 $\mu$ F capacitor
- *STORE* to QuantumTrap<sup>®</sup> Nonvolatile Elements is initiated by Software, Hardware or Autostore<sup>®</sup> on Power-down
- *RECALL* to SRAM Initiated by Software or Power-up
- Unlimited *READ*, *WRITE* and *RECALL* Cycles
- 10 mA Typical I<sub>CC</sub> at 200 ns Cycle Time
- 1,000,000 *STORE* Cycles to QuantumTrap
- 100-Year Data Retention to QuantumTrap
- Single 5V Operation  $\pm 10\%$
- Commercial Temperature
- SOIC Package
- RoHS Compliance

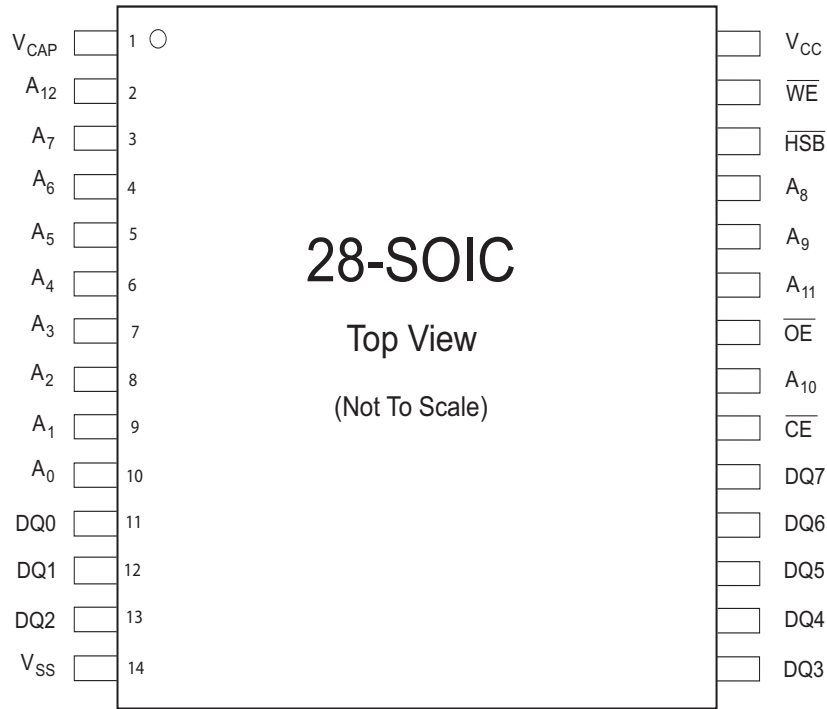
### Functional Description

The Cypress CY14E064L is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent, nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the *STORE* operation) takes place automatically at power down. On power-up, data is restored to the SRAM (the *RECALL* operation) from the nonvolatile memory. Both the *STORE* and *RECALL* operations are also available under software control. A hardware *STORE* may be initiated with HSB pin.

### Logic Block Diagram



**Pin Configurations**



**Pin Definitions**

Pin Name	I/O Type	Description
A <sub>0</sub> -A <sub>12</sub>	Input	<b>Address Inputs used to select one of the 8,192 bytes of the nvSRAM.</b>
DQ0-DQ7	Input/Output	<b>Bidirectional Data I/O lines.</b> Used as input or output lines depending on operation.
$\overline{WE}$	Input	<b>Write Enable Input, active LOW.</b> When selected <b>LOW</b> , enables data on the I/O pins to be written to the address location latched by the falling edge of $\overline{CE}$ .
$\overline{CE}$	Input	<b>Chip Enable Input, active LOW.</b> When <b>LOW</b> , selects the chip. When <b>HIGH</b> , deselects the chip.
$\overline{OE}$	Input	<b>Output Enable, active LOW.</b> The active <b>LOW</b> $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ <b>HIGH</b> causes the I/O pins to tri-state.
V <sub>SS</sub>	Ground	<b>Ground for the device.</b> Should be connected to ground of the system.
V <sub>CC</sub>	Power Supply	<b>Power Supply inputs to the device.</b>
$\overline{HSB}$	Input/Output	<b>Hardware Store Busy.</b> When low this output indicates a Hardware Store is in progress. When pulled low external to the chip it will initiate a nonvolatile STORE operation. A weak internal pull-up resistor keeps this pin high if not connected. (Connection Optional)
V <sub>CAP</sub>	Power Supply	<b>Autostore<sup>®</sup> Capacitor.</b> Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.

### Device Operation

The CY14E064L nvSRAM is made up of two functional components paired in the same physical cell. These are a SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM can be transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture allows all cells to be stored and recalled in parallel. During the STORE and RECALL operations SRAM READ and WRITE operations are inhibited. The CY14E064L supports unlimited reads and writes just like a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to 1 million STORE operations.

### SRAM Read

The CY14E064L performs a READ cycle whenever  $\overline{CE}$  and  $\overline{OE}$  are low while  $\overline{WE}$  and HSB are high. The address specified on pins  $A_{0-12}$  determines which of the 8,192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of  $t_{AA}$  (READ cycle #1). If the READ is initiated by  $\overline{CE}$  or  $\overline{OE}$ , the outputs will be valid at  $t_{ACE}$  or at  $t_{DOE}$ , whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the  $t_{AA}$  access time without the need for transitions on any control input pins, and will remain valid until another address change or until  $\overline{CE}$  or  $\overline{OE}$  is brought high, or  $\overline{WE}$  or HSB is brought low.

### SRAM Write

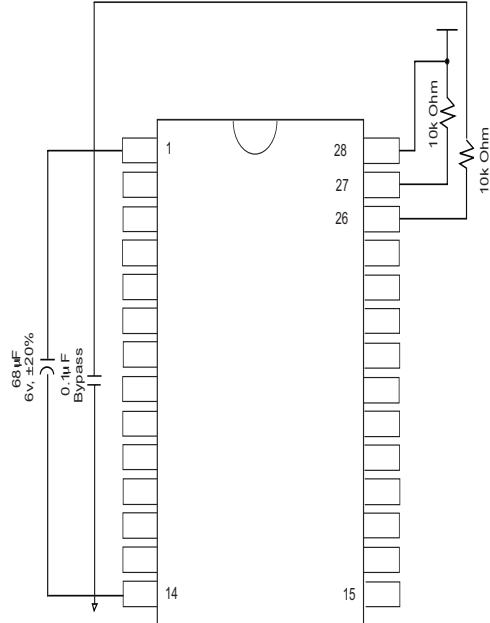
A WRITE cycle is performed whenever  $\overline{CE}$  and  $\overline{WE}$  are low and HSB is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either  $\overline{CE}$  or  $\overline{WE}$  goes high at the end of the cycle. The data on the common I/O pins  $I/O_{0-7}$  will be written into the memory if it is valid  $t_{SD}$  before the end of a  $\overline{WE}$  controlled WRITE or before the end of an  $\overline{CE}$  controlled WRITE. It is recommended that  $\overline{OE}$  be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If  $\overline{OE}$  is left low, internal circuitry will turn off the output buffers  $t_{HZWE}$  after  $\overline{WE}$  goes low.

### AutoStore Operation

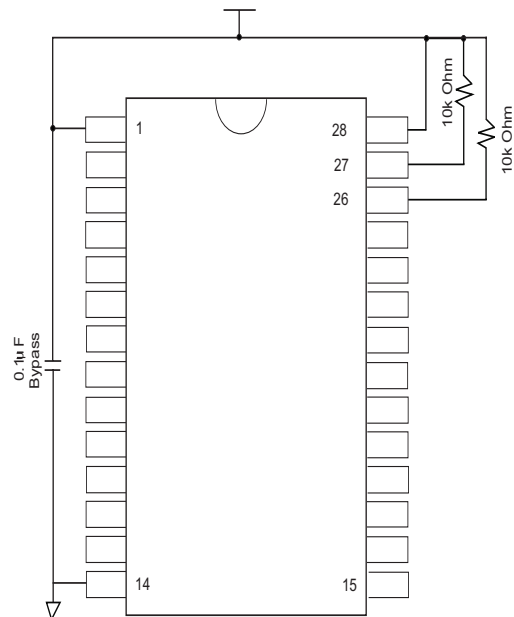
The CY14E064L stores data to nvSRAM using one of three storage operations. These three operations are Hardware Store, activated by HSB, Software Store, activated by an address sequence, and AutoStore, on device power down. AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14E064L.

During normal operation, the device will draw current from  $V_{CC}$  to charge a capacitor connected to the  $V_{CAP}$  pin. This stored charge will be used by the chip to perform a single STORE operation. If the voltage on the  $V_{CC}$  pin drops below  $V_{SWITCH}$ , the part will automatically disconnect the  $V_{CAP}$  pin from  $V_{CC}$ . A STORE operation will be initiated with power provided by the  $V_{CAP}$  capacitor.

Figure 1 shows the proper connection of the storage capacitor ( $V_{CAP}$ ) for automatic store operation. Refer to the DC Characteristics table for the size of  $V_{CAP}$ . The voltage on the  $V_{CAP}$  pin is driven to 5V by a charge pump internal to the chip. A pull-up should be placed on  $\overline{WE}$  to hold it inactive during power-up.



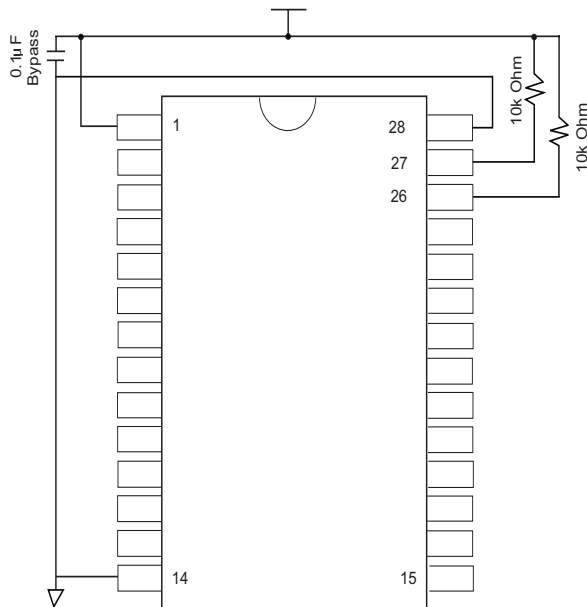
**Figure 1. AutoStore® Mode**



**Figure 2. System Power Mode**

In system power mode both  $V_{CC}$  and  $V_{CAP}$  are connected to the +5V power supply without the 68- $\mu$ F capacitor. In this mode the AutoStore function of the CY14E064L will operate on the stored system charge as power goes down. The user must, however, guarantee that  $V_{CC}$  does not drop below 3.6V during the 10-ms STORE cycle.

If an automatic STORE on power loss is not required, then  $V_{CC}$  can be tied to ground and +5V applied to  $V_{CAP}$  (Figure 3). This is the AutoStore Inhibit mode, in which the AutoStore function is disabled. If the CY14E064L is operated in this configuration, references to  $V_{CC}$  should be changed to  $V_{CAP}$  throughout this data sheet. In this mode, STORE operations may be triggered through software control or the HSB pin. It is not permissible to change between these three options “on the fly”.



**Figure 3. AutoStore Inhibit Mode**

To reduce unnecessary nonvolatile stores, AutoStore and Hardware Store operations will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. The HSB signal can be monitored by the system to detect an AutoStore cycle is in progress.

### Hardware STORE (HSB) Operation

The CY14E064L provides the  $\overline{HSB}$  pin for controlling and acknowledging the STORE operations. The  $\overline{HSB}$  pin can be used to request a hardware STORE cycle. When the  $\overline{HSB}$  pin is driven low, the CY14E064L will conditionally initiate a STORE operation after  $t_{DELAY}$ . An actual STORE cycle will only begin if a WRITE to the SRAM took place since the last STORE or RECALL cycle. The  $\overline{HSB}$  pin also acts as an open-drain driver that is internally driven low to indicate a busy condition while the STORE (initiated by any means) is in progress.

SRAM READ and WRITE operations that are in progress when  $\overline{HSB}$  is driven low by any means are given time to complete before the STORE operation is initiated. After  $\overline{HSB}$  goes low, the CY14E064L will continue SRAM operations for

$t_{DELAY}$ . During  $t_{DELAY}$ , multiple SRAM READ operations may take place. If a WRITE is in progress when  $\overline{HSB}$  is pulled low it will be allowed a time,  $t_{DELAY}$ , to complete. However, any SRAM WRITE cycles requested after  $\overline{HSB}$  goes low will be inhibited until  $\overline{HSB}$  returns high.

The  $\overline{HSB}$  pin can be used to synchronize multiple CY14E064L while using a single larger capacitor. To operate in this mode the  $\overline{HSB}$  pin should be connected together to the  $\overline{HSB}$  pins from the other CY14E064L. An external pull-up resistor to +5V is required since  $\overline{HSB}$  acts as an open-drain pull-down. The  $V_{CAP}$  pins from the other CY14E064L parts can be tied together and share a single capacitor. The capacitor size must be scaled by the number of devices connected to it. When any one of the CY14E064L detects a power loss and asserts  $\overline{HSB}$ , the common  $\overline{HSB}$  pin will cause all parts to request a STORE cycle (a STORE will take place in those CY14E064L that have been written since the last nonvolatile cycle).

During any STORE operation, regardless of how it was initiated, the CY14E064L will continue to drive the  $\overline{HSB}$  pin low, releasing it only when the STORE is complete. Upon completion of the STORE operation the CY14E064L will remain disabled until the  $\overline{HSB}$  pin returns high.

If  $\overline{HSB}$  is not used, it should be left unconnected.

### Hardware RECALL (Power-up)

During power-up, or after any low-power condition ( $V_{CC} < V_{SWITCH}$ ), an internal RECALL request will be latched. When  $V_{CC}$  once again exceeds the sense voltage of  $V_{SWITCH}$ , a RECALL cycle will automatically be initiated and will take  $t_{HRECALL}$  to complete.

If the CY14E064L is in a WRITE state at the end of power-up RECALL, the SRAM data will be corrupted. To help avoid this situation, a 10-Kohm resistor should be connected either between  $\overline{WE}$  and system  $V_{CC}$  or between  $\overline{CE}$  and system  $V_{CC}$ .

### Software STORE

Data can be transferred from the SRAM to the nonvolatile memory by a software address sequence. The CY14E064L software STORE cycle is initiated by executing sequential  $\overline{CE}$ -controlled READ cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no STORE or RECALL will take place.

To initiate the software STORE cycle, the following READ sequence must be performed:

1. Read address 0x0000, Valid READ
2. Read address 0x1555, Valid READ
3. Read address 0x0AAA, Valid READ
4. Read address 0x1FFF, Valid READ
5. Read address 0x10F0, Valid READ
6. Read address 0x0F0F, Initiate STORE cycle

The software sequence may be clocked with  $\overline{CE}$ -controlled READs or OE-controlled READs. Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that OE be low for the sequence to be valid. After the  $t_{STORE}$  cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

**Software RECALL**

Data can be transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of  $\overline{CE}$ -controlled READ operations must be performed:

1. Read address 0x0000, Valid READ
2. Read address 0x1555, Valid READ
3. Read address 0x0AAA, Valid READ
4. Read address 0x1FFF, Valid READ
5. Read address 0x10F0, Valid READ
6. Read address 0x0F0E, Initiate RECALL cycle

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the  $t_{RECALL}$  cycle time the SRAM will once again be ready for READ and WRITE operations. The RECALL operation in no way alters the data in the nonvolatile elements.

**Data Protection**

The CY14E064L protects data from corruption during low-voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low voltage condition is detected when  $V_{CC} \leq V_{SWITCH}$ . If the CY14E064L is in a WRITE mode (both  $\overline{CE}$  and  $\overline{WE}$  low) at power-up, after a RECALL, or after a STORE, the WRITE will be inhibited until a negative transition on  $\overline{CE}$  or  $\overline{WE}$  is detected. This protects against inadvertent writes during power-up or brown-out conditions.

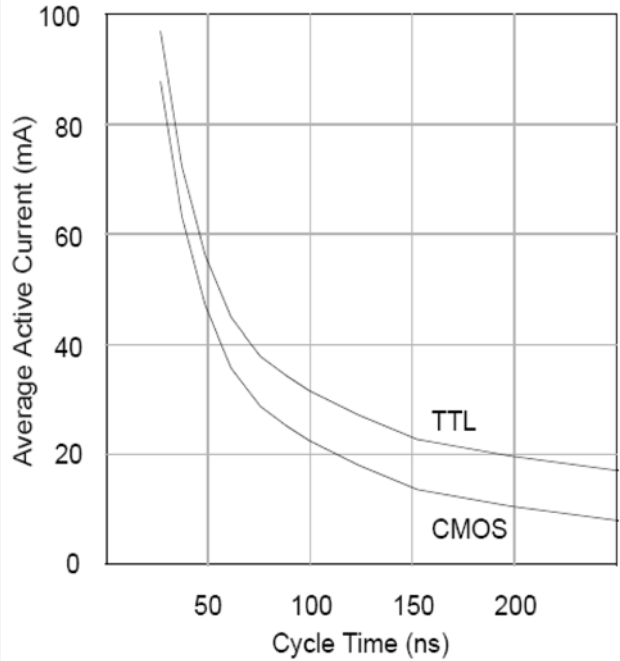
**Noise Considerations**

The CY14E064L is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1  $\mu F$  connected between  $V_{CC}$  and  $V_{SS}$ , using leads and traces that are as short as possible. As with all high-speed CMOS ICs, careful routing of power, ground, and signals will reduce circuit noise.

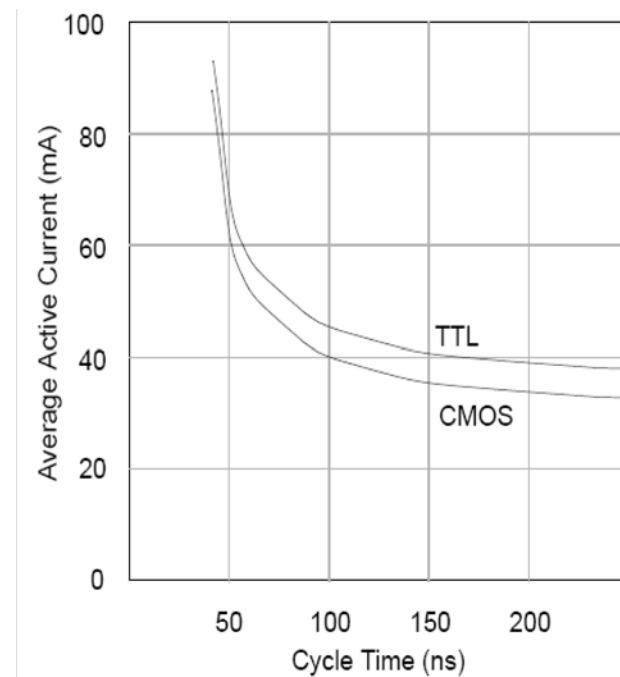
**Low Average Active Power**

CMOS technology provides the CY14E064L the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. Figure 4 shows the relationship between  $I_{CC}$  and READ/WRITE cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range,  $V_{CC} = 5.5V$ , 100% duty cycle on chip enable). Only standby current is drawn when the chip is disabled. The overall average current drawn by the CY14E064L depends on the following items:

1. The duty cycle of chip enable.
2. The overall cycle rate for accesses.
3. The ratio of READs to WRITES.
4. CMOS vs. TTL Input Levels.
5. The operating temperature.
6. The  $V_{CC}$  level.
7. I/O loading.



**Figure 4. Current vs. Cycle Time (READ)**



**Figure 5. Current vs. Cycle Time (WRITE)**

**Preventing STOREs**

The STORE function can be disabled on the fly by holding  $\overline{\text{HSB}}$  high with a driver capable of sourcing 30 mA at a  $V_{\text{OH}}$  of at least 2.2V, as it will have to overpower the internal pull-down device that drives HSB low for 20  $\mu\text{s}$  at the onset of a STORE.

When the CY14E064L is connected for AutoStore operation (system  $V_{\text{CC}}$  connected to  $V_{\text{CC}}$  and a 68- $\mu\text{F}$  capacitor on  $V_{\text{CAP}}$ ) and  $V_{\text{CC}}$  crosses  $V_{\text{SWITCH\_on}}$  the way down, the CY14E064L will attempt to pull HSB low; if HSB doesn't actually get below  $V_{\text{IL}}$ , the part will stop trying to pull HSB low and abort the STORE attempt.

**Table 1. Hardware Mode Selection**

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{HSB}}$	A12-A0	Mode	I/O	Power
H	X	H	X	Not Selected	Output High-Z	Standby
L	H	H	X	Read SRAM	Output Data	Active
L	L	H	X	Write SRAM	Input Data	Active
X	X	L	X	Nonvolatile STORE	Output High-Z	$I_{\text{CC2}}$
L	H	H	0000 1555 0AAA 1FFF 10F0 0F0F	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output Data Output Data Output Data Output Data Output Data Output High Z	Active $I_{\text{CC2}}$
L	H	H	0000 1555 0AAA 1FFF 10F0 0F0E	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output Data Output Data Output Data Output Data Output Data Output High Z	Active

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied..... -55°C to +125°C
- Supply Voltage on V<sub>CC</sub> Relative to GND..... -0.5V to 7.0V
- Voltage Applied to Outputs in High-Z State ..... -0.5V to V<sub>CC</sub> + 0.5V
- Input Voltage ..... -0.5V to V<sub>CC</sub>+0.5V
- Transient Voltage (<20 ns) on Any Pin to Ground Potential..... -2.0V to V<sub>CC</sub> + 2.0V

- Package Power Dissipation Capability (T<sub>A</sub> = 25°C) ..... 1.0W
- Surface Mount Lead Soldering Temperature (3 Seconds)..... +260°C
- Output Short Circuit Current<sup>[1]</sup>..... 15 mA
- Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)
- Latch-up Current..... > 200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	4.5V to 5.5V

**DC Electrical Characteristics** Over the Operating Range (V<sub>CC</sub> = 4.5V to 5.5V) <sup>[2]</sup>

Parameter	Description	Test Conditions	Min.	Max.	Unit
I <sub>CC1</sub>	Average V <sub>CC</sub> Current	t <sub>RC</sub> = 25 ns t <sub>RC</sub> = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads. I <sub>OUT</sub> = 0mA.	Commercial	85 65	mA mA
I <sub>CC2</sub>	Average V <sub>CC</sub> Current during STORE	All Inputs Don't Care, V <sub>CC</sub> = Max. Average current for duration t <sub>STORE</sub>		3	mA
I <sub>CC3</sub>	Average V <sub>CC</sub> Current at t <sub>AVAV</sub> = 200 ns, 5V, 25°C typical	WE > (V <sub>CC</sub> - 0.2). All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads.		10	mA
I <sub>CC4</sub>	Average V <sub>CAP</sub> Current during AutoStore Cycle	All Inputs Don't Care, V <sub>CC</sub> = Max. Average current for duration t <sub>STORE</sub>		2	mA
I <sub>SB</sub>	V <sub>CC</sub> Standby Current	CE > (V <sub>CC</sub> - 0.2). All others V <sub>IN</sub> < 0.2V or > (V <sub>CC</sub> - 0.2V). Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0MHz.		2.5	mA
I <sub>IX</sub>	Input Leakage Current	V <sub>CC</sub> = Max., V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	+1	μA
I <sub>OZ</sub>	Off-State Output Leakage Current	V <sub>CC</sub> = Max., V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> . CE or OE > V <sub>IH</sub>	-5	+5	μA
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW Voltage		V <sub>SS</sub> - 0.5	0.8	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OUT</sub> = -2 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OUT</sub> = 4 mA		0.4	V

**Capacitance** <sup>[3]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz,	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 0 to 3.0 V	7	pF

**Notes:**

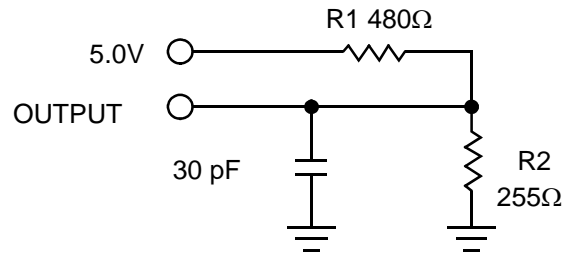
1. Outputs shorted for no more than one second. No more than one output shorted at a time.
2. Typical conditions for the Active Current shown on the front page of the data sheet are average values at 25°C (room temperature), and V<sub>CC</sub> = 5V. Not 100% tested.
3. These parameters are guaranteed but not tested.



**Thermal Resistance** <sup>[3]</sup>

Parameter	Description	Test Conditions	28-SOIC	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	TBD	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		TBD	°C/W

**AC Test Loads**



**AC Test Conditions**

Input Pulse Levels ..... 0 V to 3 V  
 Input Rise and Fall Times (10% - 90%) ..... ≤5 ns  
 Input and Output Timing Reference Levels ..... 1.5 V



**AC Switching Characteristics**

Parameter		Description	25ns part		45ns part		Unit
Cypress Parameter	Alt.		Min.	Max.	Min.	Max.	
<b>SRAM Read Cycle</b>							
t <sub>ACE</sub>	t <sub>ACS</sub>	Chip Enable Access Time		25		45	ns
t <sub>RC</sub> <sup>[4]</sup>	t <sub>RC</sub>	Read Cycle Time	25		45		ns
t <sub>AA</sub> <sup>[5]</sup>	t <sub>AA</sub>	Address Access Time		25		45	ns
t <sub>DOE</sub>	t <sub>OE</sub>	Output Enable to Data Valid		10		20	ns
t <sub>OHA</sub> <sup>[5]</sup>	t <sub>OH</sub>	Output Hold After Address Change	5		5		ns
t <sub>LZCE</sub> <sup>[6]</sup>	t <sub>LZ</sub>	Chip Enable to Output Active	5		5		ns
t <sub>HZCE</sub> <sup>[6]</sup>	t <sub>HZ</sub>	Chip Disable to Output Inactive		10		12	ns
t <sub>LZOE</sub> <sup>[6]</sup>	t <sub>OLZ</sub>	Output Enable to Output Active	0		0		ns
t <sub>HZOE</sub> <sup>[6]</sup>	t <sub>OHZ</sub>	Output Disable to Output Inactive		10		12	ns
t <sub>PU</sub> <sup>[3]</sup>	t <sub>PA</sub>	Chip Enable to Power Active	0		0		ns
t <sub>PD</sub> <sup>[3]</sup>	t <sub>PS</sub>	Chip Disable to Power Standby		25		45	ns
<b>SRAM Write Cycle</b>							
t <sub>WC</sub>	t <sub>WC</sub>	Write Cycle Time	25		45		ns
t <sub>PWE</sub>	t <sub>WP</sub>	Write Pulse Width	20		30		ns
t <sub>SCE</sub>	t <sub>CW</sub>	Chip Enable To End of Write	20		30		ns
t <sub>SD</sub>	t <sub>DW</sub>	Data Set-Up to End of Write	10		15		ns
t <sub>HD</sub>	t <sub>DH</sub>	Data Hold After End of Write	0		0		ns
t <sub>AW</sub>	t <sub>AW</sub>	Address Set-Up to End of Write	20		30		ns
t <sub>SA</sub>	t <sub>AS</sub>	Address Set-Up to Start of Write	0		0		ns
t <sub>HA</sub>	t <sub>WR</sub>	Address Hold After End of Write	0		0		ns
t <sub>HZWE</sub> <sup>[6,7]</sup>	t <sub>WZ</sub>	Write Enable to Output Disable		10		14	ns
t <sub>LZWE</sub> <sup>[6]</sup>	t <sub>OW</sub>	Output Active after End of Write	5		5		ns

**AutoStore/Power-Up RECALL**

Parameter	Description	CY14E064L		Unit
		Min.	Max.	
t <sub>HRECALL</sub> <sup>[8]</sup>	Power-Up RECALL Duration		550	μs
t <sub>STORE</sub> <sup>[9]</sup>	STORE Cycle Duration		10	ms
V <sub>SWITCH</sub>	Low Voltage Trigger Level	4.0	4.5	V
t <sub>VCCRISE</sub>	V <sub>CC</sub> Rise Time	150		μs

**Notes:**

4. WE must be HIGH during SRAM Read Cycles.
5. Device is continuously selected with CE and OE both Low.
6. Measured ±200mV from steady state output voltage.
7. If WE is Low when CE goes Low, the outputs remain in the high-impedance state.
8. t<sub>HRECALL</sub> starts from the time V<sub>CC</sub> rises above V<sub>SWITCH</sub>.
9. If an SRAM Write has not taken place since the last non-volatile cycle, no STORE will take place.

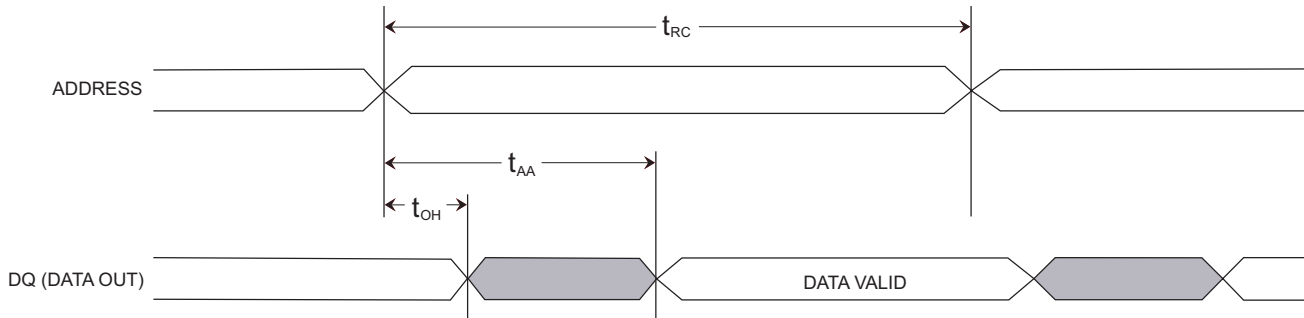
**Software Controlled STORE/RECALL Cycle** <sup>[10,11]</sup>

Parameter	Description	25ns part		45ns part		Unit
		Min.	Max.	Min.	Max.	
t <sub>RC</sub>	STORE/RECALL Initiation Cycle Time	25		45		ns
t <sub>AS</sub>	Address Set-Up Time	0		0		ns
t <sub>CW</sub>	Clock Pulse Width	20		30		ns
t <sub>GLAX</sub>	Address Hold Time	20		20		ns
t <sub>RECALL</sub>	RECALL Duration		20		20	μs

**Hardware STORE Cycle**

Parameter	Description	CY14E064L		Unit
		Min	Max	
t <sub>STORE</sub> <sup>[6]</sup>	STORE Cycle Duration		10	ms
t <sub>DELAY</sub> <sup>[12]</sup>	Time allowed to complete SRAM Cycle	1		μs
t <sub>RESTORE</sub> <sup>[13]</sup>	Hardware STORE High to Inhibit Off		700	ns
t <sub>HLHX</sub>	Hardware STORE Pulse Width	15		ns
t <sub>HLBL</sub>	Hardware STORE Low to STORE Busy		300	ns

**Switching Waveforms**

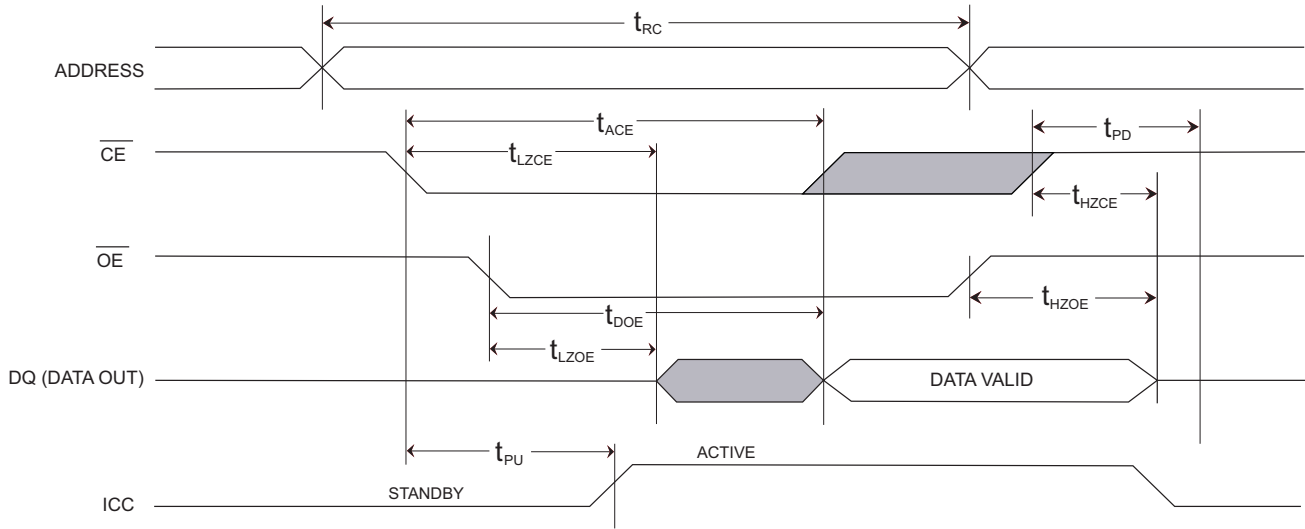


**Figure 6. SRAM Read Cycle #1: Address Controlled** <sup>[4, 5, 14]</sup>

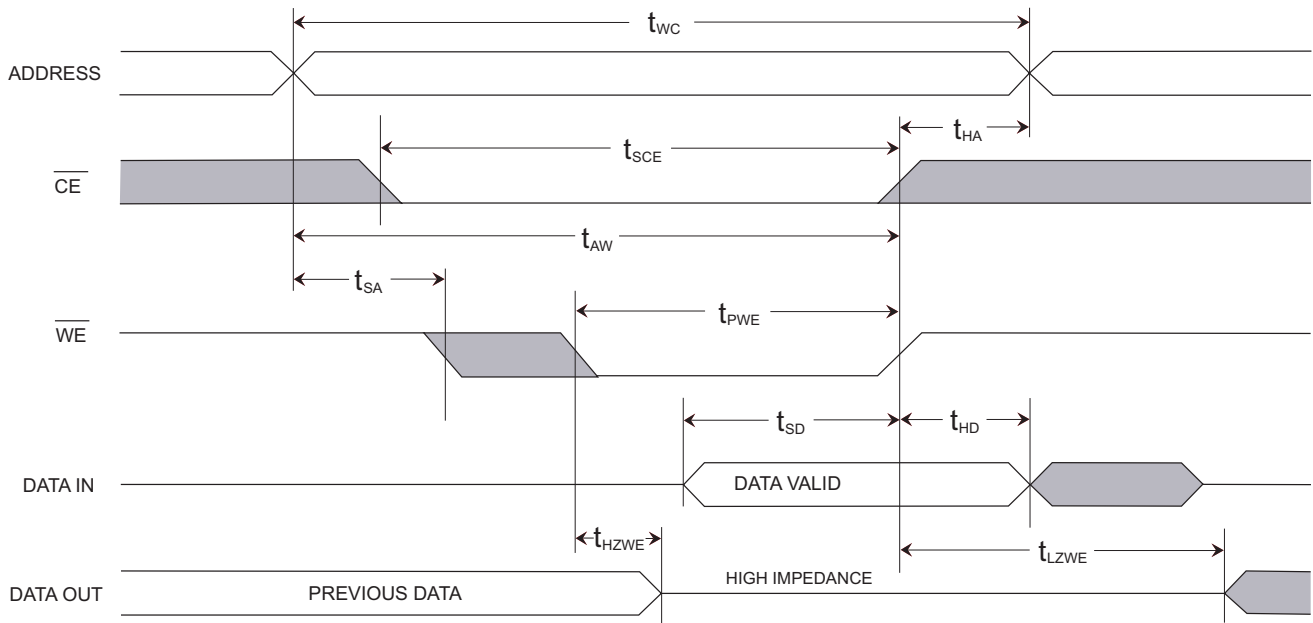
**Notes:**

- 10. The software sequence is clocked with  $\overline{CE}$  controlled READs.
- 11. The six consecutive addresses must be read in the order listed in the Mode Selection table.  $\overline{WE}$  must be HIGH during all six consecutive cycles.
- 12. Read and Write cycles in progress before HSB are given this amount of time to complete.
- 13. t<sub>RESTORE</sub> is only applicable after t<sub>STORE</sub> is complete.
- 14. HSB must remain HIGH during READ and WRITE cycles.

**Switching Waveforms (continued)**



**Figure 7. SRAM Read Cycle #2:  $\overline{\text{CE}}$  Controlled [4,14]**



**Figure 8. SRAM Write Cycle #1:  $\overline{\text{WE}}$  Controlled [14,15]**

**Note:**  
 15.  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  must be  $> V_{IH}$  during address transitions.

Switching Waveforms (continued)

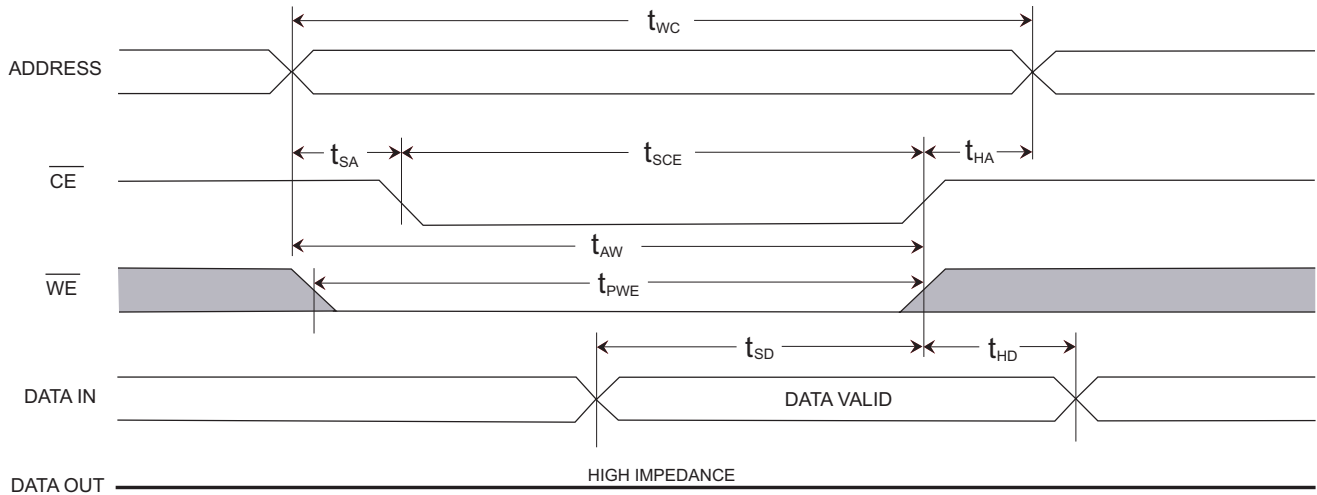


Figure 9. SRAM Write Cycle #2:  $\overline{CE}$  Controlled

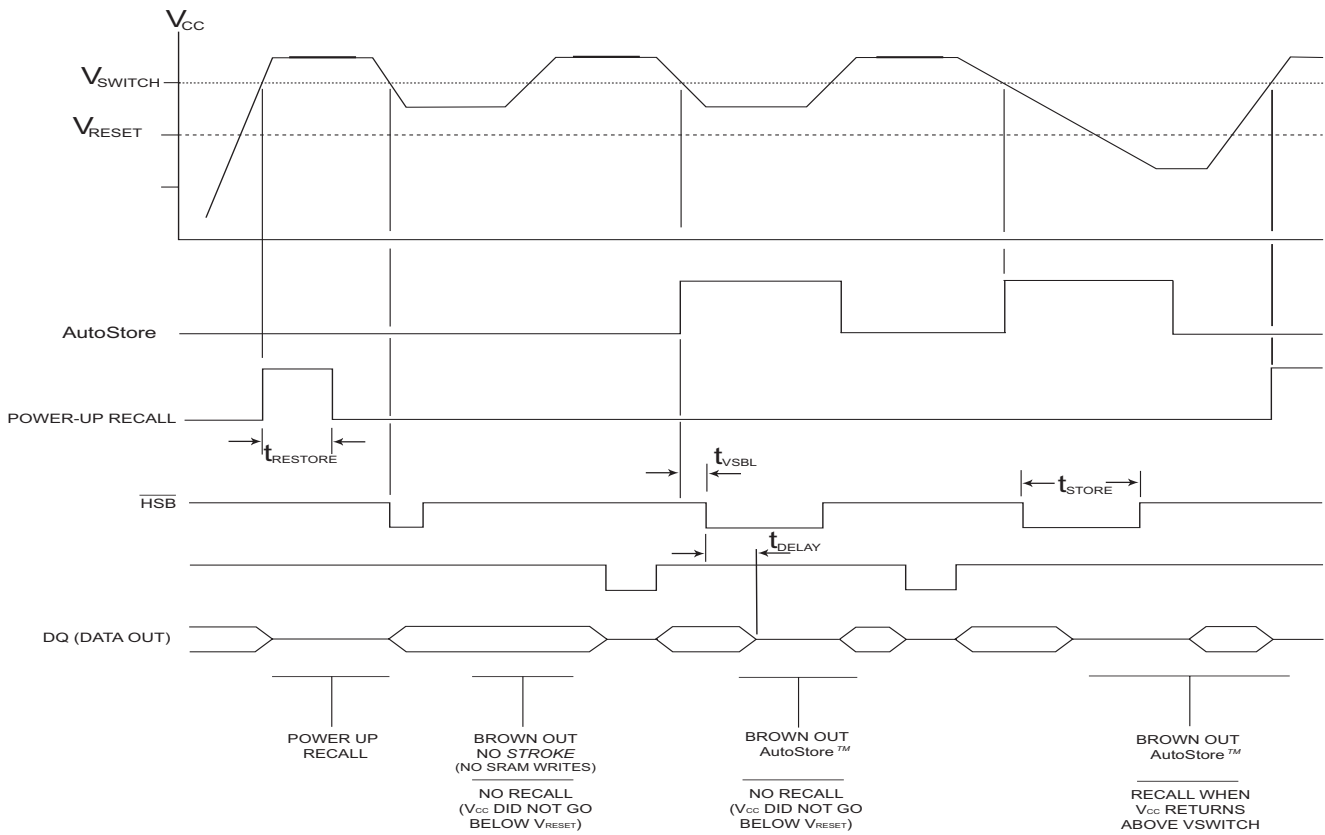
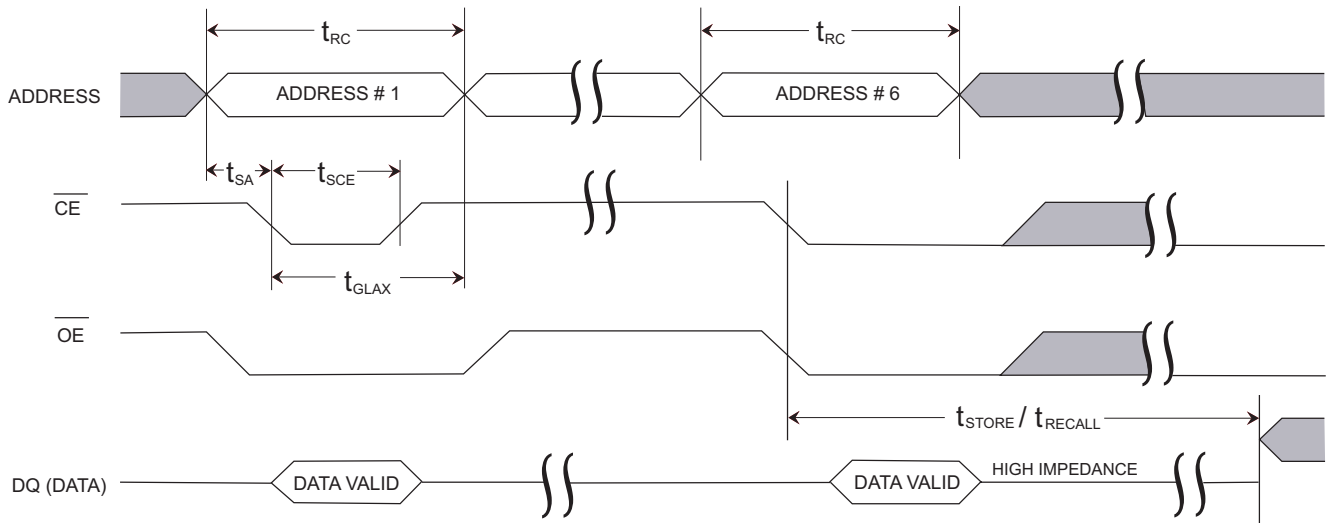
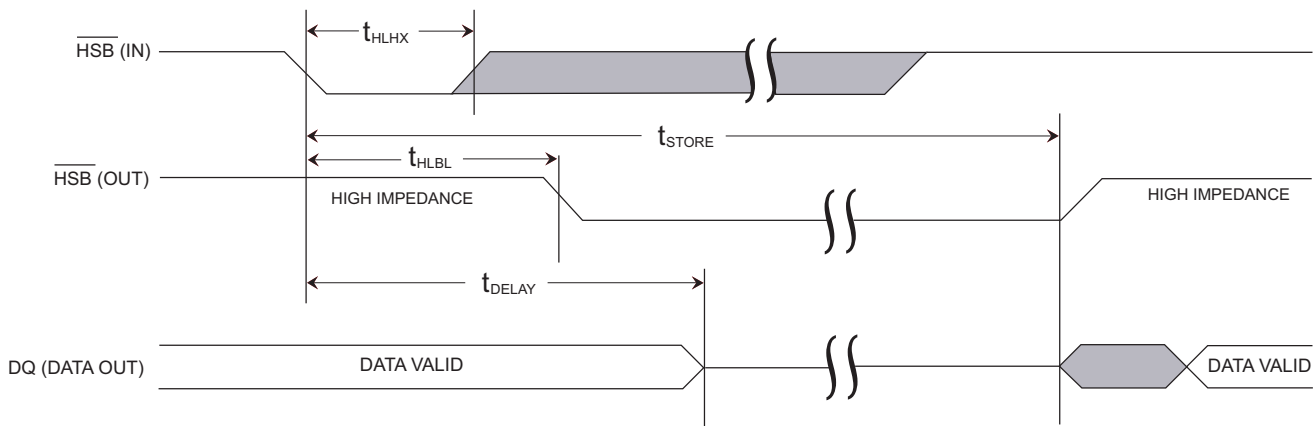


Figure 10. AutoStore/Power-Up RECALL

**Switching Waveforms (continued)**



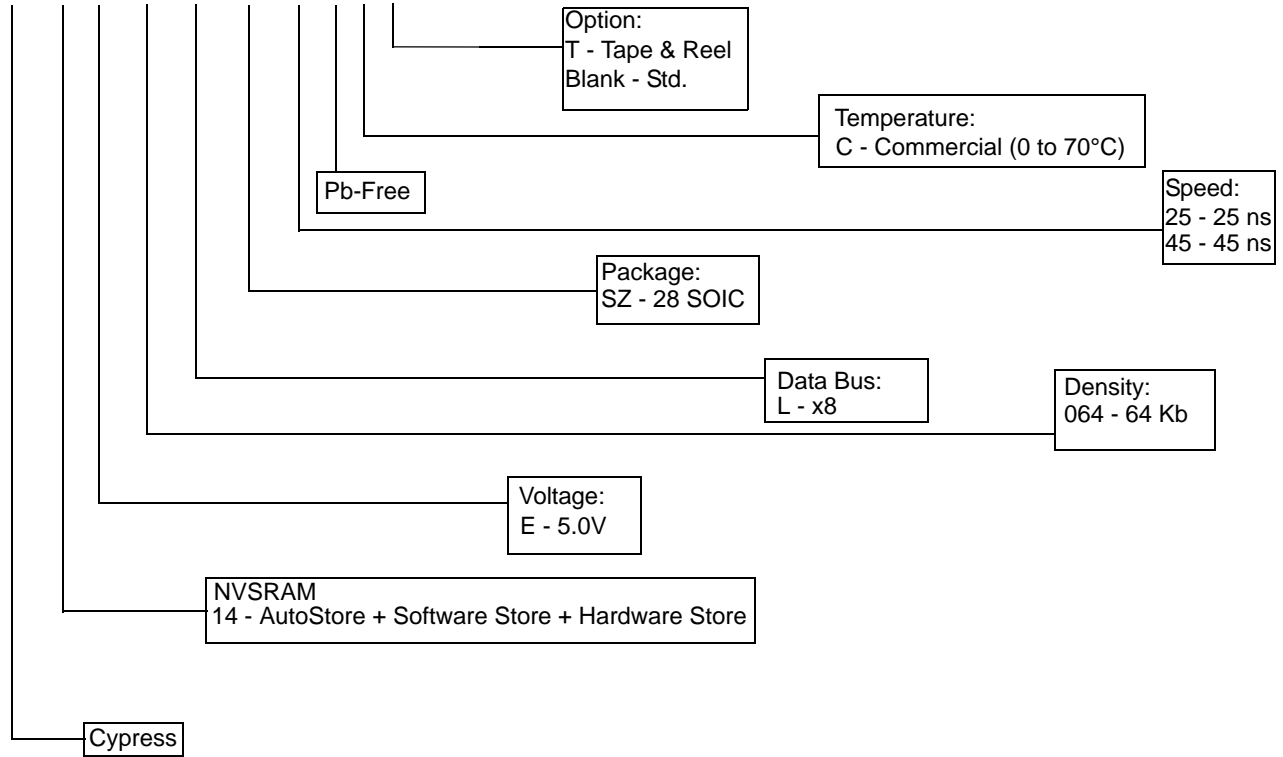
**Figure 11.  $\overline{CE}$ -controlled Software STORE/RECALL Cycle <sup>[11]</sup>**



**Figure 12. Hardware STORE Cycle**

**PART NUMBERING NOMENCLATURE**

**CY 14 E 064 L- SZ 25 X C T**

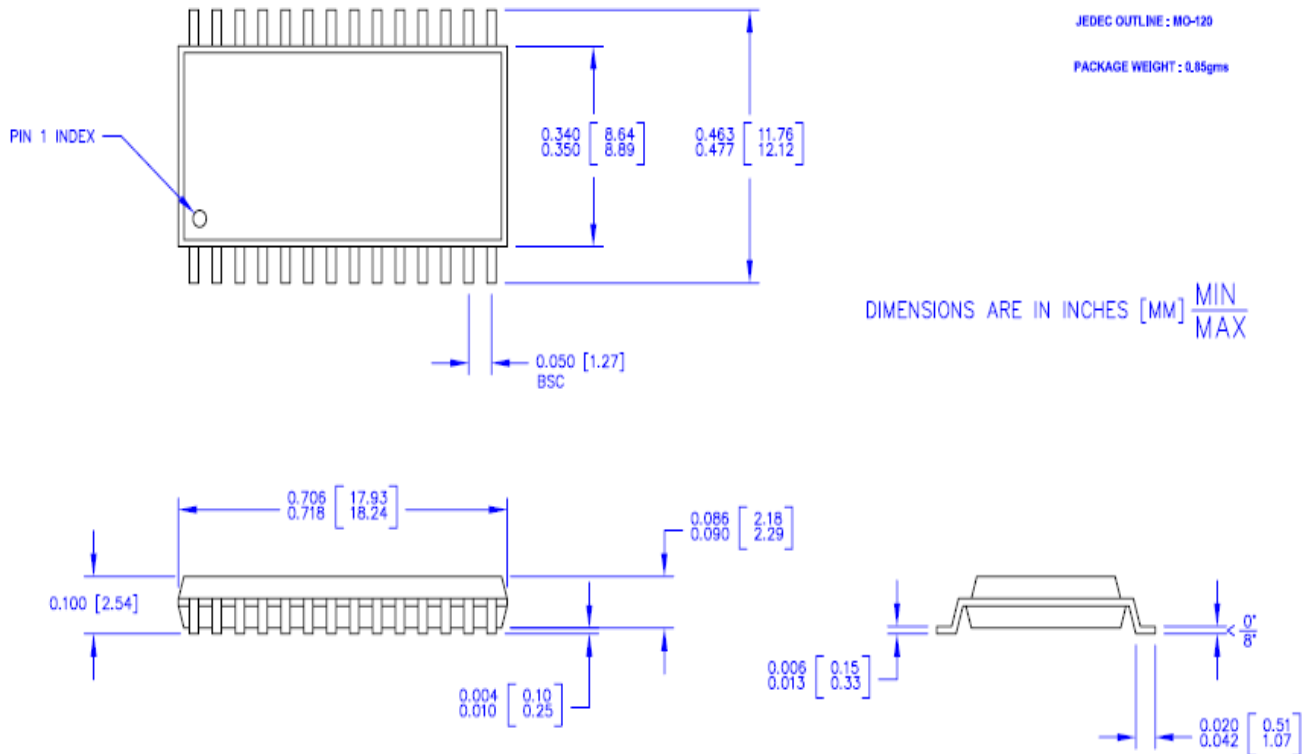


**Ordering Information**

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY14E064L-SZ25XCT	28-pin SOIC (Pb-Free)	Commercial
45	CY14E064L-SZ45XCT	28-pin SOIC (Pb-Free)	Commercial

**Package Diagrams**

**28-pin (350-Mil) SOIC (001-10395)**



001-10395 - \*\*

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**Document History Page**

Document Title: CY14E064L 64-Kbit (8K x 8) nvSRAM Document Number: 001-06543				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	427789	See ECN	TUP	New Data Sheet
*A	437321	See ECN	TUP	Show Data Sheet on Web
*B	472053	See ECN	TUP	Removed 55ns Speed Option Updated Part Numbering Nomenclature and Ordering Information
*C	503290	See ECN	PCI	Changed from Advance to Preliminary Changed the term "Unlimited" to "Infinite" Removed Industrial Grade mention Removed 35ns speed bin Removed Icc1 values from the DC table for 35 ns Industrial Grade Corrected $V_{IL}$ min. spec from $(V_{CC} - 0.5)$ to $(V_{SS} - 0.5)$ Removed all references pertaining to OE controlled "Software STORE and RECALL" operation Included Package Diagram for 28-pin (350 mil) SOIC Updated "Part Nomenclature Table" and "Ordering InformationTable"