AL4CX3650/AL4CX3660/ AL4CX3670/AL4CX3680/AL4CX3690

2K/ 4K/ 8K/ 16K/ 32K x 36 Synchronous FIFOs

Applications

- ATM switches
- Routers
- Cable modems
- Wireless base stations
- SONET(Synchronous Optical Network) multiplexers
- Multimedia systems
- TBC(Time Base Corrector)
- Hard Disk cache memory
- Buffer for Communications

Description

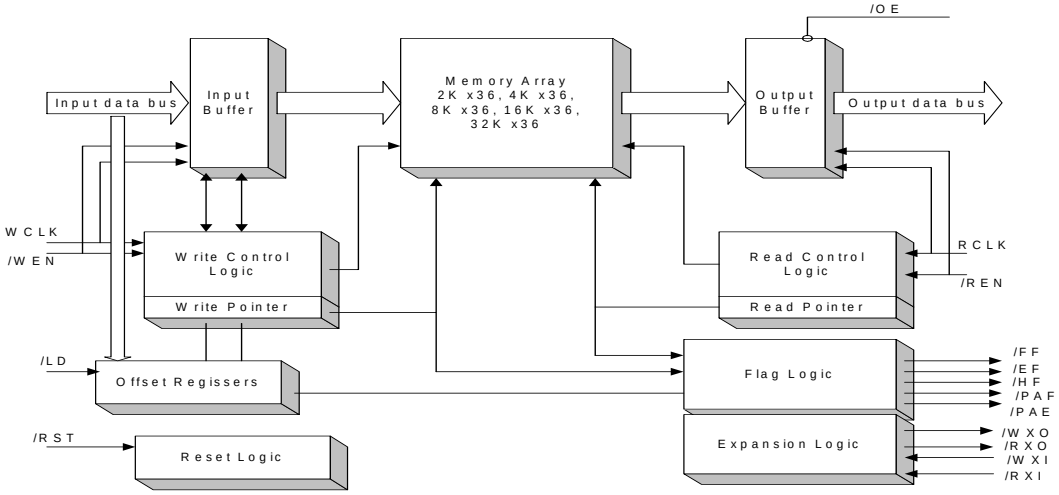
The AL4CX3650/ 3660/ 3670/ 3680/ 3690 FIFO (First In First Out) memory provides completely independent 36-bit bus width input and output port operation with flexible x36/ x18/ x9 Bus-Matching data flow control at a maximum speed of 166 MHz. The products are available in densities from 64K-bit to 1M-bit with word depths from 2K to 32K bit. Additional features of the AL4CX36x0 series include: fixed and programmable flags; low first word latency; partial reset; Endian select; expandable depth/width and optional first-word-fall-through. The AL4CX36x0 FIFO memory is AverLogic Technologies, latest products that is designed to buffer high-speed data for a wide range of application such as optical storage controllers, Networking Switches and various communication applications.

Features

- High performance, low-power, FIFO(First-In First-Out) memory
- 2K x36 bit I/O port (AL4CX3650)
- 4K x36 bit I/O port (AL4CX3660)
- 8K x36 bit I/O port (AL4CX3670)
- 16K x36 bit I/O port (AL4CX3680)
- 32K x36 bit I/O port (AL4CX3690)
- Maximum 166MHz operation
- Bus-Matching and Endian selection
- Fully independent input/output port access
- Empty, Full, Half Full and programmable Almost Empty, Almost Full flags
- Output enable control (data skipping)
- Partial Reset clears data
- Zero latency Retransmit
- Cascadable expansion in depth and width
- 3.3-volt power tolerant of 5-volt input
- Standard 128-pin TQFP

Ordering Information

Part number	AL4CX3650, AL4CX3660, AL4CX3670, AL4CX3680, AL4CX3690
Package	128-pin plastic TQFP
Power Supply	+3.3V±10%



AL4CX36x0 FIFO Block Diagram

The embedded memory array with built-in address decoder, pointer manager and state-of-the-art circuits provide an easy-to-use interface to serial read/write memory and offer a flexible way to manage memory in the system design.

The input port of the FIFO is controlled by a free running clock (WCLK), and an input enable (/WEN). The output port is controlled by another clock (RCLK) and an output enable (/REN). Data is read into or output from FIFO synchronous on every individual WRCK or RCLK clock cycle when /WEN or /REN is asserted respectively.

These FIFOs support selectable bus width up to 36bit for both input and output ports and can be configured as x36 to x36, x36 to x18, x36 to x9, x18 to x36 and x9 to x36 multiple input and output port bus width. This allows for easy conversion of the bus width between the input flow and output flow.

There are two fixed flags, Empty Flag/Output Ready and Full Flag/Input Ready, and two programmable flags, Almost-Empty and Almost-Full. The flags enable further manipulation of the synchronous control.

Multiple AL4CX36x0s can be cascaded to expand the storage depth or can be used in parallel to expand bus width.

The FIFOs are 3.3-volt devices with 5-volt input tolerance. And are available in the 128-pin thin quad flat Pack (TQFP Package).

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