Model 635

LVPECL or LVDS CLOCK OSCILLATOR

FEATURES

- Standard 7.5x5.0mm Surface Mount Footprint
- Differential LVPECL or LVDS Output
- **Fundamental or Overtone Crystal**
- Low Phase Jitter
- Frequency Range 19.44 – 250 MHz
- Frequency Stability, ±50 ppm Standard (±20 ppm, ±25 ppm and ±100 ppm available)
- +2.5Vdc or +3.3Vdc Operation
- Operating Temperature to –40°C to +85°C
- Output Enable Standard
- Tape & Reel Packaging
- **RoHS/Green Compliant (6/6)**

DESCRIPTION

The Model 635 is a ceramic packaged Clock oscillator offering reduced size and enhanced stability. The small size means it is perfect for any application. The enhanced stability means it is the perfect choice for today's communications applications that require tight frequency control.

ORDERING INFORMATION

635 □ □ □ □ □ □ □ M □ □ □ □

OUTPUT TYPE
P = PECL, Pin 1 Enable Pin 2 N.C. (standard)
L = LVDS, Pin 1 Enable Pin 2 N.C. (standard)
E = PECL, Pin 2 Enable Pin 1 N.C.
V = LVDS, Pin 2 Enable Pin 1 N.C.

FREQUENCY IN MHz
M - indicates MHz and decimal point. Frequency is recorded with minimum 4 significant digits to the right of the "M".

FREQUENCY STABILITY
6 = ± 20 ppm *
5 = ± 25 ppm
3 = ± 50 ppm (standard)
2 = ± 100 ppm (over -40°C to 85°C only)

SUPPLY VOLTAGE
2 = 2.5 Vdc
3 = 3.3 Vdc

OPERATING TEMPERATURE RANGE
C = -20°C to +70°C (standard)
I = -40°C to +85°C

* - Not available with 'I' temperature range. Consult factory for availability before ordering.

Example Part Number: 635P3C3155M5200

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• • • www.ctscorp.com • • •

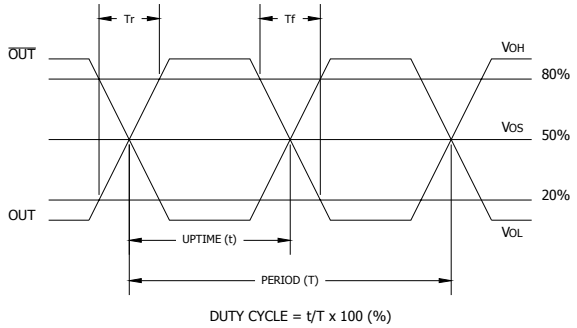
ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Absolute Maximums	Maximum Supply Voltage	V_{CC}	-	-0.5	-	5.0	V
	Storage Temperature	T_{STG}	-	-55	-	125	°C
	Frequency Range (See Note 1) LVPECL and LVDS	f_O	-	 19.44	-	 250	MHz
	Frequency Stability (See Note 2 and Ordering Information)	$\Delta f/f_O$	-	-	-	20, 25, 50 or 100	± ppm
	Operating Temperature Commercial Industrial	T_A	-	 -20 -40	 25	 70 85	°C
Electrical and Waveform Parameters	Supply Voltage	V_{CC}	± 5 %	2.38 3.14	2.5 3.3	2.63 3.47	V
	Supply Current LVPECL LVDS	I_{CC}	Maximum Load	 - -	 50 25	 100 60	mA
	Start Up Time	T_S	Application of V_{CC}	-	3	5	ms
	Phase Jitter Period Jitter	tjrms pjrms	Bandwidth 12 kHz - 20 MHz -	- -	- -	1 5	ps RMS ps RMS
	Enable Function Enable Input Voltage Disable Input Voltage	 V_{IH} V_{IL}	Standby Pin 1 or Pin 2 Logic '1', Output Enabled Pin 1 or Pin 2 Logic '0', Output Disabled	 0.7*V_{CC} -	 - -	 - 0.3*V_{CC}	V
	Disable Current	I_{IL}	Pin 1 or Pin 2 Logic '1' , Output Disabled	-	-	20	uA
	Enable Time	T_{PLZ}	Pin 1 or Pin 2 Logic '1'	-	-	5	ns
	LVPECL WAVEFORM						
	Output Load	R_L	-	-	50	-	Ohms
	Output Duty Cycle	SYM	@ V_{CC} - 1.3V	45	-	55	%
	Output Voltage Levels Logic '1' Level Logic '0' Level	 V_{OH} V_{OL}	 PECL Load PECL Load	 V_{CC} - 1.025V -	 - -	 - V_{CC} - 1.62V	V
	Rise and Fall Time f_O < 100 MHz f_O > 100 MHz	 T_R, T_F	 @ 20% - 80% Levels	 - -	 0.8 0.5	 1.0 0.6	ns
	LVDS WAVEFORM						
	Output Load	R_L	Between Outputs	-	100	-	Ohms
	Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
	Differential Output Voltage	V_{OD}	RL = 100 Ohms	247	350	454	mV
	Differential Output Error	-	-	-	-	50	mV
	Offset Voltage	V_{OS}	LVDS Load	1.125	1.25	1.375	V
	Offset Error	-	-	-	-	50	mV
	Output Voltage Levels Logic '1' Level Logic '0' Level	 V_{OH} V_{OL}	 LVDS Load LVDS Load	 - 0.9	 1.43 1.1	 1.6 -	V
	Rise and Fall Time f_O < 100 MHz f_O > 100 MHz	 T_R, T_F	 @ 20% - 80% Levels	 - -	 0.8 0.5	 1.0 0.6	ns

Notes:

1. For frequencies above 160 MHz consult factory for availability.
2. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 10 year aging.

PECL / LVDS OUTPUT WAVEFORM

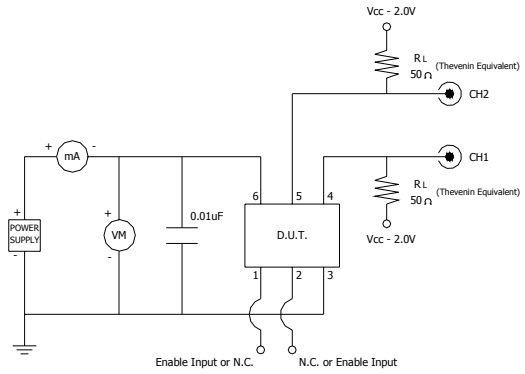


DUTY CYCLE = t/T x 100 (%)

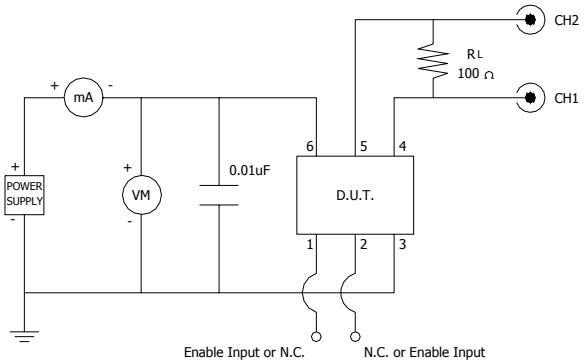
ENABLE TRUTH TABLE

PIN 1 or PIN 2	PIN 4 / PIN 5
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

TEST CIRCUIT, PECL LOAD

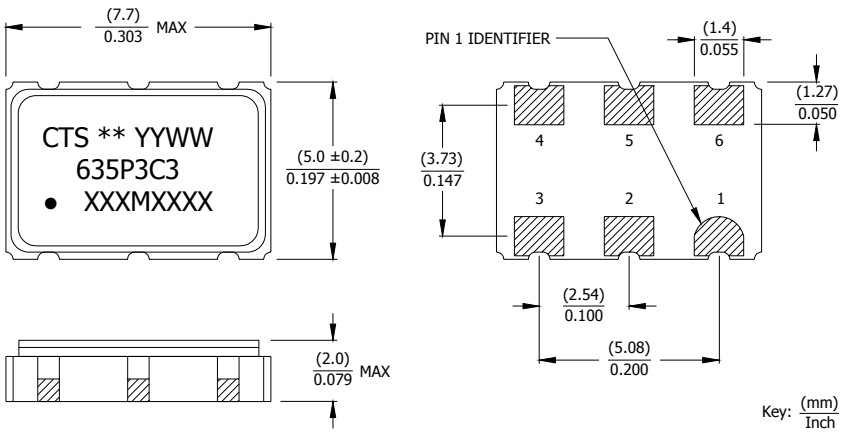


TEST CIRCUIT, LVDS LOAD



MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



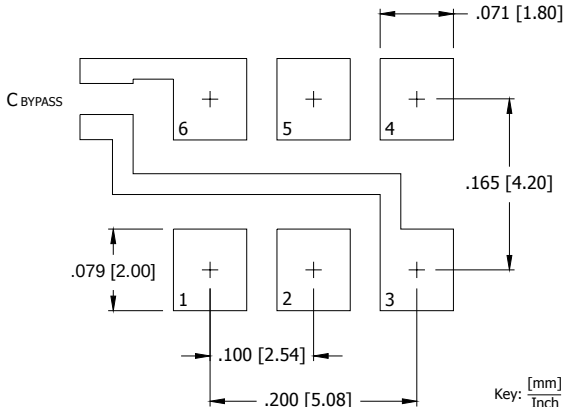
MARKING INFORMATION

1. ** - Manufacturing Site Code.
2. YYWW – Date code, YY – year, WW – week.
3. Truncated CTS part number.
4. XXXMXXXX - Frequency marked with 4 significant digits after the 'M'.

NOTES

1. Termination pads (e4), barrier-plating is nickel (Ni) with gold (Au) flash plate.
2. Reflow conditions per JEDEC J-STD-020.

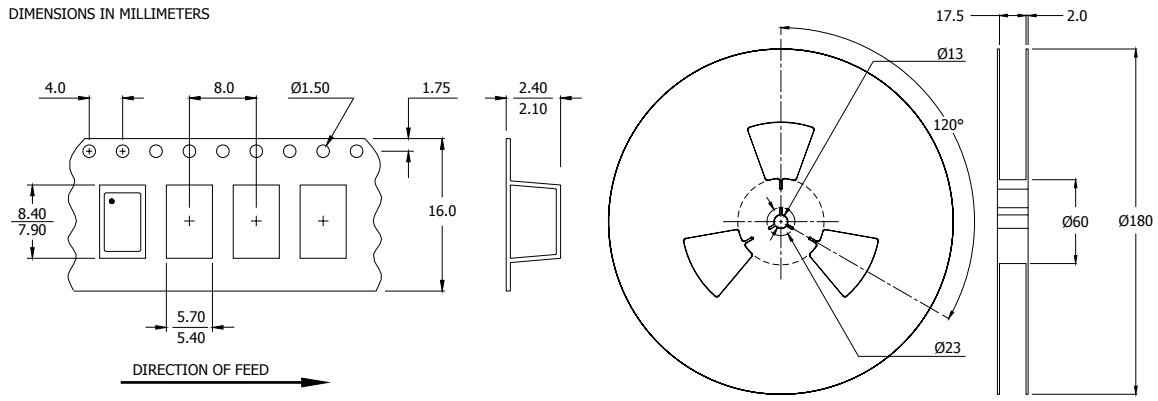
SUGGESTED SOLDER PAD GEOMETRY



D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	EOH or N.C.	Enable (std) or optional No Connect
2	EOH or N.C.	No Connect (std) or optional Enable
3	GND	Circuit & Package Ground
4	Output	RF Output
5	Output	Complimentary RF Output
6	V_{CC}	Supply Voltage

TAPE AND REEL INFORMATION



Device quantity is 1,000 pieces per 180mm reel.

ENVIRONMENTAL SPECIFICATIONS

Temperature Cycle:	400 cycles from –55°C to +125°C, 10 minute dwell at each temperature, 1 minute transfer time between temperatures.
Mechanical Shock:	1,500g's, 0.5mS duration, ½ sinewave, 3 shocks each direction along 3 mutually perpendicular planes (18 total shocks).
Sinusoidal Vibration:	0.06 inches double amplitude, 10 to 55 Hz and 20g's, 55 to 2,000 Hz, 3 cycles each in 3 mutually perpendicular planes (9 times total).
Gross Leak:	No leak shall appear while immersed in an FC40 or equivalent liquid at +125°C for 20 seconds.
Fine Leak:	Mass spectrometer leak rates less than $2x10^{-8}$ ATM cc/sec air equivalent.
Resistance to Solder Heat:	Product must survive 3 reflows of +260°C peak, 10 seconds maximum.
High Temperature Operating Bias:	2,000 hours at +125°C, maximum bias, disregarding frequency shift.
Frequency Aging:	1,000 hours at +85°C, full bias, less than ±5 ppm shift.
Moisture Sensitivity Level:	Level 1 per JEDEC J-STD-020.

QUALITY AND RELIABILITY

Quality systems meet or exceed the requirements of ISO 9000:2000 standards.