RNA51xx Series

CMOS system–RESET IC

REJ03D0505-0300
Rev.3.00
Oct 10, 2008

General Description

The RNA51xx series provide system reset signal for microprocessor and electrical systems.
Threshold voltage is 1.4 V, 2.6 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V, 4.4 V, 4.5 V, 4.6 V, 5.0 V and accuracy is ±1.0%.
The reset output delay time can be set by external capacitor connected to CD pin.
Manual reset input is available and input resistance is 2 MΩ typ.
This series have two output types (active-low CMOS output and active-low open-drain output).

Features

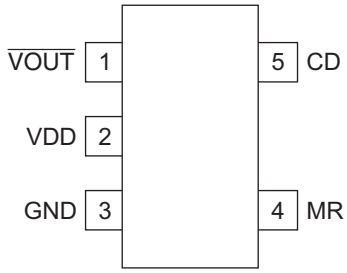
- Threshold voltage: 1.4 V, 2.6 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V, 4.4 V, 4.5 V, 4.6 V, 5.0 V
- Threshold voltage accuracy: ±1.0%
- Threshold voltage hysteresis: 5% typ.
- Low supply current: 0.7 µA typ.
- Capacitor-adjustable output delay time
- Manual reset
- $\overline{\text{VOUT}}$ CMOS output, or open-drain output
- 5-pin SOT-23 package
- Temperature range: –40°C to 85°C
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
RNA51A26FLPEL	MPAK-5pin	PLSP0005ZB-A	LP	EL (3,000pcs/Reel)
RNA51A27FLPEL	MPAK-5pin	PLSP0005ZB-A	LP	EL (3,000pcs/Reel)
RNA51A28FLPEL	MPAK-5pin	PLSP0005ZB-A	LP	EL (3,000pcs/Reel)
RNA51A29FLPEL	MPAK-5pin	PLSP0005ZB-A	LP	EL (3,000pcs/Reel)
RNA51A30FLPEL	MPAK-5pin	PLSP0005ZB-A	LP	EL (3,000pcs/Reel)
RNA51A31FLPEL	MPAK-5pin	PLSP0005ZB-A	LP	EL (3,000pcs/Reel)
RNA51A44FLPEL	MPAK-5pin	PLSP0005ZB-A	LP	EL (3,000pcs/Reel)
RNA51A45FLPEL	MPAK-5pin	PLSP0005ZB-A	LP	EL (3,000pcs/Reel)
RNA51A46FLPEL	MPAK-5pin	PLSP0005ZB-A	LP	EL (3,000pcs/Reel)
RNA51B14FLPEL	MPAK-5pin	PLSP0005ZB-A	LP	EL (3,000pcs/Reel)
RNA51B27FLPEL	MPAK-5pin	PLSP0005ZB-A	LP	EL (3,000pcs/Reel)
RNA51B50FLPEL	MPAK-5pin	PLSP0005ZB-A	LP	EL (3,000pcs/Reel)

Applications

- Power supply voltage monitoring for microprocessors
- Battery-powered portable equipment
- Computers and notebook computers
- Wireless Communication Systems
- Digital still camera, digital video camera, PDA

Pin Arrangement



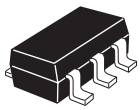
(Top view)

Product list

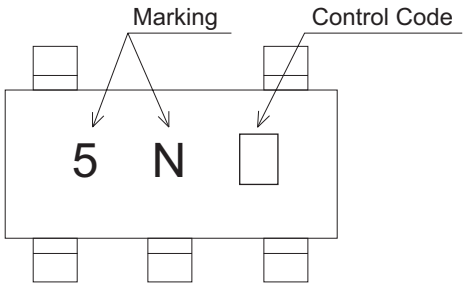
Threshold Voltage $-V_{TH}$ [V]	Open-Drain output		CMOS output	
	Type No.	Marking	Type No.	Marking
1.4	—	—	RNA51B14FLP	6P
2.6	RNA51A26FLP	5N	—	—
2.7	RNA51A27FLP	5P	RNA51B27FLP	7C
2.8	RNA51A28FLP	5Q	—	—
2.9	RNA51A29FLP	5R	—	—
3.0	RNA51A30FLP	5S	—	—
3.1	RNA51A31FLP	5T	—	—
4.4	RNA51A44FLP	6G	—	—
4.5	RNA51A45FLP	6H	—	—
4.6	RNA51A46FLP	6J	—	—
5.0	—	—	RNA51B50FLP	3R

Outline and Article Indication

• RNA51A26FLP (Example)

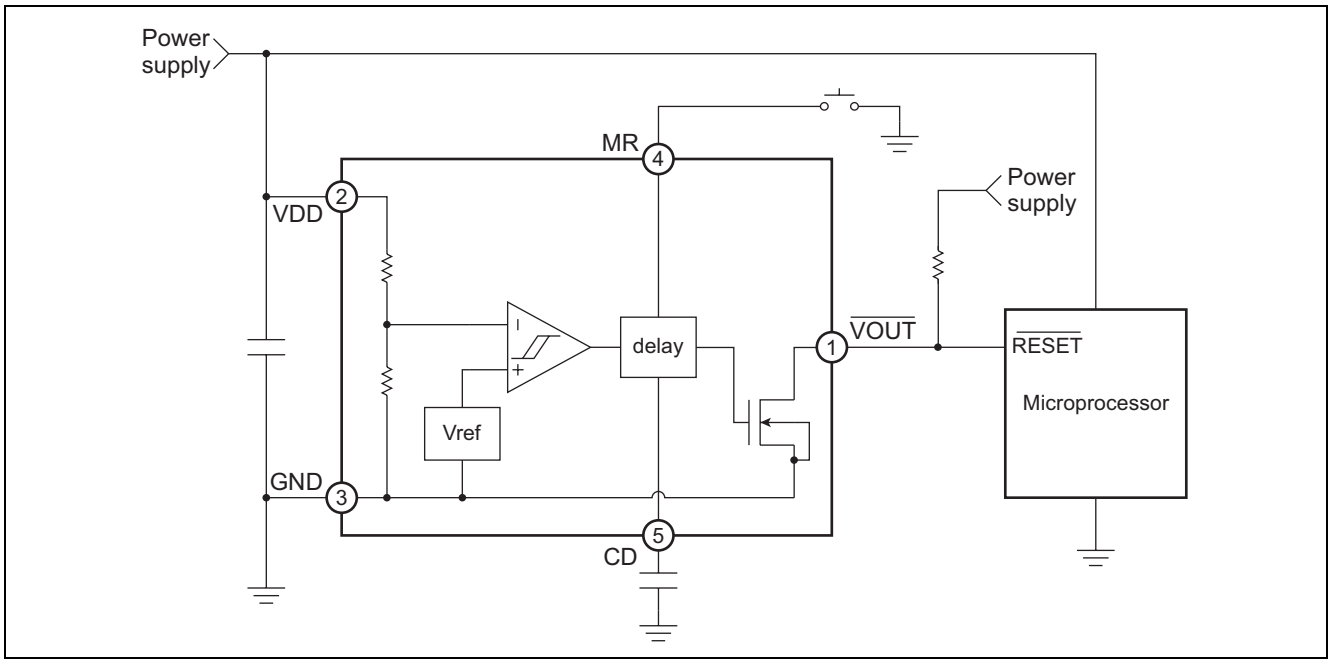


MPAK-5

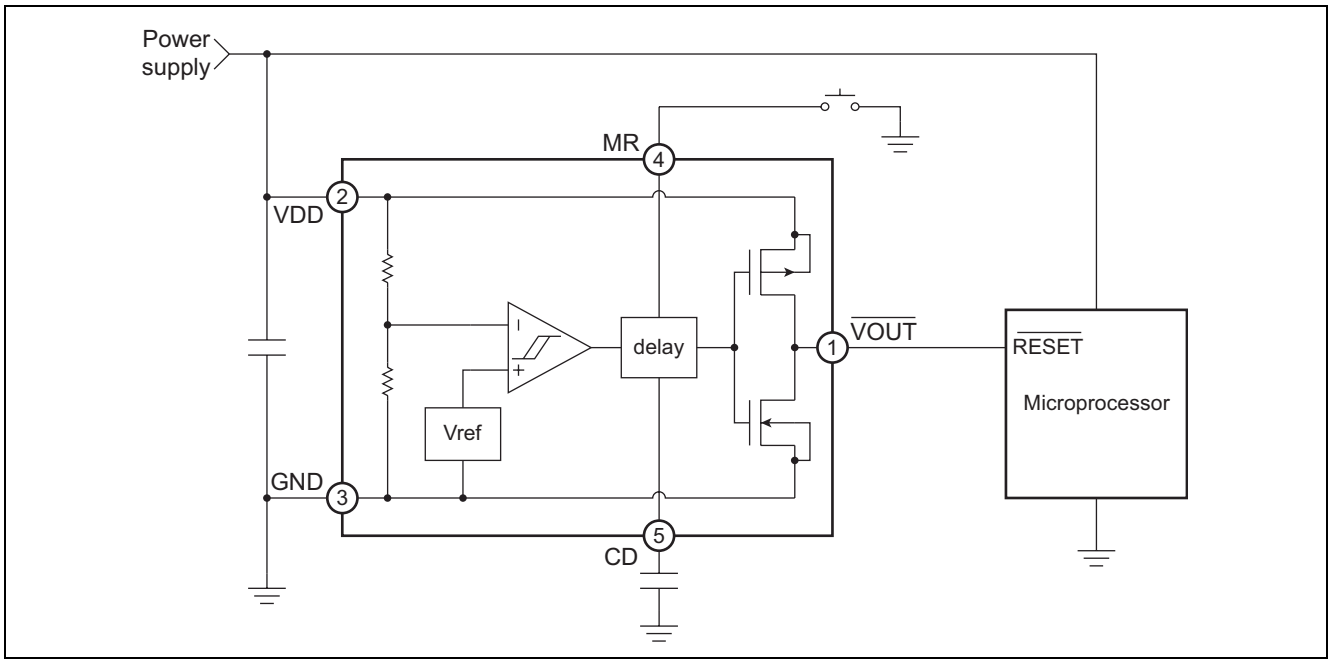


Functional block diagram & typical application circuit

(1) RNA51Axx Products

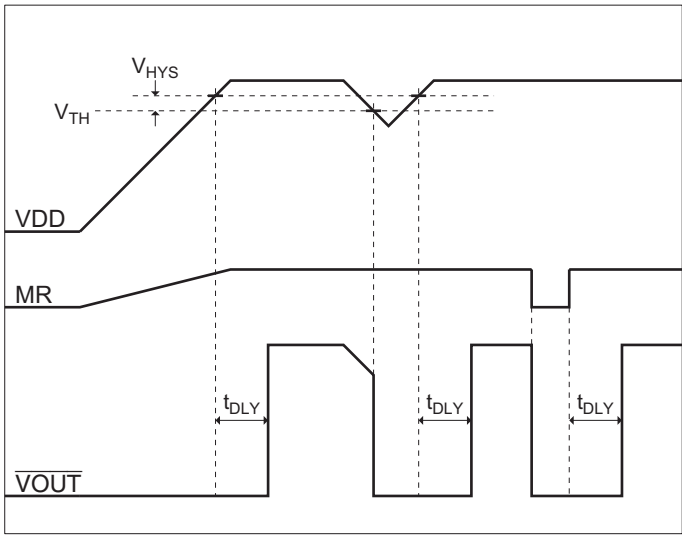


(2) RNA51Bxx Products



Notes: 1. It is good for stable operation to use a decoupling capacitor with excellent high frequency characteristics between VDD and GND pin.
2. Capacitor value is determined by system conditions.

Timing Diagram



Absolute Maximum Ratings

(1) RNA51Axx Products

Temperature condition Ta = 25°C

Item	Symbol	Pin	Ratings	Unit
Supply voltage	V_{DD}	V_{DD}	6.0	V
Output voltage	V_{OUT}	$\overline{V_{OUT}}$	–0.3 to 6.0	V
Input voltage	V_{IN}	MR, MD	–0.3 to V_{DD}+0.3	V
Output current	I_{OUT}	V_{OUT}	±50	mA
Continuous power dissipation	P_D	—	120	mW
Operating temperature range	T_{OPR}	—	–40 to +85	°C
Storage temperature range	T_{STG}	—	–55 to +125	°C

(2) RNA51Bxx Products

Temperature condition Ta = 25°C

Item	Symbol	Pin	Ratings	Unit
Supply voltage	V_{DD}	V_{DD}	6.0	V
Output voltage	V_{OUT}	$\overline{V_{OUT}}$	–0.3 to V_{DD}+0.3	V
Input voltage	V_{IN}	MR, MD	–0.3 to V_{DD}+0.3	V
Output current	I_{OUT}	V_{OUT}	±50	mA
Continuous power dissipation	P_D	—	120	mW
Operating temperature range	T_{OPR}	—	–40 to +85	°C
Storage temperature range	T_{STG}	—	–55 to +125	°C

Electrical characteristics

(1) RNA51Axx Products

Temperature condition Ta = 25°C

Item	Symbol	Min	Typ	Max	Unit	Conditions	
Supply voltage	V_{DD}	1.1	—	5.5	V	pull-up resistor = 470 kΩ $V_{OUT} \leq 0.1 \times VDD$	
Supply current	I_{DD}	—	0.7	4.2	µA	V_{DD} = 5.5 V	
Threshold voltage	$-V_{TH}$	$-V_{TH} \times 0.99$	—	$-V_{TH} \times 1.01$	V		
Temperature coefficiency of the thereshold voltage (Reference value)	$\frac{\Delta(-V_{TH})}{-V_{TH} \cdot \Delta Ta}$	—	±100	—	ppm/°C	Ta = –40 to 85°C	
Threshold voltage hysteresis	V_{HYS}	$-V_{TH} \times 3\%$	$-V_{TH} \times 5\%$	$-V_{TH} \times 8\%$	V		
$\overline{VOUT}$ low-level output current	I_{OL}	0.2	1.2	—	mA	V_{OUT} = 0.5 V	V_{DD} = 1.3 V
		3.4	7.0	—			V_{DD} = 2.4 V ($-V_{TH} \geq 2.7$ V)
$\overline{VOUT}$ Output leakage current (open drain output)	I_{LEAK}	—	—	0.1	µA	$V_{DD} = V_{OUT}$ = 5.5 V	
Delay time Note1	t_{DLY}	10	20	35	ms	V_{DD} = 1.1 to 5.5V, t_{TLH} = 1 µs C_D = 4.7 nF	
MR Low-level input voltage Note2	V_{IL}	—	—	$V_{DD} \times 0.25$	V		
MR High-level input voltage	V_{IH}	$V_{DD} \times 0.75$	—	—	V		
MR internal pull-up resistance	R_{MR}	1	2	7	MΩ		

(2) RNA51Bxx Products

Temperature condition Ta = 25°C

Item	Symbol	Min	Typ	Max	Unit	Conditions	
Supply voltage	V_{DD}	1.1	—	5.5	V	pull-up resistor = 470 kΩ $V_{OUT} \leq 0.1 \times VDD$	
Supply current	I_{DD}	—	0.7	4.2	µA	V_{DD} = 5.5 V	
Threshold voltage	$-V_{TH}$	$-V_{TH} \times 0.99$	—	$-V_{TH} \times 1.01$	V		
Threshold voltage temperature dependency (Reference value for design)	$\frac{\Delta(-V_{TH})}{-V_{TH} \cdot \Delta Ta}$	—	±100	—	ppm/°C	Ta = –40 to 85°C	
Threshold voltage hysteresis	V_{HYS}	$-V_{TH} \times 3\%$	$-V_{TH} \times 5\%$	$-V_{TH} \times 8\%$	V		
$\overline{VOUT}$ low-level output current	I_{OL}	0.2	1.2	—	mA	V_{OUT} = 0.5 V	V_{DD} = 1.3 V
		3.4	7.0	—			V_{DD} = 2.4 V ($-V_{TH} \geq 2.7$ V)
$\overline{VOUT}$ High-level output current (CMOS output)	I_{OH}	–1.4	–2.7	—	mA	V_{OUT} = V_{DD}–0.5 V	V_{DD} = 4.5 V ($-V_{TH} \leq 4.0$ V)
		–1.5	–3.0	—			V_{DD} = 5.5 V
Delay time Note1	t_{DLY}	10	20	35	ms	V_{DD} = 1.1 to 5.5 V, t_{TLH} = 1 µs C_D = 4.7 nF	
MR Low-level input voltage Note2	V_{IL}	—	—	$V_{DD} \times 0.25$	V		
MR High-level input voltage	V_{IH}	$V_{DD} \times 0.75$	—	—	V		
MR internal pull-up resistance	R_{MR}	1	2	7	MΩ		

Note: 1. Delay time is specified when charging starts in the condition that CD pin is completely discharged. When discharging of CD pin is not complete because of immediate stop and other reasons, the delay time is not guaranteed. Therefore, when passing of VDD pin input voltage immediately stops (the period of condition that VDD pin input voltage is lower than the detected voltage is short), discharging of external capacitor CD is inadequate, and the delay time becomes much shorter than the minimum guaranteed value. Be sure to fully check that there are no problems as the system.

2. Minimum value of low-pulse width to be input to MR pin depends on the value of external capacitor CD. Therefore, set the low-pulse width to be input to MR pin to the minimum input low-pulse width shown in figure 1 or more.

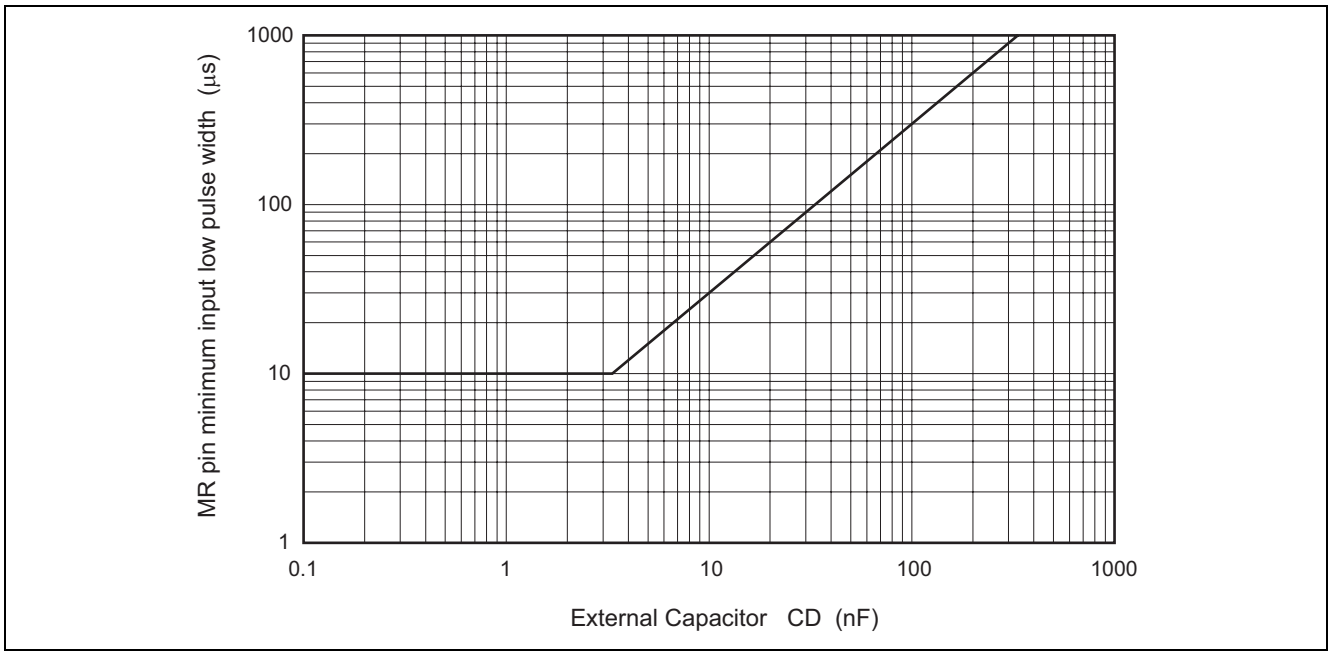


Figure 1 Dependence of MR pin minimum input low pulse width and external capacitor CD

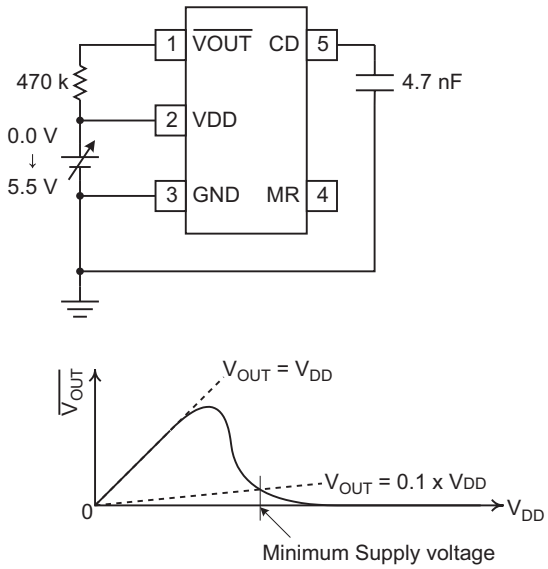
Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{VOUT}}$	$\overline{\text{VOUT}}$ changes from high to low whenever VDD drops below $-V_{TH}$. A pull-up resistor from 470 kΩ to 1 MΩ should be used on this pin for open-drain output.
2	VDD	Supply voltage and input for voltage detector. A decoupling capacitor with excellent high frequency characteristics should be placed near VDD pin and connected between VDD and GND pin.
3	GND	Ground
4	MR	Active-low Manual Reset Input. $\overline{\text{VOUT}}$ is low-level while MR is low. Once MR is disabling, $\overline{\text{VOUT}}$ turn to high-level after delay time. MR pin is internally pulled up to VDD through 2 MΩ.
5	CD	Connect capacitor between CD and GND pin to set programmable delay time. Ceramic capacitor from 100 pF to 0.1 µF is recommended.

Test Circuit

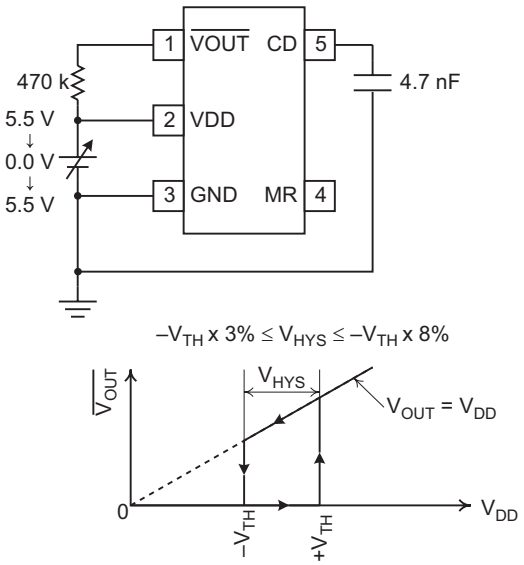
(1) RNA51Axx Products

Minimum Supply voltage V_{DDmin}



Minimum Supply voltage: $V_{OUT} = 0.1 \times V_{DD} \leq 1.1$ V

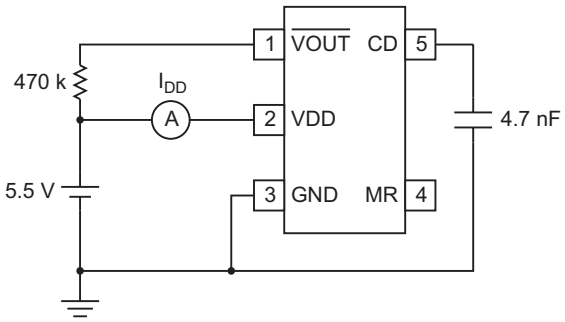
Threshold voltage and Hysteresis $\pm V_{TH}$ & V_{HYS}



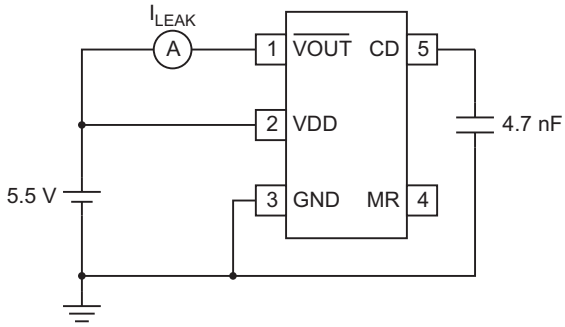
$-V_{TH}$: Reset asserted voltage

$+V_{TH}$: Reset released voltage

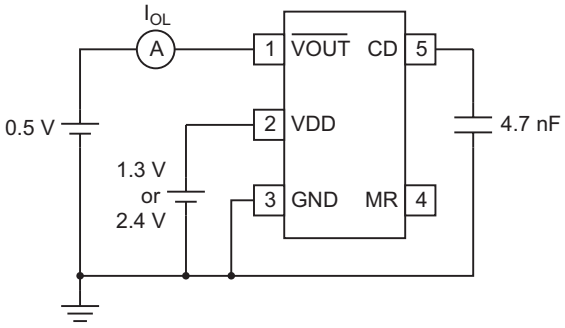
Supply current I_{DD}



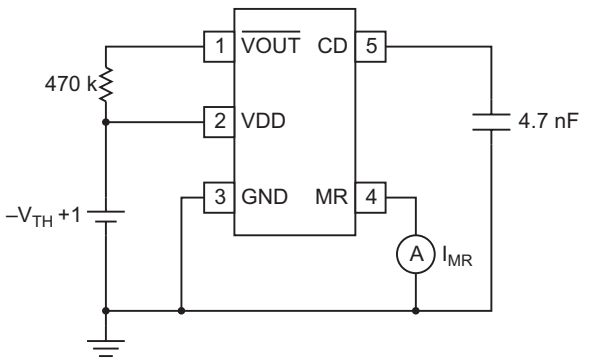
Output leakage current I_{LEAK}



Low-level output current I_{OL}



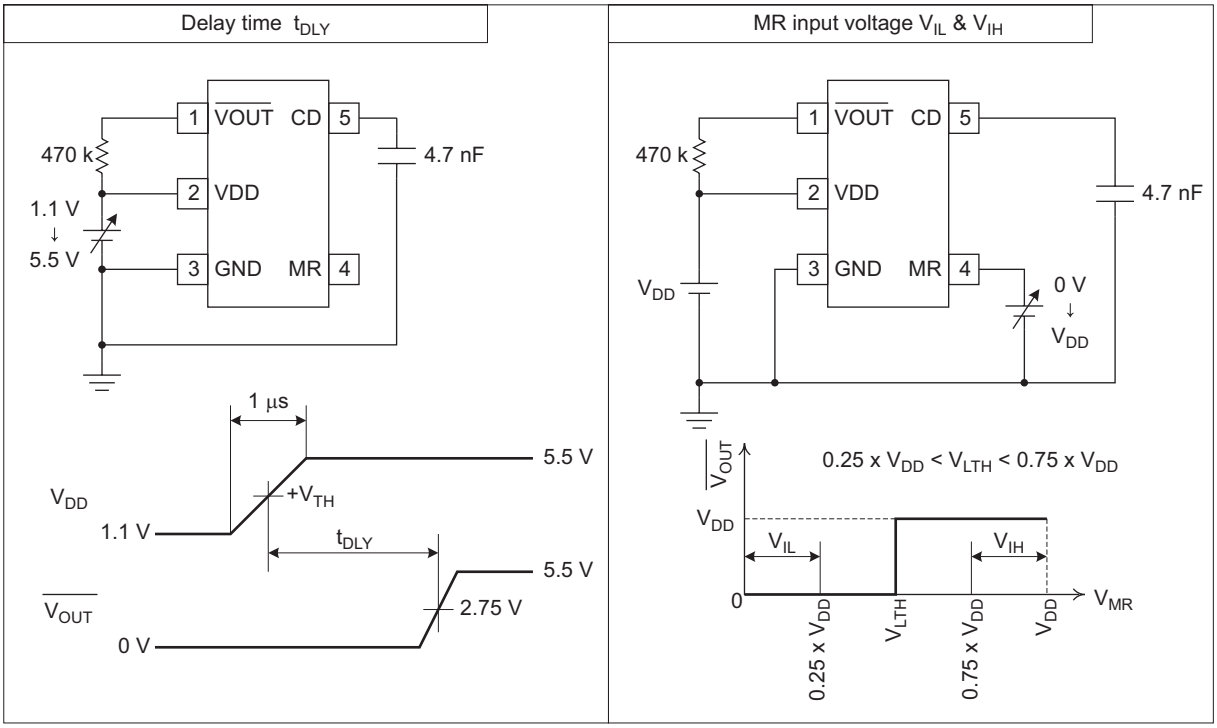
MR internal pull-up resistance R_{MR}



$$R_{MR} = \frac{-V_{TH} + 1}{I_{MR}}$$

Test Circuit (Cont.)

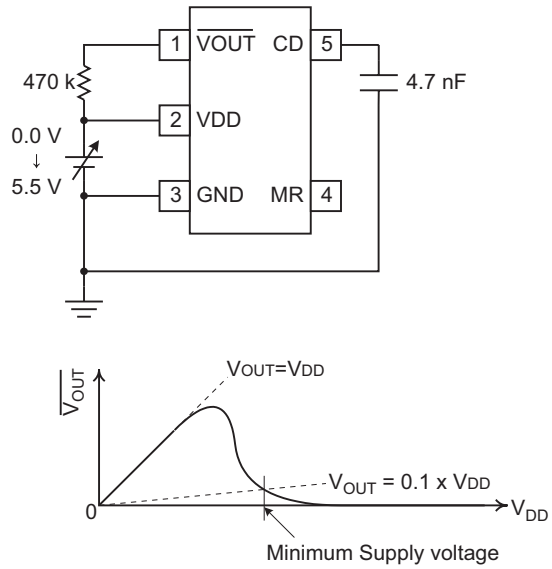
(1) RNA51Axx Products



Test Circuit (Cont.)

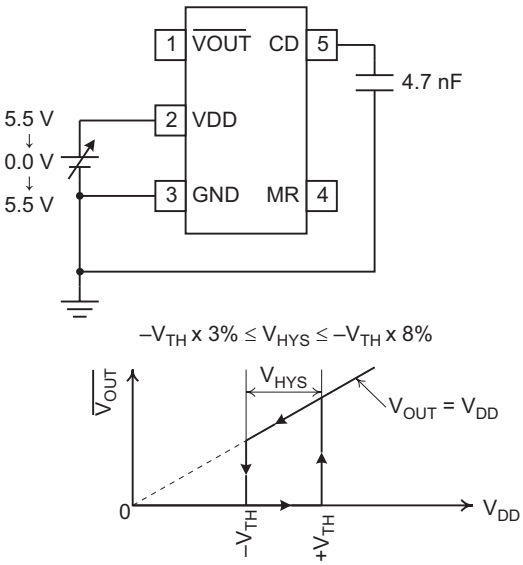
(2) RNA51Bxx Products

Minimum Supply voltage V_{DDmin}



Minimum Supply voltage: $V_{OUT} = 0.1 \times V_{DD} \leq 1.1$ V

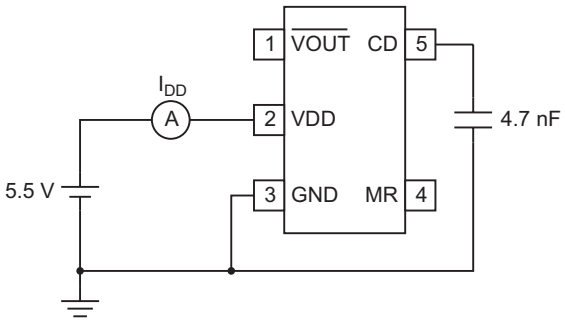
Threshold voltage and Hysteresis $\pm V_{TH}$ & V_{HYS}



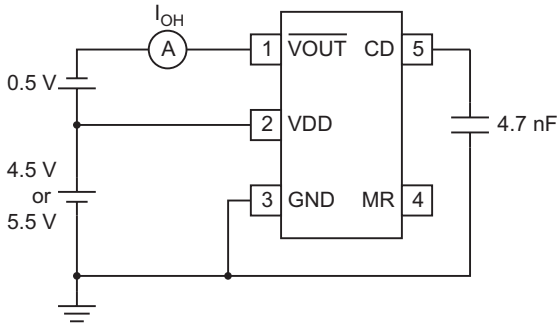
$-V_{TH}$: Reset asserted voltage

$+V_{TH}$: Reset released voltage

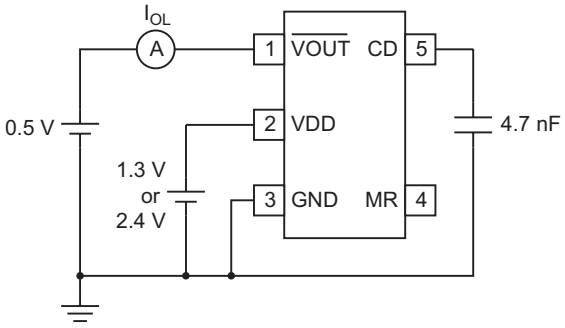
Supply current I_{DD}



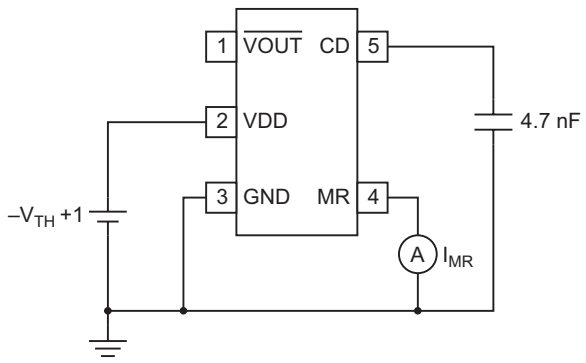
High-level output current I_{OH}



Low-level output current I_{OL}



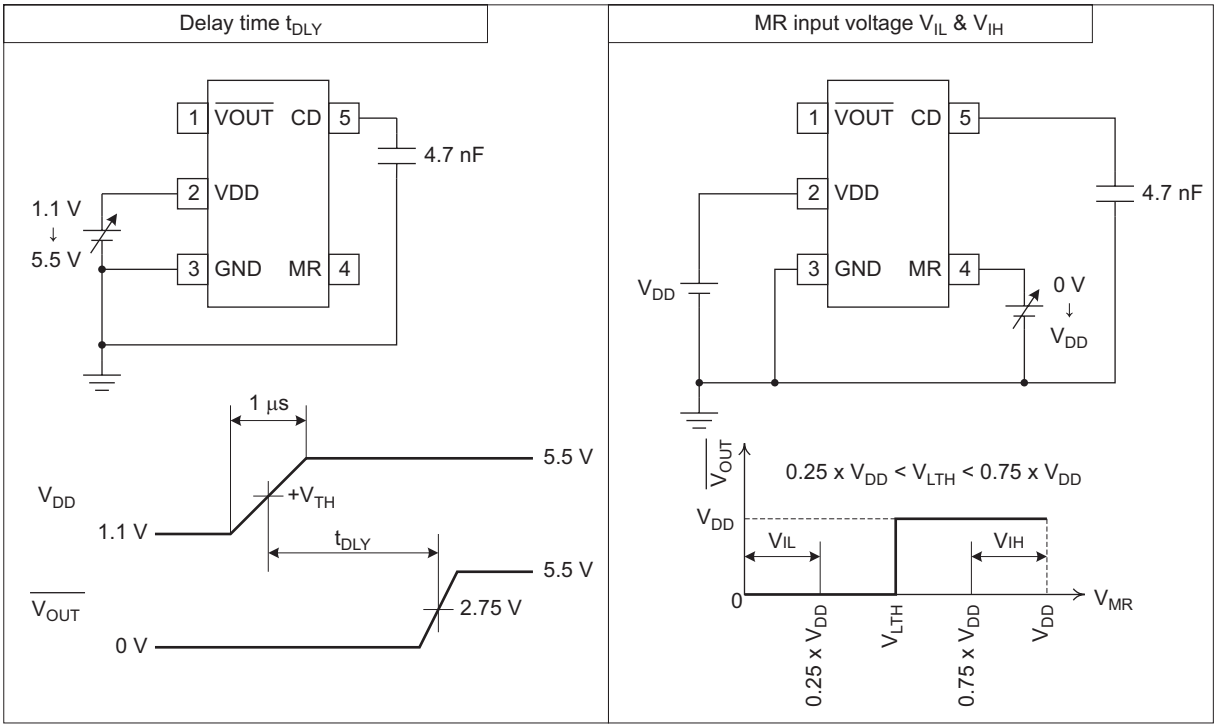
MR internal pull-up resistance R_{MR}



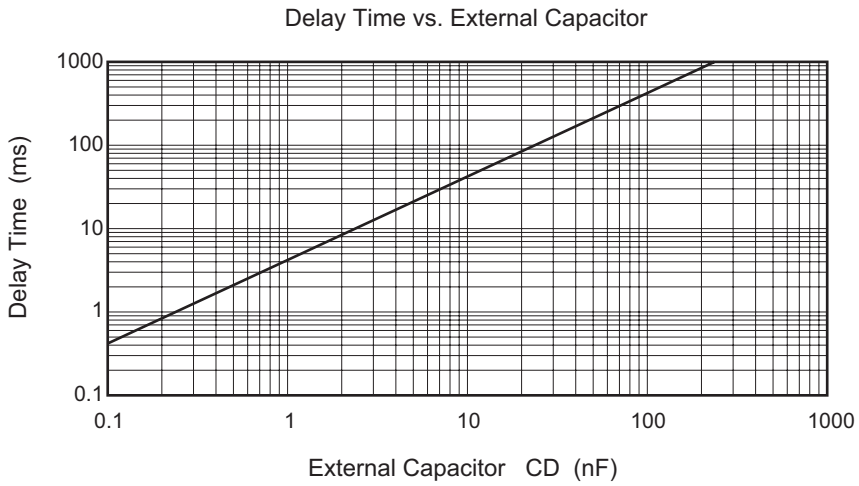
$$R_{MR} = \frac{-V_{TH} + 1}{I_{MR}}$$

Test Circuit (Cont.)

(2) RNA51Bxx Products



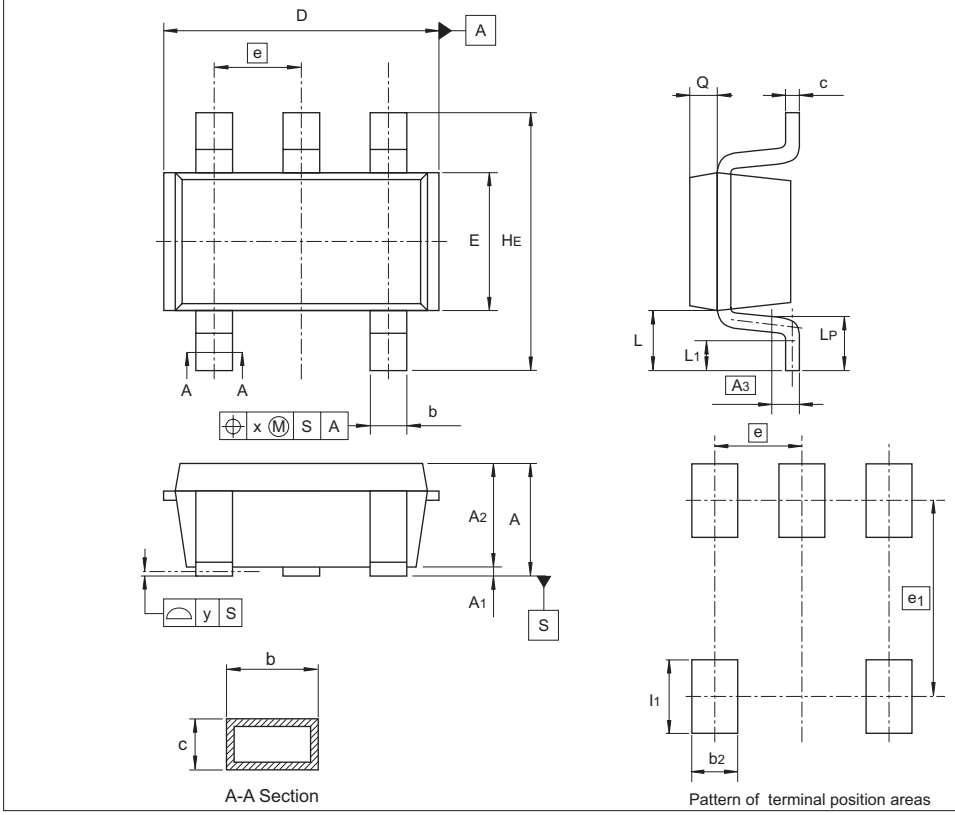
Delay Time Graph



Note: This graph shows simulation results.

Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
MPAK-5	SC-74A	PLSP0005ZB-A	MPAK-5 / MPAK-5V	0.015g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	1.0	–	1.4
A_1	0	–	0.1
A_2	1.0	1.1	1.3
$\boxed{A_3}$	–	0.25	–
b	0.35	0.4	0.5
c	0.11	0.16	0.26
D	2.8	2.95	3.1
E	1.5	1.6	1.8
$\boxed{e}$	–	0.95	–
H_E	2.5	2.8	3.0
L	0.3	–	0.7
L_1	0.1	–	0.5
L_P	0.2	–	0.6
x	–	–	0.05
y	–	–	0.05
b_2	–	–	0.55
$\boxed{e_1}$	–	2.15	–
l_1	–	–	0.85
Q	–	0.3	–

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