

RAiO

RA8917

**8-Bit
Micro-Controller**

Version 1.0

October, 2003

RAiO Technology Inc.

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Overview

RA8917 is an 8-bit downloadable micro-controller. Up to 22MHz system clock makes it a perfect choice for high-end device. It contains a 16x16 Multiplier and Accumulator (MAC), which not only greatly reduce programmer's effort, but also shorten development time. RA8917 is embedded 4-channel 12-Bit ADC that can vary your application fields in analog detection, such as temperature, pressure, humidity, etc. Moreover, matched with LCM (LCD Module), 12-bit ADC can be perfectly used in Touch Panel function.

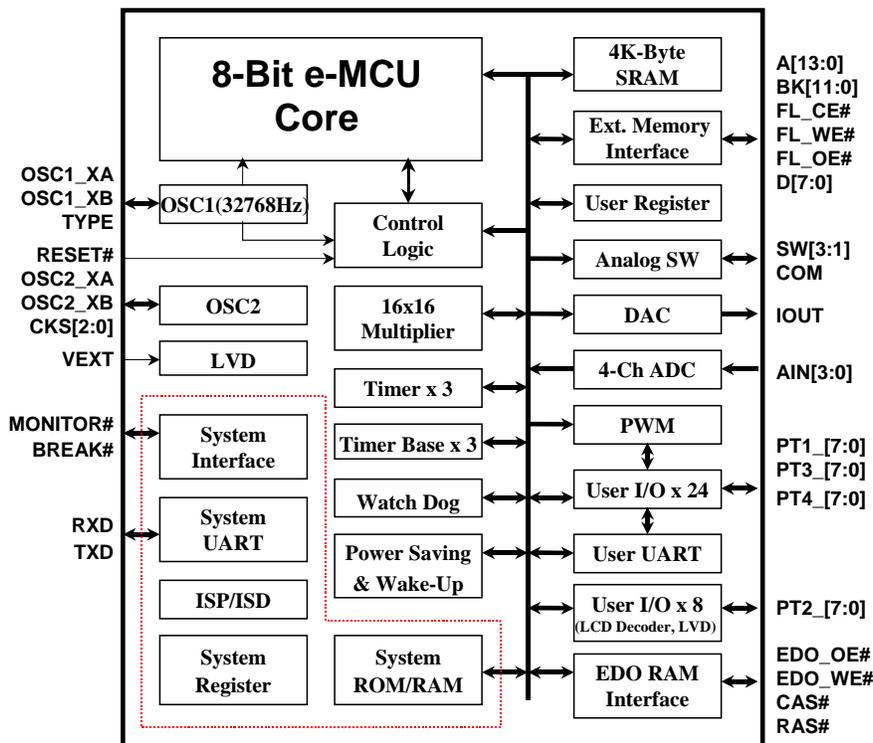
RA8917 is suitable for any downloadable device no matter used by end-users for voice/data download, or used by programmers for S/W program updated. The built-in 8K-byte ROM supports the on-chip RAiO ICE Monitor program, ISP(In-System Programming) and ISD(In-System Debugging), which controls the UART and enables the RS232 connection between the RA8917 and a PC host. Besides that, IrDA application is also allowed to give the device multiple attractive characteristics.

In short, RA8917 supports embedded 4K-byte SRAM, three I/O ports, LCD interface, built in PLL / RC Oscillator, LVD, multiple timer/counter sources, versatile interrupt-handling architecture, built-in one DAC (Digital-to-Analog Converters), 16x16 Multiplier and Accumulator (MAC), 4-channel 12-Bit ADC and support three EDO DRAM (Extended Data Out) interface configuration: one 4Mx4bit chip, two 4Mx4 chips and one 8Mx8 chip.

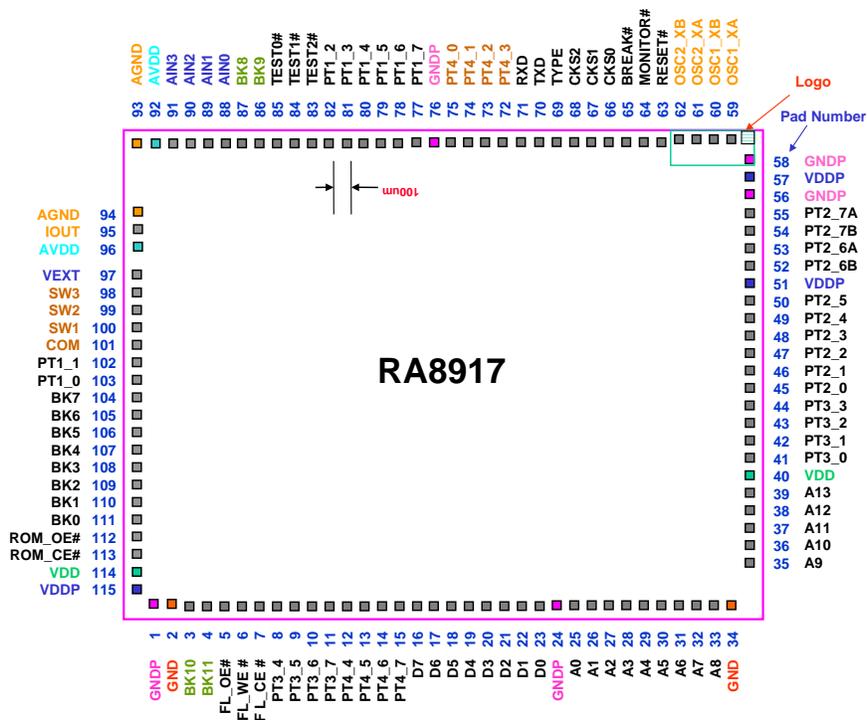
Feature

- ◆ 8-bit Micro Processor for Maximum 22MHz
- ◆ Support 3 EDO DRAM Interface configuration
 1. External one 4Mx4bit chip
 2. External two 4Mx4bit chips
 3. External one 8Mx8bit chip
- ◆ Internal 4K-Byte SRAM
- ◆ Support External ROM/RAM/Flash Interface
- ◆ Flexible External Flash Support, Up to 128MByte
- ◆ Flexible I/O Interrupt & Wake-Up Mode
- ◆ Support Wake-Up Reset Mode
- ◆ Support LVD(Low Voltage Detector)
- ◆ Support External Memory Interface
- ◆ Support LCD Interface
- ◆ Support PWM Output with 50% or 100% duty select
- ◆ Four 8-Bits Programmable I/O Port
- ◆ Three 12-Bits Timer
- ◆ Six Time-Base Options
- ◆ Watch Dog Timer
- ◆ One 3 -Level 10-bits Fixed Current Mode DAC
- ◆ Support 4-channel 12-bit ADC with Touch Panel Function
- ◆ One User's UART with Baud Rate Generator, Up to 115200bps
- ◆ UART Provide Normal, IrDA/ASK IR Mode
- ◆ Support UART Wakeup
- ◆ Support Idle/Sleep/Power Saving Mode
- ◆ Support Timer Wake-Up Mode
- ◆ Support H/W 16x16 Multiplier with Adder Option
- ◆ 1Hz, 2Hz and 1/60Hz Interrupt/Wake up
- ◆ Support Interrupt Vector & Priority
- ◆ Built in two Independent Oscillator; Low Speed (32768Hz) and High Speed (From 1.84MHz to 22.1MHz)
- ◆ Low Power Consumption
- ◆ Operating Voltage: 2.2V ~ 4.5V
- ◆ Package: Die Form or PQFP-128Pin

Block Diagram



PAD Diagram



PAD X/Y Coordinate

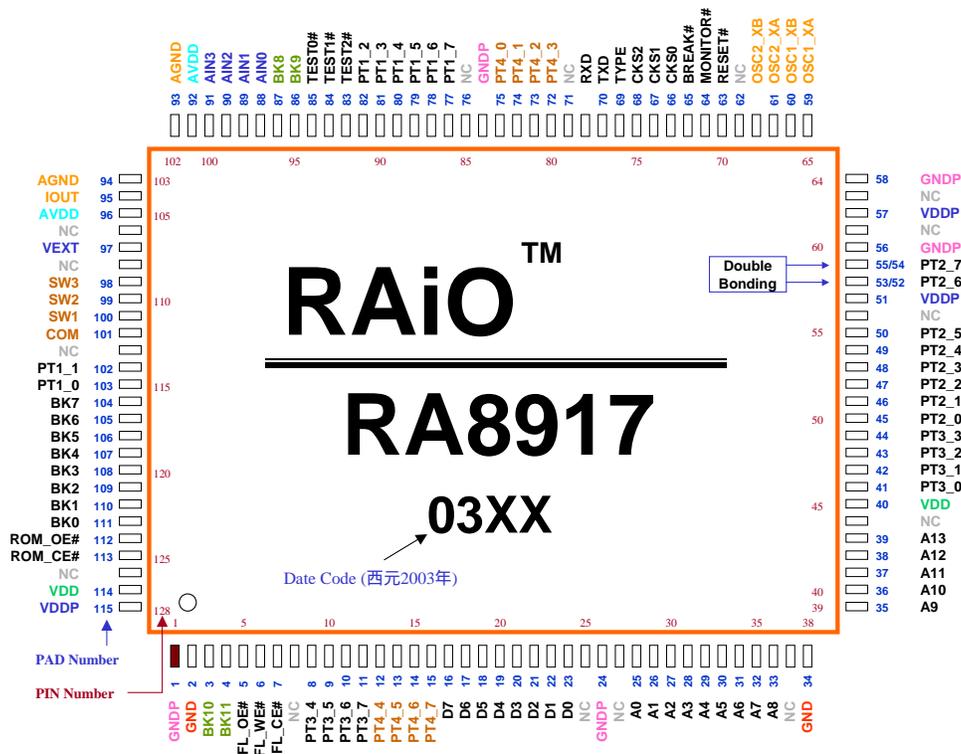
Pad Order	Pin Name	X	Y
1	GNDP	-1651.65	-1330.4
2	GND	-1546.65	-1330.4
3	BK10	-1446.65	-1330.4
4	BK11	-1346.65	-1330.4
5	FL_OE#	-1246.65	-1330.4
6	FL_WE#	-1146.65	-1330.4
7	FL_CE#	-1046.65	-1330.4
8	PT3_4	-946.65	-1330.4
9	PT3_5	-846.65	-1330.4
10	PT3_6	-746.65	-1330.4
11	PT3_7	-646.65	-1330.4
12	PT4_4	-546.65	-1330.4
13	PT4_5	-446.65	-1330.4
14	PT4_6	-346.65	-1330.4
15	PT4_7	-246.65	-1330.4
16	D7	-146.65	-1330.4
17	D6	-46.65	-1330.4
18	D5	53.35	-1330.4
19	D4	153.35	-1330.4
20	D3	253.35	-1330.4
21	D2	353.35	-1330.4
22	D1	453.35	-1330.4
23	D0	553.35	-1330.4
24	GNDP	653.35	-1330.4
25	A0	753.35	-1330.4
26	A1	853.35	-1330.4
27	A2	953.35	-1330.4
28	A3	1053.35	-1330.4
29	A4	1153.35	-1330.4
30	A5	1253.35	-1330.4
31	A6	1353.35	-1330.4
32	A7	1453.35	-1330.4
33	A8	1553.35	-1330.4
34	GND	1653.35	-1330.4
35	A9	1769.7	-1214.05
36	A10	1769.7	-1114.05

Pad Order	Pin Name	X	Y
37	A11	1769.7	-1014.05
38	A12	1769.7	-914.05
39	A13	1769.7	-814.05
40	VDD	1769.7	-585.85
41	PT3_0	1769.7	-485.85
42	PT3_1	1769.7	-385.85
43	PT3_2	1769.7	-285.85
44	PT3_3	1769.7	-185.85
45	PT2_0	1769.7	-85.85
46	PT2_1	1769.7	14.15
47	PT2_2	1769.7	114.15
48	PT2_3	1769.7	214.15
49	PT2_4	1769.7	314.15
50	PT2_5	1769.7	414.15
51	VDDP	1769.7	514.15
52	PT2_6	1769.7	614.15
53	PT2_6B	1769.7	714.15
54	PT2_7	1769.7	814.15
55	PT2_7B	1769.7	914.15
56	GNDP	1769.7	1014.15
57	VDDP	1769.7	1114.15
58	GNDP	1769.7	1215.55
59	OSC1_XA	1680.23	1330.5
60	OSC1_XB	1580.22	1330.5
61	OSC2_XA	1480.22	1330.5
62	OSC2_XB	1380.22	1330.5
63	RESET#	1280.22	1330.5
64	MONITOR#	1180.22	1330.5
65	BREAK#	1080.22	1330.5
66	CKS0	980.22	1330.5
67	CKS1	880.22	1330.5
68	CKS2	780.22	1330.5
69	TYPE	680.22	1330.5
70	TXD	580.22	1330.5
71	RXD	480.22	1330.5
72	PT4_3	380.22	1330.5

Pad Order	Pin Name	X	Y
73	PT4_2	280.22	1330.5
74	PT4_1	180.22	1330.5
75	PT4_0	80.22	1330.5
76	GNDP	-19.78	1330.5
77	PT1_7	-119.78	1330.5
78	PT1_6	-219.78	1330.5
79	PT1_5	-319.78	1330.5
80	PT1_4	-419.78	1330.5
81	PT1_3	-519.78	1330.5
82	PT1_2	-619.78	1330.5
83	TEST2	-719.78	1330.5
84	TEST1	-819.78	1330.5
85	TEST0	-919.78	1330.5
86	BK9	-1019.78	1330.5
87	BK8	-1119.78	1330.5
88	AIN0	-1234.25	1330.5
89	AIN1	-1339.25	1330.5
90	AIN2	-1444.25	1330.5
91	AIN3	-1549.25	1330.5
92	AVDD	-1648.75	1330.5
93	AGND	-1748.75	1330.5
94	AGND	-1769.55	872.25

Pad Order	Pin Name	X	Y
95	IOUT	-1769.55	771.75
96	AVDD	-1769.55	672.25
97	VEXT	-1769.55	567.95
98	SW3	-1769.55	467.95
99	SW2	-1769.55	367.95
100	SW1	-1769.55	267.95
101	COM	-1769.55	167.95
102	PT1_1	-1769.55	67.95
103	PT1_0	-1769.55	-32.05
104	BK7	-1769.55	-132.05
105	BK6	-1769.55	-232.05
106	BK5	-1769.55	-332.05
107	BK4	-1769.55	-432.05
108	BK3	-1769.55	-532.05
109	BK2	-1769.55	-632.05
110	BK1	-1769.55	-732.05
111	BK0	-1769.55	-832.05
112	ROM_OE#	-1769.55	-932.05
113	ROM_CE#	-1769.55	-1032.05
114	VDD	-1769.55	-1132.05
115	VDDP	-1769.55	-1232.05

Package (PQFP-128Pin)



Pin Description

Signal	I/O	Description
RESET#	IN	External Hardware Reset, active low. This pin is used to reset the system.
BREAK#	IN	User Program Break, active low. This signal is used to break the user's program from the ISD mode.
MONITOR#	IN	Monitor Program Select, active low. This signal is used to select the system boot from monitor program (ROM) or user program (Flash). This signal has to pull low when the user wants to download the data from PC or enter the ISP/ISD mode. Note: Couldn't be floating.
PT1_[7:0]	I/O	Bit[7:0] of Port 1 These are programmable pins for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register.
PT2_7	I/O	Bit-7 of Port 2 This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.
PWM1		The PT2_7 is also as the output of PWM1. In PWM mode, the pin is always output and 72mA-driving current is selected.

PT2_6	I/O	<p>Bit-6 of Port 2 This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.</p>
PWM2		<p>The PT2_6 is also as the output of PWM2. In PWM mode, the pin is always output and 72mA-driving current is selected.</p>
PT2_5	I/O	<p>Bit-5 of Port 2 This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.</p>
EXP_WR#		<p>The PT2_5 is also as the write control of register \$101E. If the write register \$101F enabled, the pin is always output except the power saving mode.</p>
PT2_4	I/O	<p>Bit-4 of Port 2 This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.</p>
FL_CE2#		<p>The PT2_4 is also as the secondary external flash chip select. If the secondary flash is enabled, the pin is always output except the power saving mode.</p>
PT2_3	I/O	<p>Bit-3 of Port 2 This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.</p>
LVD_#		<p>The PT2_3 is also as the output of LVD. If the LVD enabled, the pin is always output except the power saving mode.</p>
PT2_2	I/O	<p>Bit-2 of Port 2 This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.</p>
MEM_WE#		<p>The PT2_2 is also as the external memory write enable. If the external memory enabled, the pin is always output except the power saving mode. If REG[1032h] bit6 is set as 1, and then MEM_WE# and FL_WE# can be jointly used.</p>
PT2_1	I/O	<p>Bit-1 of Port 2 This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.</p>
MEM_OE#		<p>The PT2_1 is also as the external memory output enabling. If the external memory enabled, the pin is always output except the power saving mode. If REG[1032h] bit6 is set as 1, and then MEM_OE# and FL_OE# can be jointly used.</p>
PT2_0	I/O	<p>Bit-0 of Port 2 This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.</p>
MEM_CE#		<p>The PT2_0 is also as the external memory chip selecting. If the external memory enabled, the pin is always output except the power saving mode.</p>
PT3_7	I/O	<p>Bit-7 of Port 3 This is a programmable pin for general-purpose I/O Port 3. The driving current and pull-high or pull-low can be selected by user register.</p>
EDO_OE#		<p>The PT3_7 is also as the EDO RAM data output enable.</p>
PT3_6	I/O	<p>Bit-6 of Port 3 This is a programmable pin for general-purpose I/O Port 3. The driving current and pull-high or pull-low can be selected by user register.</p>
EDO_WE#		<p>The PT3_6 is also as the EDO RAM Read/Write input.</p>

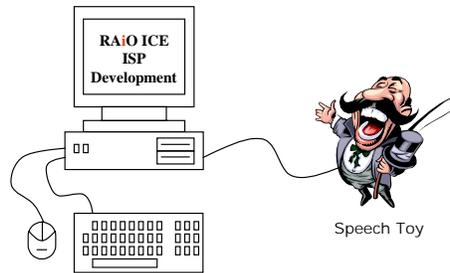
PT3_5	I/O	Bit-5 of Port 3 This is a programmable pin for general-purpose I/O Port 3. The driving current and pull-high or pull-low can be selected by user register.
CAS#		The PT3_5 is also as the EDO RAM Column Address Strobe.
PT3_4	I/O	Bit-4 of Port 3 This is a programmable pin for general-purpose I/O Port 3. The driving current and pull-high or pull-low can be selected by user register.
RAS#		The PT3_4 is also as the EDO RAM Row Address Strobe.
PT3_3	I/O	Bit-3 of Port 3 The PT3_3 is also as the transmission output of user's UART. In UART mode, the pin is always output except the power saving mode.
TX		
PT3_2	I/O	Bit-2 of Port 3 The PT3_2 is also as the receive input of user's UART. In UART mode, the pin is always input.
RX		
PT3_1	I/O	Bit-1 of Port 3 The PT3_1 is also as the chip enable of external LCD controller. If the external LCD enabled, the pin is always output except the power saving mode.
LCD_E		
PT3_0	I/O	Bit-0 of Port 3 The PT3_0 is also as the read/write signal of external LCD controller. If the external LCD enabled, the pin is always output except the power saving mode.
LCD_RW		
PT4_[7:0]	I/O	Bit 7~0 of Port 4 This is a programmable pin for general-purpose I/O Port 4. The driving current and pull-high or pull-low can be selected by user register.
IOUT	OUT	DAC Current Output This pin is the current output of DAC.
AIN[3:0]	IN	ADC Analog Input These pins are the analog input of 12-bit ADC for 4-channel.
		ADC Mode Touch Panel Mode
		AIN0 X1
		AIN1 X2
		AIN2 Y1
AIN3 Y2		
SW[3:1]	OUT	Analog switch [3~1]
COM	IN	Common input voltage of switch [3~1]
A[13:0]	OUT	14-bit Address Bus. These signal are used for external memory address bus.
D[7:0]	I/O	8-bit Data Bus. These signal are used for external memory data bus.
FL_CE#	OUT	Flash Chip Select, active low. This signal is used for external flash.
FL_WE#	OUT	Flash Write Enable, active low. This signal is used for external flash. If REG[1032h] bit6 is set as 1, and then FL_WE# and MEM_WE can be jointly used.
FL_OE#	OUT	Flash Output Enable, active low. This signal is used for external flash. If REG[1032h] bit6 is set as 1, and then FL_OE# and MEM_OE# can be jointly used.
BK[11:0]	OUT	Bank Bus. Register FBANK[1030h], [105Ah] and Ext_SBank [103Fh], [105Bh] jointly use Bank[11:0] Bus as the output of memory bank register. Normally, they are connected to the higher address of external Flash memory.

RXD	IN	Receive Data This is the received data input of system UART. Normally it's connected to the RS232's TX of PC.																																				
TXD	OUT	Transmit Data This signal is the transmitted data output of system UART. Normally it's connected to the RS232's RX of PC.																																				
OSC1_XA	IN	Oscillator1 Input. This is the input signal of external X'tal(32768Hz).																																				
OSC1_XB	OUT	Oscillator1 Output. This is the output signal of external X'tal(32768Hz).																																				
OSC2_XA	IN	Oscillator2 Input. This is the input signal of external X'tal. (maximum up to 22.1184MHz)																																				
OSC2_XB	OUT	Oscillator2 Output. This is the output signal of external X'tal. (maximum up to 22.1184MHz)																																				
CKS[2:0]	IN	OSC2 Frequency Select These input signals are used to select the OSC2 speed during the hardware reset.																																				
		<table border="1"> <thead> <tr> <th>CKS2</th> <th>CKS1</th> <th>CKS0</th> <th>OSC2 Clock</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1.8432MHz</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>3.6864MHZ</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>5.5296MHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>7.3728MHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>11.0592MHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>14.7456MHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>18.432MHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>22.1184MHz</td> </tr> </tbody> </table>	CKS2	CKS1	CKS0	OSC2 Clock	0	0	0	1.8432MHz	0	0	1	3.6864MHZ	0	1	0	5.5296MHz	0	1	1	7.3728MHz	1	0	0	11.0592MHz	1	0	1	14.7456MHz	1	1	0	18.432MHz	1	1	1	22.1184MHz
		CKS2	CKS1	CKS0	OSC2 Clock																																	
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Clock Type Select for 32768Hz 0: RC Oscillator 1: 32768 X'tal Note: Couldn't be floating.																																						
Low Voltage Detector Input																																						
Test Pins Test Pins are for RAiO's internal testing purpose used in testing IC and ROM status. Normally, users will not use these pins. Therefore, please connect these three pins to VDD when making PCB board.																																						
Power Supply Voltage of Chip Core.																																						
Power Supply Voltage of Chip I/O.																																						
Analog Power Supply Voltage.																																						
Ground of Chip Core.																																						
Ground of Chip I/O.																																						
Analog Ground.																																						

Development

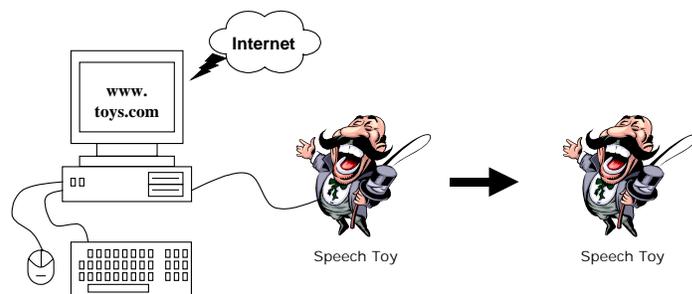
The RA8917 support the ISP (In-System Programming) and ISD (In-System Debugging) functions for customer to develop their system. Users can download their programs as well as data from a PC host to the external Flash ROM.

-ISP/ISD Mode is entered when the MONITOR# pin having been pulled down to ground voltage level. The on-chip Monitor program together with RAiO's ICE (RICE-2000) Utility Program running on a PC will be executed to support ICE debugging and ISP download of user programs from the PC Host.



Develop Program from ISP Mode
(Customers)

-User Mode is entered when the MONITOR# pin has been pulled up to logic high voltage level. User application programs can be executed only in this mode. The end-user can download the application program or data from the customer's website through the PC interface. Because the program/data was stored in the flash so the application device of customer (such as speech toy) will operate independent that after disconnect with the PC.



Down load from Internet
(End-Users)

A Portable Speech Toy

RICE-2000 (RICE for short) is a full-completed environment developed by RAiO especially for RA89XX series. The major reason for developing RICE is give fully convenience to program designers who are using RA89XX IC, and let them enjoy consistent and friendly design environment at planning, designing and debugging. In RICE environment, it saves a great deal of developing time by not only providing Editor for users to do direct coding, but also providing many Hot-Key functions for users to do direct compiling, linking, and downloading. Since RA89XX series carry 8-bit micro-processor and a framework of ISP (In-System-Programming), ISD (In-System Debugging), then this simple and reliable environment of RICE can let program designers to proceed design and debug in Real Chip. Moreover, the mass-production ICs are ready for clients to do planning and designing directly without diverse traits happened between developing time and mass production period.

In the meanwhile, in order to support integrated speech interface, RICE provides a solution of 32K-bps ADPCM for programmers to easily combine programs and speech files. If you want to have more information and program design skills of RA8917, please refer to the user manual of RICE-2000.

Application

The following Block diagram is the basic application circuit of RA8917. We also give three examples on the user manual of RICE-2000 to let users have more understanding of RA8917 and the develop environment of RICE-2000, and then start to proceed program designing and product developing. The examples have one simple I/O control and two speech samples. Please refer to the user manual of RICE-2000 if you needed.

Application Field	
Simple I/O Controller	General Propose Controller
Speech Controller	Internet Download (Speech/Voice Toy, Sound Book, Voice-Prompted Controller...)
Low-Grade Product	LCD Game, Calculator, Calendar, Internet Download (educational toy or household appliance...)
High-Grade Product	SMS Controller, Low-end PDA Controller and Internet Download Device Function

