M65580MAP-XXXFP

Digital Video/Chroma/Deflection +MCU

REJ03F0184-0201
Rev.2.01
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Description

The M65580MAP-XXXFP are semiconductor integrated circuits designed with CMOS silicon gate technology for NTSC television system, include 8 bit MCU (M37272MA core) with a closed caption decoder and circuits needed for TV base-band signals (Video and Chroma) processor and Deflection in a chip. PCB area and EMI noise can be reduced by one chip and 80QFP, and internal connection of OSD signals. And it can realize an adjustment free system by built-in MCU and get a high performance adaptive YC separation by 1 line memory. The above technology makes its performance more stable and better.

Features

- Y/C processor: 8 bit Input, 10 bit Output digital processing
- Deflection processor: optimized system by conventional analog and digital mixed solution
- ADC & DAC: 8 bit high speed video ADC & 10 bit high speed video DAC

[MCU Block]

MCU (single microcomputer) in this IC has almost same function and performance as M37272MA-XXXSP/FP in mass-production. And it is operated by simple instruction in the same memory space as that of built-in ROM, RAM, I/O. It has an OSD, data slicer, and I^2C-BUS interface. So it is very useful for a channel selection system for NTSC TV with a closed caption decoder.

[ASIC Block]

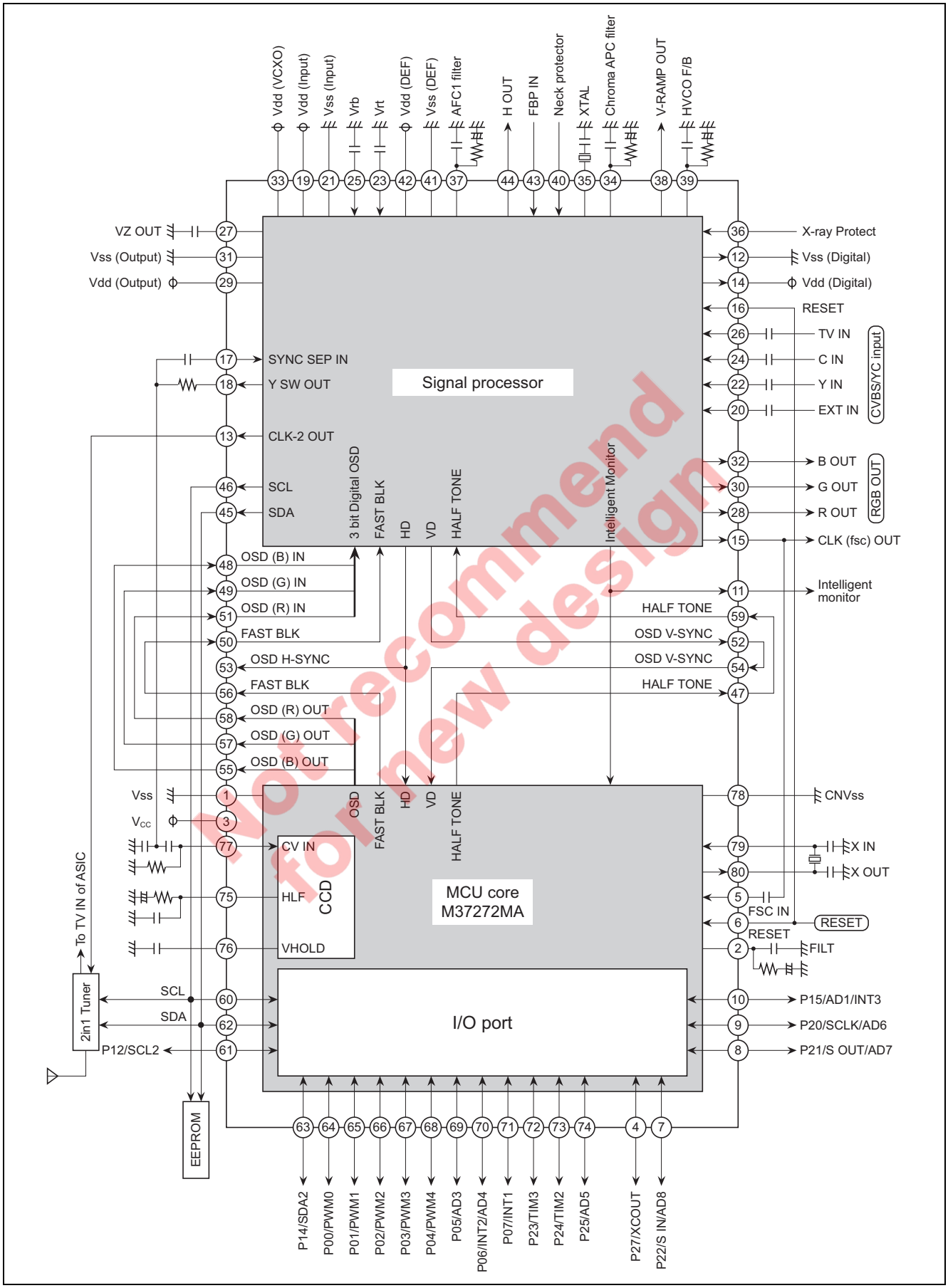
ASIC block consists of the following blocks.

(1) Analog front-end block; Analog SW (2 CVBS (TV & EXT) inputs, Y/C signals to one signal, 2 channels 8 bit high speed video ADCs, and ACC amplifiers.
(2) Video and Chroma block; A high performance 2 line adaptive YC separation by 1 line memory, Video blocks including sharpness, YNR, a high performance black-stretch circuits, Chroma decoder, and RGB matrix including OSD mixing circuit.
(3) Deflection block; A high performance sync separation by analog and digital mixed solution.
(4) Analog backend block; 3 channels 10 bit high speed video DACs for Cutoff & Drive, and Mute circuit.

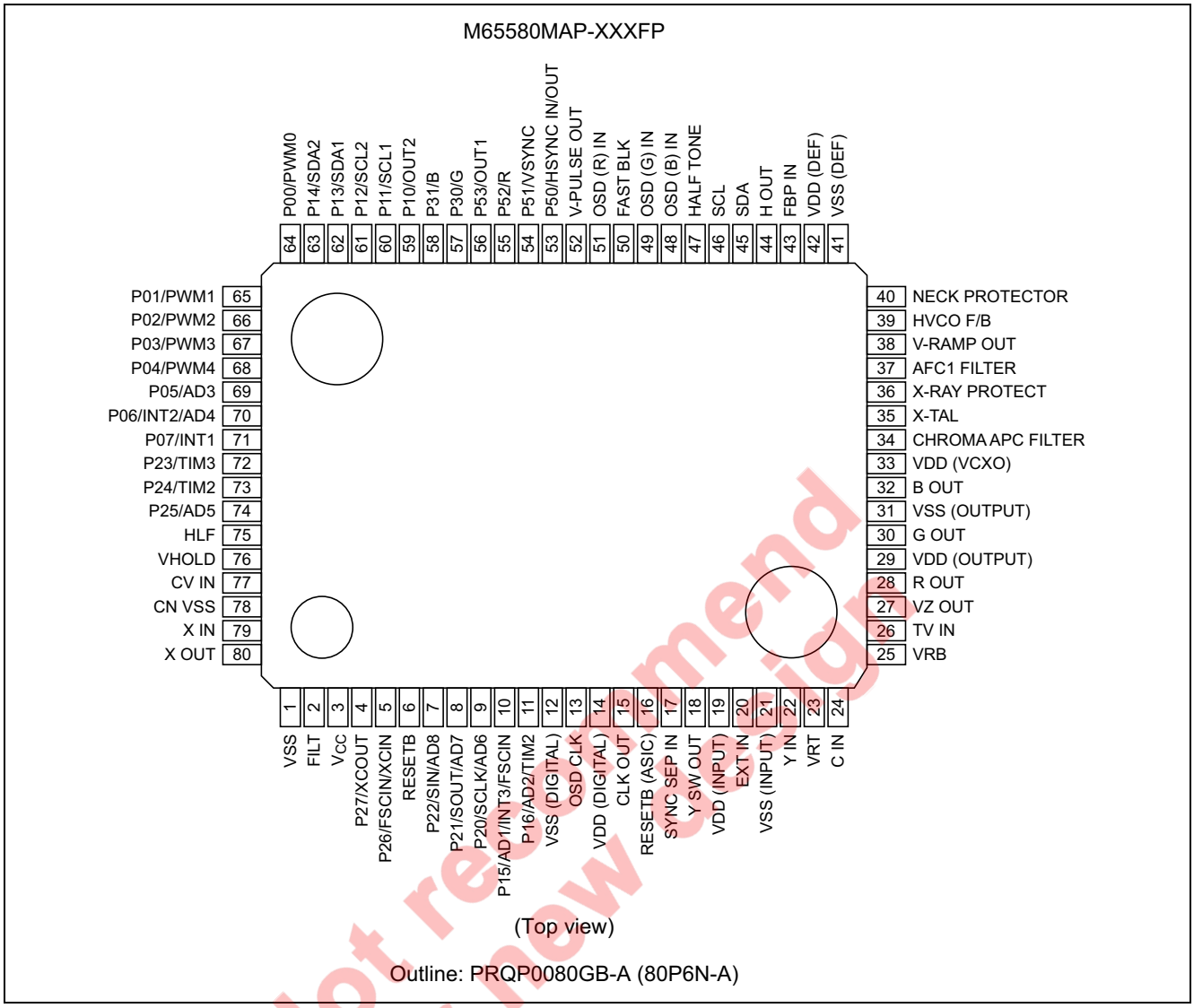
Application

NTSC TV with a closed caption decoder

Block Diagram (Whole)



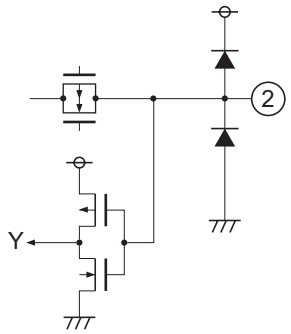
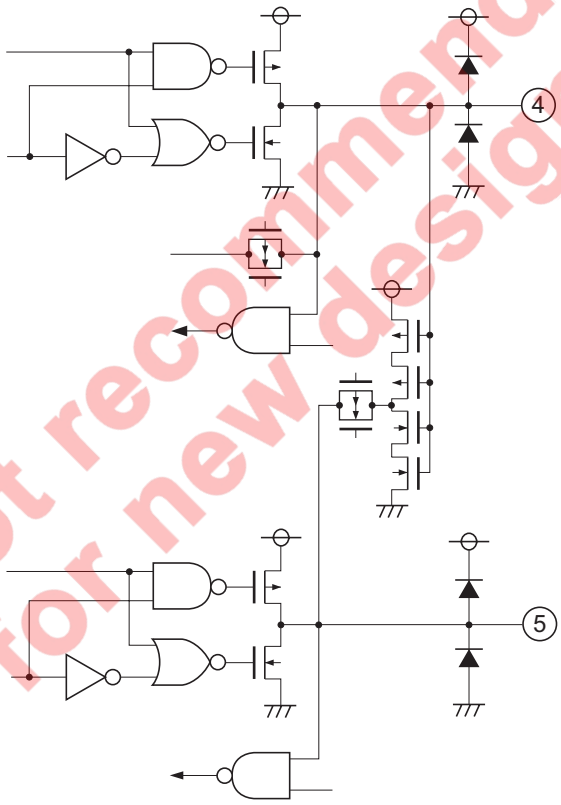
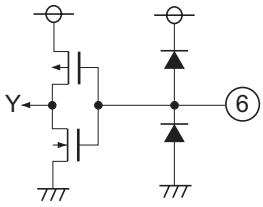
Pin Arrangement

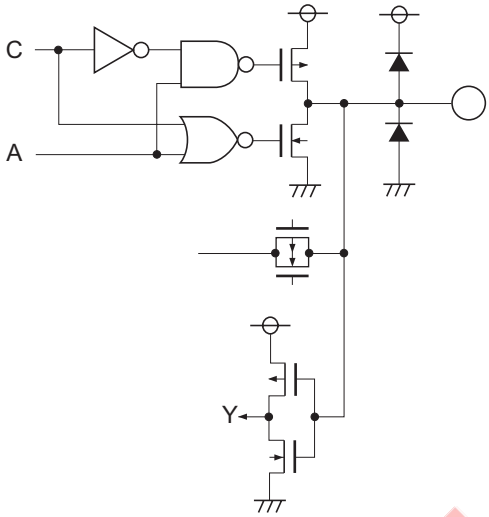
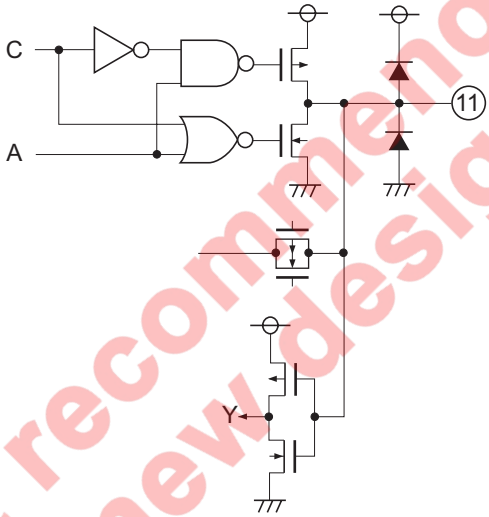
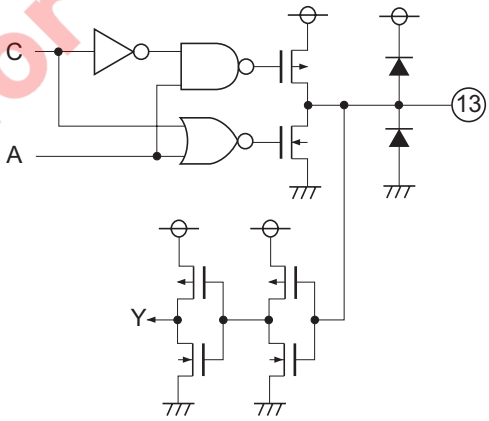


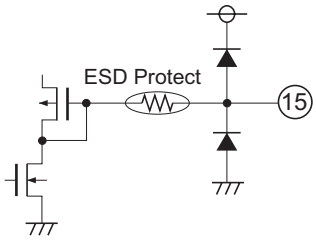
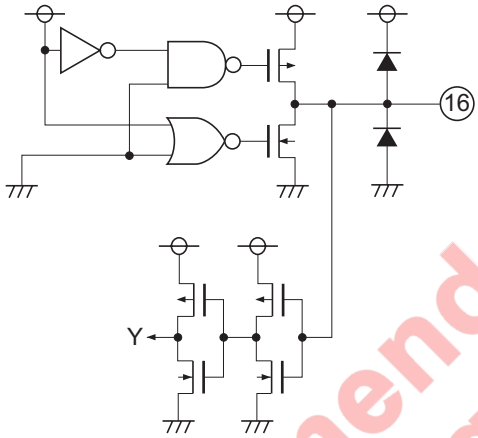
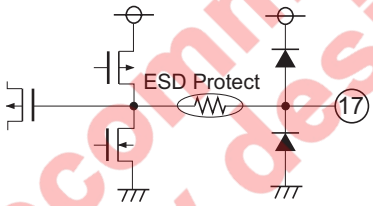
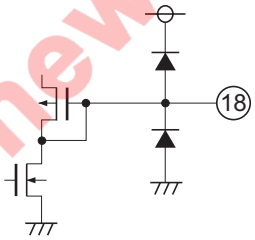
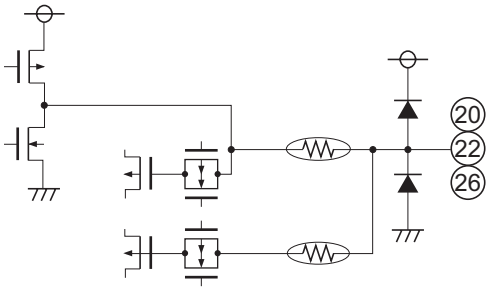
(Top view)

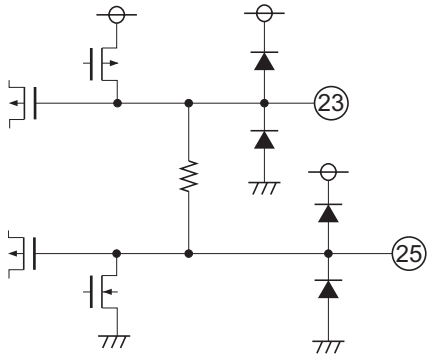
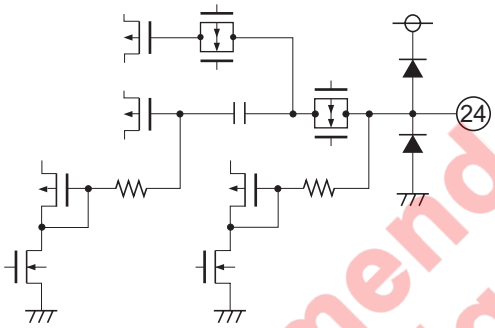
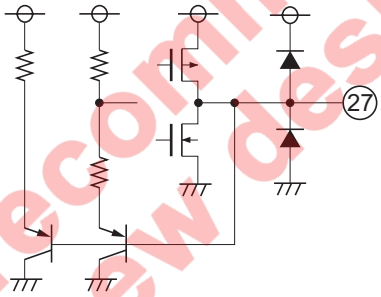
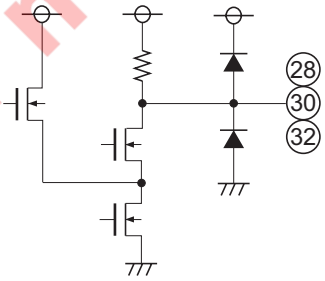
Outline: PRQP0080GB-A (80P6N-A)

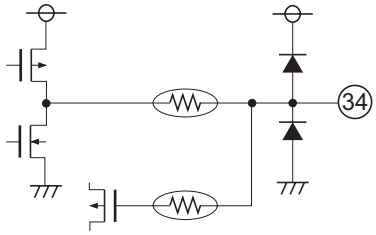
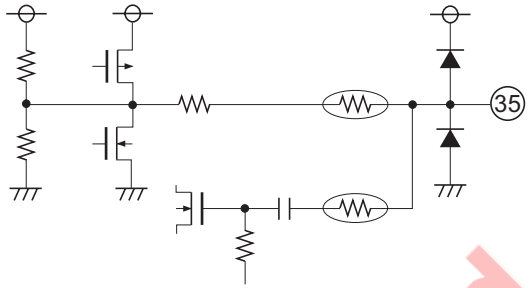
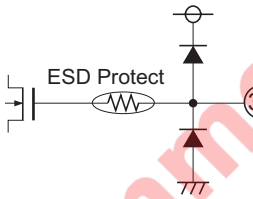
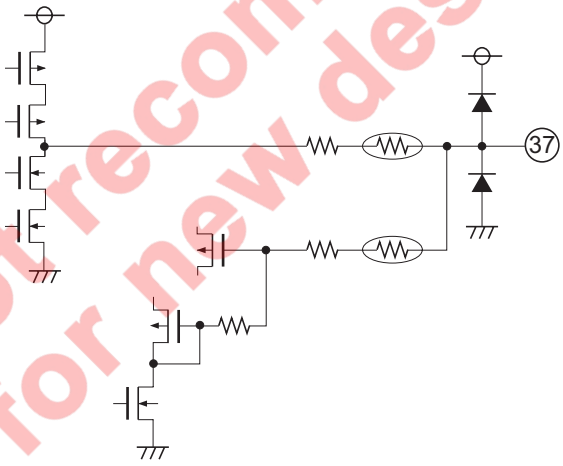
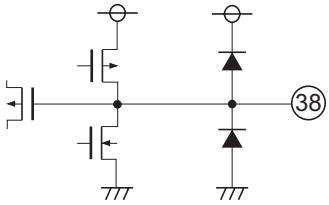
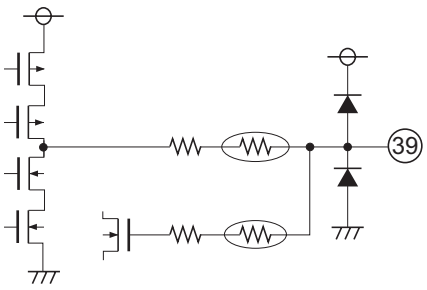
Pin Description

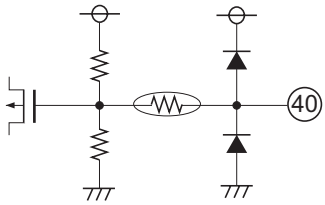
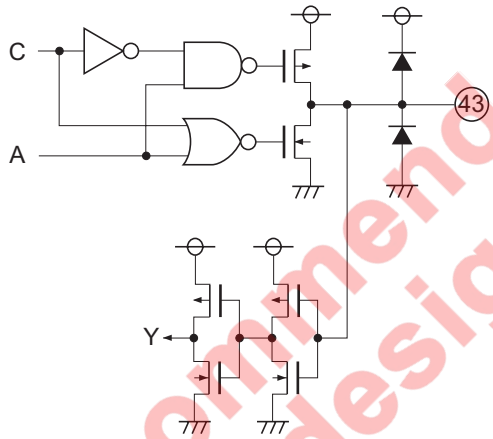
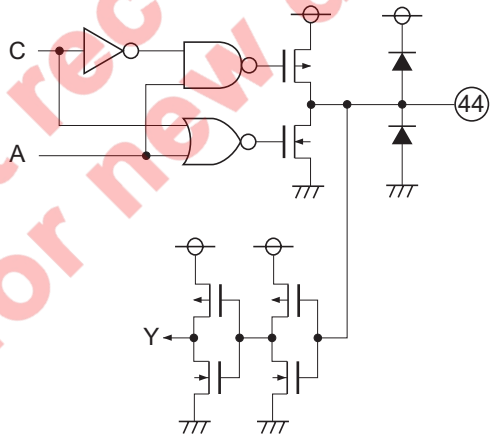
Pin No.	Name	Peripheral Circuit of Pins	Note
1	Vss (MCU)	—	Power source for MCU. 0 V
2	FILT		
3	V_{CC} (MCU)	—	Power source for MCU. 5.0 V ± 5%
4 5	P27/XCONT P26/FSCIN/XCIN		
6	RESETB		CMOS INPUT (Impedance > 100 kΩ) V_{OL} = 0 V: Reset state V_{OH} = 5 V: Release from reset state

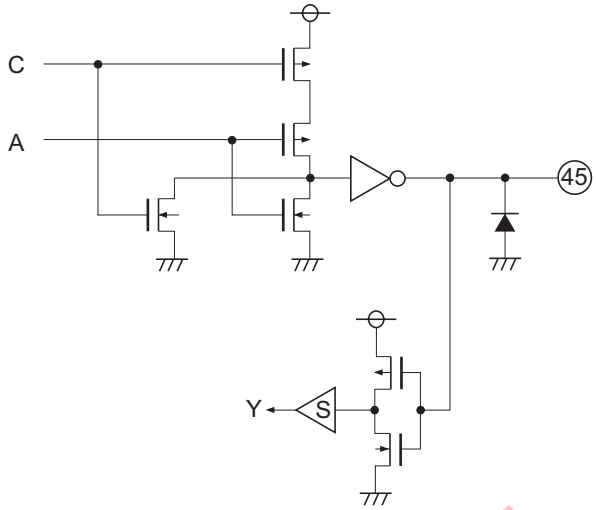
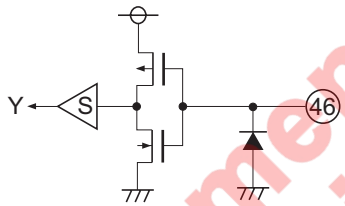
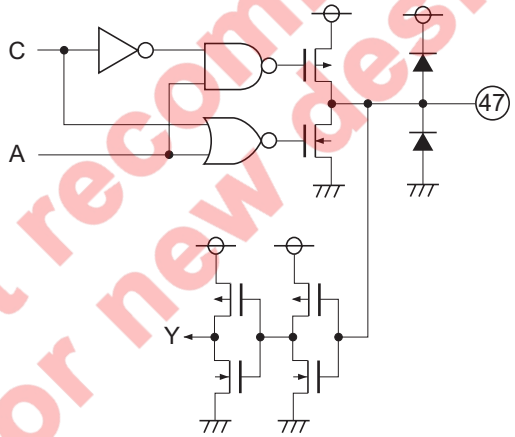
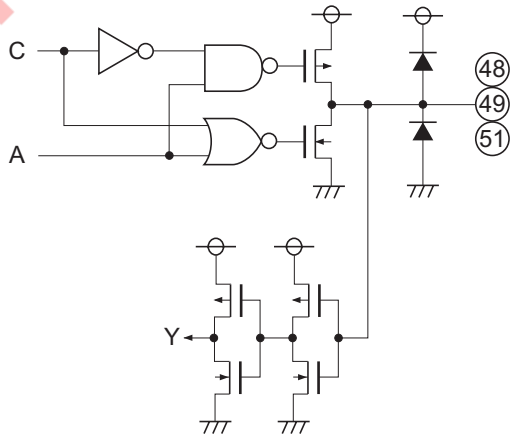
Pin No.	Name	Peripheral Circuit of Pins	Note
7 8 9 10	P22/SIN/AD8 P21/SOUT/AD8 P20/SCLK/AD6 P15/AD1/INT3/FSCIN		CMOS IN/OUT 1 Impedance > 100 kΩ (input) Impedance ≈ 250 Ω (output)
11	P16/AD2/TIM2		CMOS IN/OUT 1 Impedance > 100 kΩ (input) Impedance ≈ 250 Ω (output) Intelligent monitor output (Analog/Digital)
12	Vss (Digtal)	—	0 V
13	OSD CLK		CMOS IN/OUT 1 Impedance > 100 kΩ (input) Impedance < 100 Ω (output)
14	Vdd (Digital)	—	Power source for digital block. 5.0 V ± 5%

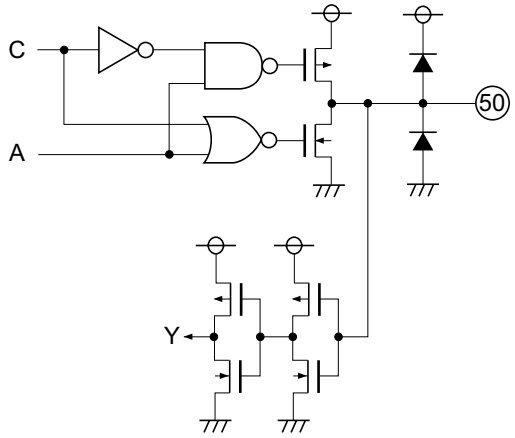
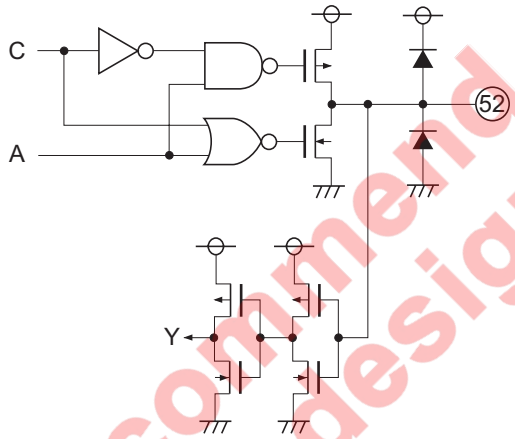
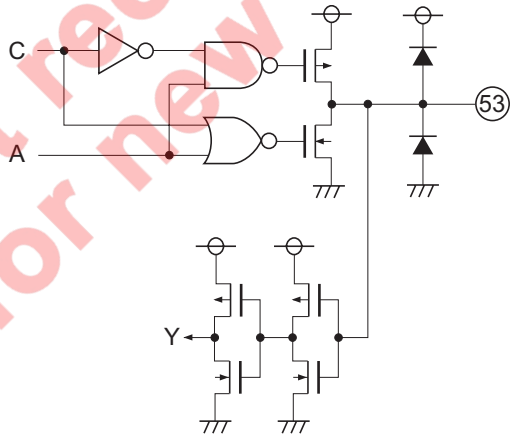
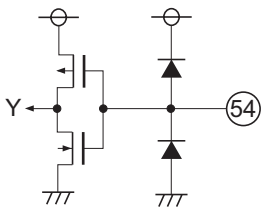
Pin No.	Name	Peripheral Circuit of Pins	Note
15	CLK OUT		Impedance ≈ 400 Ω
16	RESET		CMOS INPUT (Impedance > 100 kΩ) V_{IL} = 0 V: Reset state V_{IH} = 5 V: Release from reset state
17	C.Sync IN		Sync Sep. input impedance = N.A. DC 2.5 V
18	CVBS OUT		Impedance ≈ 150 Ω DC: 0.55 V (sync) AC: 1.75 Vp-p (typ.)
19	Vdd (Input)	—	Power source for A/D etc. 3.3 V ± 5%
20 22 26	EXT (CVBS) IN Y IN TV (CVBS) IN		Impedance = N.A. DC: 0.5 V (sync) AC: 1.0 Vp-p (typ.)
21	Vss (Input)	—	Power source for A/D etc. 0 V

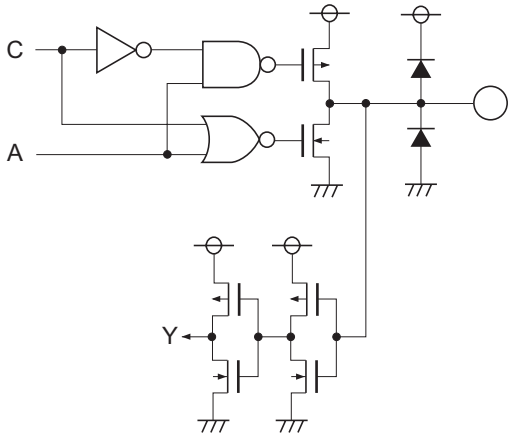
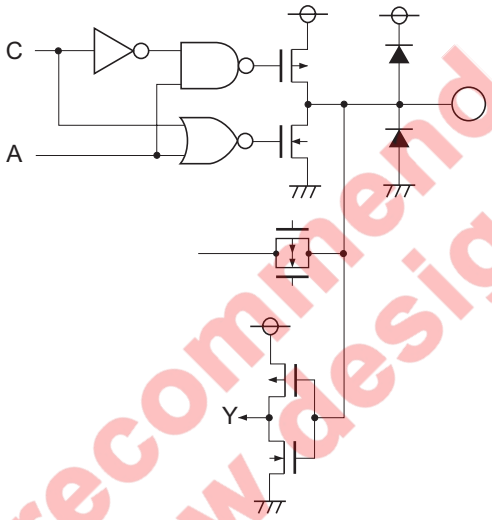
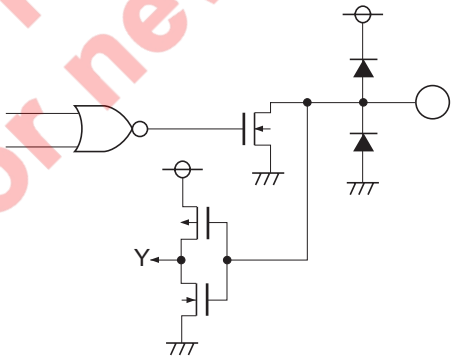
Pin No.	Name	Peripheral Circuit of Pins	Note
23 25	VRT VRB		Impedance > 50 Ω DC: 1.7 V (VRT) 0.5 V (VRB)
24	C IN		Impedance ≈ 7.5 kΩ DC: 1.0 V AC: 0.286 Vp-p (burst)
27	VZ OUT		Impedance ≈ 400 Ω DC: 2.05 V
28 30 32	R OUT G OUT B OUT		Impedance ≈ 1 kΩ DC: 3 V (blanking)
29	Vdd (Output)	—	Power source for D/A etc. 3.3 V ± 5%
31	Vss (Output)	—	Power source for D/A etc. 0 V
33	Vdd (VCXO)	—	Power source for VCXO etc. 5.0 V ± 5%

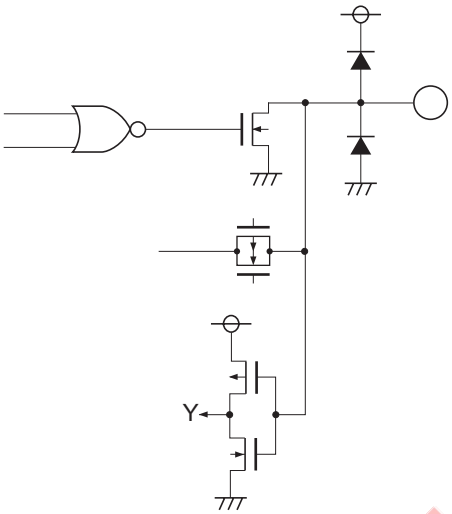
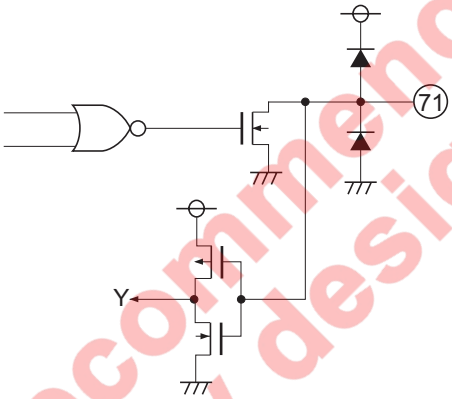
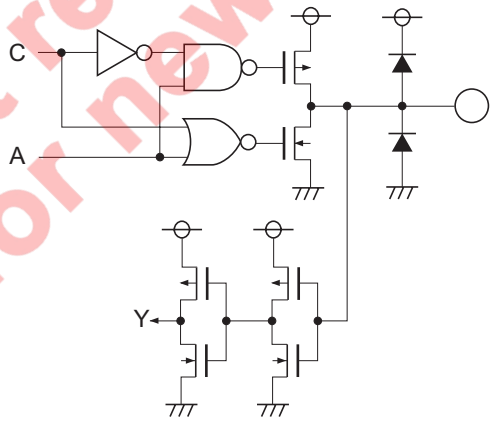
Pin No.	Name	Peripheral Circuit of Pins	Note
34	APC Filter		Impedance = N.A. (Additional filter on PCB Board) DC: 2.9 V
35	X'tal		Impedance ≈ 1 kΩ
36	X-ray Protector		Impedance > 100 kΩ 0.0-3.0: Normal 3.2-3.3: Hold down 3.7-5.0: Shut down
37	AFC1 Filter		Impedance = N.A. (Additional filter on PCB Board) DC: 2.5 V
38	V RAMP OUT		Impedance ≈ 400 Ω 2.5 Vp-p (typ.)
39	HVCO F/B		Impedance = N.A. (Additional filter on PCB Board) DC: 3.0 V

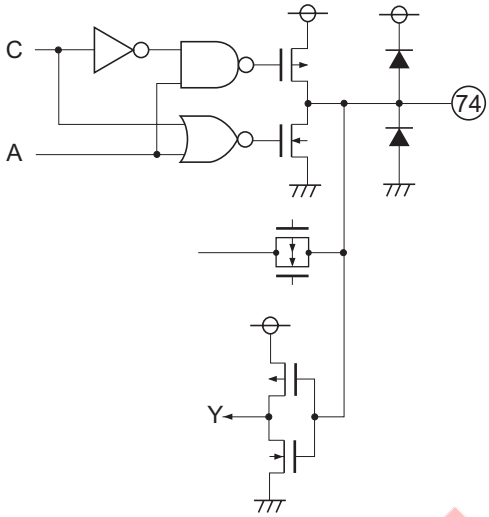
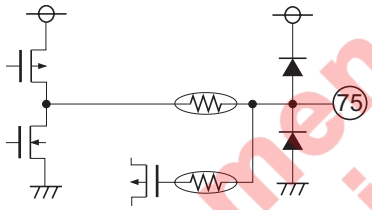
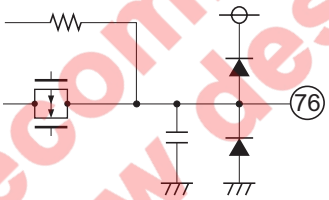
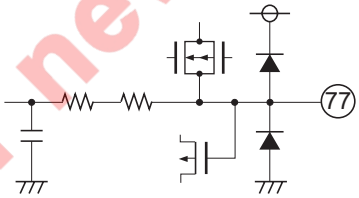
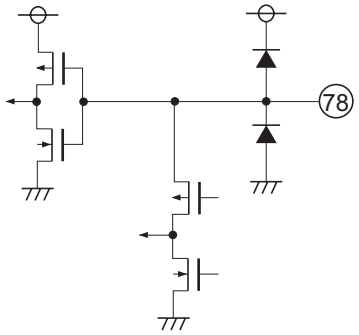
Pin No.	Name	Peripheral Circuit of Pins	Note
40	Neck Protector		Impedance ≈ 5 kΩ 0.0-1.0: RGB off 1.6-3.0: Normal 4.0-5.0: Test mode
41	Vss (DEF)	—	Power source for deflection block. 0 V
42	Vdd (DEF)	—	Power source for deflection block. 5.0 V ± 5%
43	FBP IN		CMOS IN/OUT 1 Impedance > 100 kΩ (input) Impedance < 100 Ω (output) V_{IL} = 0 V: RGB output V_{IH} = 5 V: Blanking
44	H OUT		CMOS IN/OUT 1 Impedance > 100 kΩ (input) Impedance < 100 Ω (output) V_{OL} = 0 V V_{OH} = 5 V

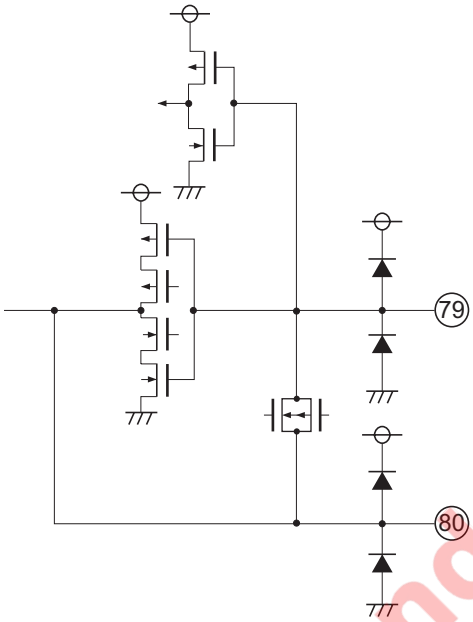
Pin No.	Name	Peripheral Circuit of Pins	Note
45	SDA		CMOS IN/OUT 2 Impedance > 100 kΩ (input) Impedance < 100 Ω (output) V_{IL} = 0 V V_{IH} = 5 V
46	SCL		CMOS Schmitt IN Impedance > 100 kΩ V_{IL} = 0 V V_{IH} = 5 V
47	Half Tone IN		CMOS IN/OUT 1 Impedance > 100 kΩ (input) Impedance < 100 Ω (output) V_{IL} = 0 V: RGB output V_{IH} = 5 V: Half tone on
48 49 51	OSD (B) IN OSD (G) IN OSD (R) IN		CMOS IN/OUT 1 Impedance > 100 kΩ (input) Impedance < 100 Ω (output) V_{IL} = 0 V V_{IH} = 5 V

Pin No.	Name	Peripheral Circuit of Pins	Note
50	Fast BLK IN		CMOS IN/OUT 1 Impedance > 100 kΩ (input) Impedance < 100 Ω (output) V_{IL} = 0 V: RGB output V_{IH} = 5 V: OSD output
52	V sync OUT		CMOS IN/OUT 1 Impedance > 100 kΩ (input) Impedance < 100 Ω (output) V_{OL} = 0 V V_{OH} = 5 V
53	H sync OUT		CMOS IN/OUT 1 Impedance > 100 kΩ (input) Impedance < 100 Ω (output) V_{OL} = 0 V V_{OH} = 5 V
54	P51/VSYNC		CMOS INPUT Impedance > 100 kΩ

Pin No.	Name	Peripheral Circuit of Pins	Note
55 56 57 58 59	P52/R P53/OUT1 P30/G P31/B P10/OUT2		CMOS IN/OUT 1 Impedance > 100 kΩ (input) Impedance < 100 Ω (output)
60 61 62 63	P11/SCL1 P12/SCL2 P13/SDA1 P14/SDA2		CMOS IN/OUT 1 Impedance > 100 kΩ (input) Impedance ≈ 250 Ω (output)
64 65 66 67 68	P00/PWM0 P01/PWM1 P02/PWM2 P03/PWM3 P04/PWM4		CMOS IN/OUT Impedance > 100 kΩ (input) Impedance ≈ 250 Ω (output)

Pin No.	Name	Peripheral Circuit of Pins	Note
69 70	P05/AD3 P06/INT2/AD4		CMOS IN/OUT Impedance > 100 kΩ (input) Impedance ≈ 250 Ω (output)
71	P07/INT1		CMOS IN/OUT Impedance > 100 kΩ (input) Impedance ≈ 250 Ω (output)
72 73	P23/TIM3 P24/TIM2		CMOS IN/OUT 1 Impedance > 100 kΩ (input) Impedance < 100 Ω (output)

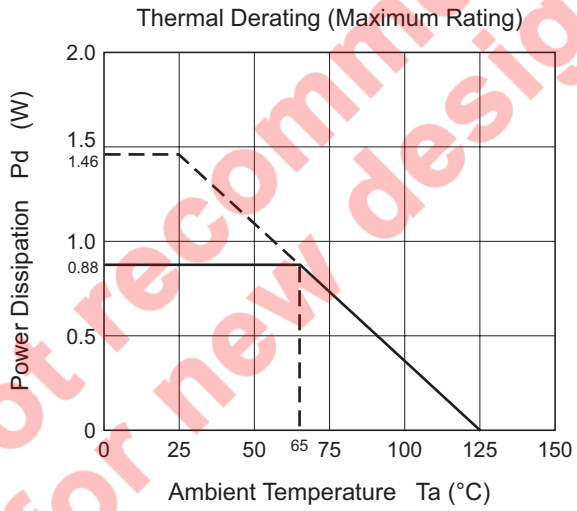
Pin No.	Name	Peripheral Circuit of Pins	Note
74	P25/AD5		CMOS IN/OUT 1 Impedance > 100 kΩ (input) Impedance ≈ 250 Ω (output)
75	HLF		Impedance = N.A. (Additional filter on PCB board)
76	VHOLD		
77	CV IN		
78	CN VSS		CMOS IN/OUT Impedance > 100 kΩ (input) Impedance ≈ 250 Ω (output)

Pin No.	Name	Peripheral Circuit of Pins	Note
79 80	X IN X OUT		

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage (MCU)	V_{DD} (MCU)	–0.3 to 6.0	V	All voltage are based on Vss. Output transistors are cut off.
Supply voltage (ASIC 5 V)	V_{DD} (ASIC 5 V)	–0.3 to 6.0	V	
Supply voltage (ASIC 3.3 V)	V_{DD} (ASIC 3.3 V)	–0.3 to 4.0	V	
Input voltage (MCU)	V_I (MCU)	–0.3 to V_{CC}+0.3	V	
Output voltage (MCU)	V_O (MCU)	–0.3 to V_{CC}+0.3	V	
Circuit current (MCU)	I_{OH} (MCU)	0 to 1 Note1	mA	
Circuit current (P00-P07, P10, P15, P16, P20-P27, P30, P31, P52, P53)	I_{OL1} (MCU)	0 to 2 Note2	mA	
Circuit current (P11-P14)	I_{OL2} (MCU)	0 to 6 Note2	mA	
Digital input voltage	V_{ID} (ASIC)	–0.3 to V_{CC}+0.3	V	
Analog output current	I_{OUT} (ASIC)	–30	mA	
Power dissipation	Pd	1460	mW	
Thermal derating	Kθ	14.6	mW/°C	
Operating temperature	Topr	–20 to 65	°C	
Storage temperature	Tstg	–40 to 125	°C	

Notes: 1. The total current that flows out the MCU must be 20 mA or less.
2. The total input current to MCU (I_{OL1} + I_{OL2}) must be 30 mA or less.



Recommended Operating Condition

(Ta = –20 to 65°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit
Supply voltage (MCU) Note3		V_{DD} (MCU)	4.75	5.0	5.25	V
Supply voltage (Digital)		V_{DD} (Digital)	4.75	5.0	5.25	V
Supply voltage (Input)		V_{DD} (Input)	3.13	3.3	3.47	V
Supply voltage (Output)		V_{DD} (Output)	3.13	3.3	3.47	V
Supply voltage (VCXO)		V_{DD} (VCXO)	4.75	5.0	5.25	V
Supply voltage (DEF)		V_{DD} (DEF)	4.75	5.0	5.25	V
High input voltage	P00-P07, P10-P16, P20-P27, P50, P51, RESETB, X_{IN}	V_{IH1} (MCU)	0.8 V_{CC}	—	V_{CC}	V
High input voltage	SCL1, SCL2, SDA1, SDA2 (When using I^2C-Bus)	V_{IH2} (MCU)	0.7 V_{CC}	—	V_{CC}	V
High input voltage	RESETB, FBP IN, HALF TONE, OSD (R/G/B) IN, FAST BLK	V_{IH3} (ASIC)	0.8 V_{CC}	—	V_{CC}	V
Low input voltage	P00-P07, P10-P16, P20-P27	V_{IL1} (MCU)	0	—	0.4 V_{CC}	V
Low input voltage	SCL1, SCL2, SDA1, SDA2 (When using I^2C-Bus)	V_{IL2} (MCU)	0	—	0.3 V_{CC}	V
Low input voltage Note4	P50, P51, RESETB, X_{IN}, TIM2, TIM3, INT1, INT2, INT3, S_{IN}, S_{CLK}	V_{IL3} (MCU)	0	—	0.2 V_{CC}	V
Low input voltage	RESETB, FBP IN, HALF TONE, OSD (R/G/B) IN, FAST BLK	V_{IL4} (ASIC)	0	—	0.2 V_{CC}	V
High average output current Note1	P10-P16, P20-P27, P30, P31, P52, P53	I_{OH} (MCU)	—	—	1	mA
Low average output current Note2	P00-P07, P10, P15, P16, P20-P27, P30, P31, P52, P53	I_{OL1} (MCU)	—	—	2	mA
Low average output current Note2	P11-P14	I_{OL2} (MCU)	—	—	6	mA
Oscillation frequency (for CPU operation) Note5	X_{IN}	f(X_{IN}) (MCU)	7.9	8.0	8.1	MHz
Oscillation frequency (for sub-clock operation)	X_{CIN}	f(X_{CIN}) (MCU)	29	32	35	kHz
Oscillation frequency (for OSD standard clock)	FSC_{IN}	FSC_{IN} (MCU)	—	3.58	—	MHz
Input frequency	TIM2, TIM3, INT1, INT2, INT3	f_{hs1} (MCU)	—	—	100	kHz
Input frequency	S_{CLK}	f_{hs2} (MCU)	—	—	1	MHz
Input frequency	SCL1, SCL2	f_{hs3} (MCU)	—	—	400	kHz
Input amplitude video signal	CV_{IN}	V_I (MCU)	1.5	2.0	2.5	V

Notes: 1. The total current that flows out the MCU must be 20 mA or less.

2. The total input current to MCU (I_{OL1} + I_{OL2}) must be 30 mA or less.
3. Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit. When using the data slicer, use 8 MHz.
4. Pin name in each parameter is described pin names.
   (1) Dedicated pins: dedicated pin name.
   (2) Double-/Triple-function ports.
   When the same limits: I/O port name.
   When the limits of function except ports are different from I/O port limits; function pin name.
5. P06, P07, P15, P23, P24 have the hysteresis when these pins are used as interrupt input pins or timer pins.
   P11-P14 have the hysteresis when these pins are used as multi-master I^2C-Bus interface ports.
   P20-P22 have the hysteresis when these pins are used as serial I/O pins.

[MCU Block (M37272MA)]

Description

MCU (single microcomputers) in this IC has almost same function and performance as M37272MA-XXXSP/FP in mass production. And it is operated by simple instruction in the same memory space as that of built-in ROM, RAM, I/O. It has an OSD, data slicer, and I^2C-BUS interface, so it is very useful for a channel selection system for NTSC TV with a closed caption decoder.

Features

- Number of basic instructions 71
- Memory size ROM ..... 40 Kbytes
  RAM ..... 1152 bytes (ROM correction memory: 64 bytes included)
- Minimum instruction execution time ..... 0.5 µs
  (at 8 MHz oscillation frequency)
- Power source voltage ..... 5 V ± 10%
- Subroutine nesting ..... 128 levels (max.)
- Interrupts ..... 17 bytes 16 vector
- 8-bit timers 6
- Programmable I/O ports (Ports P0, P1, P2) 23
- Input ports (Ports P50, P51) 2
- Output ports (Ports P30, P31, P52, P53) 4
- Serial I/O ..... 8-bit × 1channel
- Multi-master I^2C-BUS interface ..... 1 (2 systems)
- A/D comparator (7-bit resolution) ..... 8 channels
- PWM output circuit ..... 8-bit × 5
- ROM correction function ..... 32 bytes × 2
  Power dissipation ..... 165 mW
  (at V_{CC} = 5.5 V, 8 MHz oscillation frequency, OSD on, and Data slicer on)
- Closed caption data slicer
- OSD function
  Display characters ..... 32 characters × 2 lines (possible to display 3 lines or more by software)
  Kinds of characters 254 kinds
  Character display area CC mode: 16 × 26 dots
  OSD mode: 16 × 20 dots
  Kinds of character sizes CC mode: 1 kind
  OSD mode: 8 kinds
  Kinds of character colors 8 colors (R, G, B) (coloring unit: a character)
  Kinds of background colors CC mode: 1 kind (black)
  OSD mode: 8 kinds (possible to select color in character unit)
  Display position horizontal: 128 levels, Vertical: 512 levels
  Attribute CC mode: smooth italic, underline, flash, automatic solid space
  OSD mode: border (black)
  Kinds of raster colors 8 kinds
  Smooth roll-up
  Window function

[ASIC Block]

Description

CVBS (TV/EXT) signals or Y/C signals input to this IC are converted to 8 bit digital signal by 2 channels high speed video ADCs. These signals are input to digital section to obtain high performance R/G/B signals. First, CVBS signals are separated to high quality Y/C signals by 2 dimensional adaptive YC separation circuit, and then Y/C signals are converted to R-Y & B-Y signals by digital chroma decoder, after that, to R/G/B signals by RGB matrix circuit. These signals are mixed with OSD signals come from MCU block, are converted to analog R/G/B signals by 3 channel 10 bit high speed video DACs. In deflection block, to get a better Horizontal & Vertical signals, a conventional analog solution by analog CMOS technology is used.

ASIC block consists of the followings blocks.

(1) Analog front-end block; Analog SW (2 CVBS (TV & EXT) inputs, Y/C signals to one signal), 2 channels 8 bit high speed video ADCs, and ACC amplifiers.
(2) Video and Chroma block; A high performance 2 line adaptive YC separation by 1 line memory, Video blocks including sharpness, YNR, a high performance black-stretch circuits, Chroma decoder, and RGB matrix including OSD mixing circuit.
(3) Deflection block; A high performance sync separation by analog and digital mixed solution.
(4) Analog backend block; 3 channels 10 bit high speed video DACs for Cutoff & Drive, and Mute circuit.

Features

[Video/Chroma Block]

- Built-in 1 Video SW for TV/EXT signal input
- 2 additional pins for S (Y/C) input
- YUV input signal available (T.B.D)
- 2 channel 8 bit Video ADCs for CVBS (TV & EXT) or Y/C signal inputs
- Built-in adaptive 2 line comb filter (2DYCS) ⇒ Few dot crawl & cross-color, and clear color transition
- Built-in a high performance Black-stretch ⇒ Dynamic & detailed picture
- Digital Luminance delay circuit ⇒ stable Y/C timing adjustment
- Built-in VCXO circuit (4 fsc)
- High resolution R/G/B output ⇒ Built-in 10 bit high speed Video DACs
- Internal connection of 8 color digital OSD (R/G/B, F.B, H.T)
- Reference CLK output for tuner (fsc or 4 MHz)
- Built-in YNR (about fsc ± 1 MHz)
- Gamma correction (for R/G/B signals)

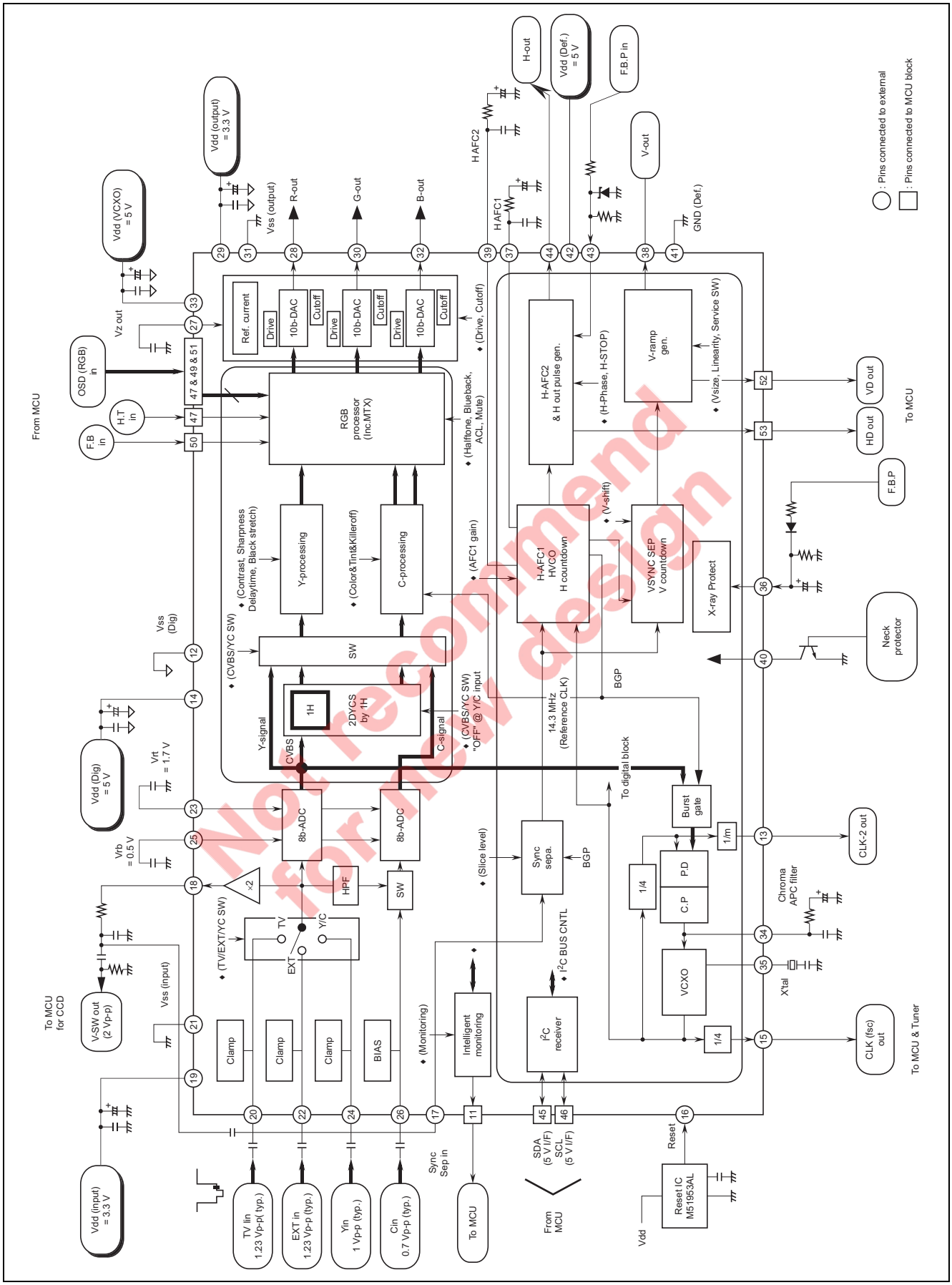
[Deflection Block]

- Analog (conventional) sync separation ⇒ Better performance by abundant experience
- Double AFC Circuit ⇒ Stable Horizontal scanning
- Built-in Horizontal reference Oscillator ⇒ No ceramic resonator and Adjustment free
- HD and VD pulse by Countdown ⇒ Stable HD & VD
- Built-in digital Vramp generator

[List of Main I^2C Bus Controllable Items]

- Chip: Power-down mode
- Analog Input Stage: CVBS/Y & C Input SW
- Luminance Processing: Sharpness, Black-stretch
- Chroma Processing: Color, Tint, Killer level
- RGB Matrix: ACL, OSD Input Level, Contrast, Brightness
- Analog Output Stage: Drive adj.(R/G/B), Cutoff adj.(R/G/B)
- Deflection Block: H-Phase, V-size, V-shift, V-Linearity

ASIC Block Detailed Diagram



Function and Outline of ASIC Block

Chip

Power down mode:	3 modes [PD0 & PD1 & PD2]
Service SW:	stop of Vertical (Vramp) output (For cutoff adjustment)

Analog Block

- Input stage ⇒ CVBS & Y/C input signals

Input level (CVBS):	1.23 Vp-p (173 IRE) @max. / 1.0 Vp-p @typ.
Input level (Y/C):	Y: 1.00 Vp-p (140 IRE) @typ. / C: 0.7 Vp-p @typ.

- Output stage ⇒ RGB output signals

Output level:	0.7 Vp-p (typ.)
Drive (R & G & B):	–3 to +4 dB by 7 bit (White Balance)
Cutoff (R & G & B):	0.5 V by 9 bit (Start lighting point)

Digital Block

- 2DYCS

  Adaptive YC separation by using of 1H line memory and original algorithm
- Luminance processing

Contrast:	0 to 200 LSB by 7 bit
Brightness:	–20 to 20 LSB by 8 bit (Pedestal DC level)
Sharpness:	0 to 3 dB by 5 bit (by 0, 70, 140, 210 ns)
Delay adjustment:	0 to 210 ns by 2 bit (70 ns step) to Chroma signal
Black-stretch:	3 selectable stretch point
	[Stretch areas (0 to 25/30/40 IRE), through areas (25/30/40 IRE ~)]
	4 selectable black-stretch curves (1/4, 2/4, 3/4, 4/4)

- Chroma processing

Tint:	–45 to 45 degree by 7 bit ⇒ about 0.7 degree
	Variable demodulator (R-Y) axis
	(–22.5 to +22.5 degree by 6 bit ⇒ about 0.7 degree)
Color:	0 to 200% by 7 bit

- RGB matrix

	Matrix (R-Y signal) ratio selectable (12/8, 13/8, 14/8)
ACL:	Automatic Contrast Limiter by MCU port (ADC) and I^2C bus
EXT/RGB:	clip to 7 LSB @ data < 0Fh
BlueBack:	ON/OFF selectable
Mute:	ON/OFF of R/G/B output
Neck Protector:	R/G/B output to zero (no signal)

Deflection Block

- Horizontal Output

AFC2 phase:	+5 to –5 µs by 5 bit
Hold ⇒ Shut down:	fh@Hold-down: in about 16.5 kHz ⇒ fh@Shutdown: H-STOP
AFC1 gain:	Normal/High selectable for VTR skew

- Vertical Output

V position:	0 to 16 H by 3 bit ⇒ 2H unit (connected with BLK)
V size:	1.4 to 2.6 V by 7 bit
Linearity:	0 to 30% by 7 bit

Electrical characteristics

(Ta = 25°C, Vdd = 5.0 V, 3.3 V)

Item	Symbol	Limits			Unit	Input Signal		Test Point	Remarks
		Min	Typ	Max		Pins	SG		
Standard conditions	ICC	—	—	—	—	—	—	—	
5.0 V supply current	ICC50	102	116	130	mA	—	—	3, 14, 33, 42	Supply of MCU, Digital, VCXO and Deflection
3.3 V supply current	ICC33	47	56	65	mA	—	—	18, 29	Supply of A/D and D/A
Standard conditions of video character	VIDEO	—	—	—	—	—	—	—	
Video SW output level (TV input)	2AGTV	1.5	1.7	1.9	Vp-p	26	SG.A	18	
Video SW output level (External input)	2AGEV	1.5	1.7	1.9	Vp-p	20	SG.A	18	
Video standard output	Vtyp	590	740	890	mVp-p	26	SG.A	28, 30, 32	
Video frequency characteristics	FBY	–3	0	3	dB	26	SG.B	28, 30, 32	f = 5 MHz
Y/C separation function 1	Y/C1	—	–30	–20	dB	26	SG.E	28, 30, 32	feb = fec = fsc
Y/C separation function 2	Y/C2	–3	0	3	dB	26	SG.E	28, 30, 32	feb = fsc, fec = fsc $\pm 1/2f_H$
Y/C separation function 3	Y/C3	—	–30	–20	dB	26	SG.E	28, 30, 32	feb = fsc, fec = fsc $\pm f_H$
Y total delay time	YDL0	2.4	3.0	3.6	µs	26	SG.A	28, 30, 32	
Y delay time 1	YDL1	50	70	90	ns	26	SG.A	28,30, 32	YDL1 = measure – YDL0
Y delay time 2	YDL2	50	70	90	ns	26	SG.A	28,30, 32	YDL2 = measure – YDL1
Y delay time 3	YDL3	50	70	90	ns	26	SG.A	28,30, 32	YDL3 = measure – YDL2
Video tone control characteristic 1	GTnor	640	800	960	mV	26	SG.B	28,30, 32	f = 2.5 MHz
Video tone control characteristic 2	GTmax	1	2.5	4	dB	26	SG.B	28,30, 32	f = 2.5 MHz
Video tone control characteristic 3	GTmin	–7	–4	–1	dB	26	SG.B	28,30, 32	f = 2.5 MHz
Black-stretch characteristic	BLS	20	50	80	mV	26	SG.D	28,30, 32	Vy = 0.18 V, 45H = 80h (BLS ON) / 00h (BLS OFF)
Half Tone function	HT	–9	–6	–3	dB	26	SG.A	28,30, 32	

Electrical characteristics (cont.)

Item	Symbol	Limits			Unit	Input Signal		Test Point	Remarks
		Min	Typ	Max		Pins	SG		
Standard condition of chroma parameter	CHROMA	—	—	—	—	—	—	—	5DH = 03h
Chroma standard output (R-Y)	CnorR	155	180	205	mV	26	SG.E	28	feb = fec + 50 kHz
Chroma standard output (B-Y)	CnorB	275	310	345	mV	26	SG.E	32	feb = fec + 50 kHz
ACC characteristic 1	ACC1	–3	0	3	dB	26	SG.E	28	Veb, Vec: +6 dB of typical input level
ACC characteristic 2	ACC2	–3	0	3	dB	26	SG.E	28	Veb, Vec: –20 dB of typical input level
Killer operation input level	VikN	–40	–35	–30	dB	26	SG.E	28	Veb, Vec: variable
Color residual at killer on	KillP	—	–40	–28	dB	26	SG.E	28	Veb = 0 mV
APC pull-in range (upper)	APCU	400	—	—	Hz	26	SG.E	28	feb = fec: variable
APC pull-in range (lower)	APCL	—	—	–400	Hz	26	SG.E	28	feb = fec: variable
Demodulated output ratio	DEMR	0.47	0.57	0.67	—	26	SG.E	28, 32	feb = fec + 50 kHz
Demodulation phase angle	DEMP	85	90	95	deg	26	SG.F	28, 32	
Color control characteristic 1	Ccon 1	160	200	240	%	26	SG.E	28	feb = fec + 50 kHz
Color control characteristic 2	Ccon 2	—	0	10	%	26	SG.E	28	feb = fec + 50 kHz
TINT control characteristic 1	TC1	30	45	60	deg	26	SG.F	28, 32	
TINT control characteristic 2	TC2	–60	–45	–30	deg	26	SG.F	28, 32	
CLK output frequency	Fclk	3.578	3.579	3.580	MHz	26	SG.C	15	
CLK output amplitude	Vclk	350	500	650	mVp-p	26	SG.C	15	

Electrical characteristics (cont.)

Item	Symbol	Limits			Unit	Input Signal		Test Point	Remarks
		Min	Typ	Max		Pins	SG		
Standard condition of RGB parameter	RGB	—	—	—	—	—	—	—	
Output pedestal voltage	VPED	2.7	3.0	3.3	V	26	SG.D	28, 30, 32	Vy = 0.0 V
Matrix ratio R/B	MTXRB	0.74	0.92	1.10	—	26	SG.H	28, 32	
Matrix ratio G/B	MTXGB	0.24	0.33	0.42	—	26	SG.H	30, 32	
Contrast control characteristic 1	GYmax	160	200	240	%	26	SG.D	28, 30, 32	Vy = 0.286 V
Contrast control characteristic 2	GYmin	—	0	10	%	26	SG.D	28, 30, 32	Vy = 0.286 V
Contrast control characteristic 5	GYEclip	250	300	350	mV	48, 49, 51	SG.G	28, 30, 32	
Brightness control characteristic 2	Lum max	100	150	200	mV	26	SG.D	28, 30, 32	
Brightness control characteristic 3	Lum min	–200	–150	–100	mV	26	SG.D	28, 30, 32	Vy = 0.286 V
R Drive control characteristic 1	D (R) 1	1.5	3.5	5.5	dB	26	SG.D	28	Vy = 0.286 V
G Drive control characteristic 1	D (G) 1	1.5	3.5	5.5	dB	26	SG.D	30	Vy = 0.286 V
B Drive control characteristic 1	D (B) 1	1.5	3.5	5.5	dB	26	SG.D	32	Vy = 0.286 V
R Drive control characteristic 2	D (R) 2	–4.6	–2.6	–0.6	dB	26	SG.D	28	Vy = 0.286 V
G Drive control characteristic 2	D (G) 2	–4.6	–2.6	–0.6	dB	26	SG.D	30	Vy = 0.286 V
B Drive control characteristic 2	D (B) 2	–4.6	–2.6	–0.6	dB	26	SG.D	32	Vy = 0.286 V
R Cut off control characteristic 1	C (R) 1	210	260	310	mV	26	SG.D	28	Vy = 0.286 V
G Cut off control characteristic 1	C (G) 1	210	260	310	mV	26	SG.D	30	Vy = 0.286 V
B Cut off control characteristic 1	C (B) 1	210	260	310	mV	26	SG.D	32	Vy = 0.286 V
R Cut off control characteristic 2	C (R) 2	–310	–260	–210	mV	26	SG.D	28	Vy = 0.286 V
G Cut off control characteristic 2	C (G) 2	–310	–260	–210	mV	26	SG.D	30	Vy = 0.286 V
B Cut off control characteristic 2	C (B) 2	–310	–260	–210	mV	26	SG.D	32	Vy = 0.286 V
OSD (R) output level	OSD (R)	500	600	700	mVp-p	51	SG.G	28	
OSD (G) output level	OSD (G)	500	600	700	mVp-p	49	SG.G	30	
OSD (B) output level	OSD (B)	500	600	700	mVp-p	48	SG.G	32	
OSD speed characteristic 1	SOSD1	—	100	200	ns	48, 49, 51	SG.G	28, 30, 32	
OSD speed characteristic 2	SOSD2	—	100	200	ns	48, 49, 51	SG.G	28, 30, 32	
Offset voltage between R and OSD (R)	OFF (R)	–50	0	50	mV	—	—	—	Difference at pedestal level
Offset voltage between G and OSD (G)	OFF (G)	–50	0	50	mV	—	—	—	Difference at pedestal level
Offset voltage between B and OSD (B)	OFF (B)	–50	0	50	mV	—	—	—	Difference at pedestal level
Neck protector function threshold voltage	NECK	1.0	1.3	1.6	V	26	SG.A	40	While monitoring at pins 28, 30, 32

Electrical characteristics (cont.)

Item	Symbol	Limits			Unit	Input Signal		Test Point	Remarks
		Min	Typ	Max		Pins	SG		
Standard condition of deflection parameter	DEF	—	—	—	—	—	—	—	
Horizontal free-running frequency 1	fH1	15.53	15.73	15.93	kHz	—	—	44	
Horizontal free-running frequency 2	fH2	13.72	14.32	14.92	kHz	—	—	44	
Horizontal free-running frequency 3	fH3	17.25	17.85	18.45	kHz	—	—	44	
Horizontal pull-in range (upper)	FPHU	250	500	—	Hz	17	SG.I	44	Vary frequency of input signal.
Horizontal pull-in range (lower)	FPHL	—	–500	–250	Hz	17	SG.I	44	Vary frequency of input signal.
Horizontal pulse amplitude	HPV	4.0	4.5	5.0	V	26	SG.A	44	
Horizontal pulse width	HPTW	19.3	22.3	25.3	µs	26	SG.A	44	
Horizontal pulse duty cycle	HPD	30	35	40	%	26	SG.A	44	
Horizontal pulse timing 1	HPT1	8.7	10.7	12.7	µs	26	SG.A	44	
Horizontal pulse timing 2	HPT2	2.2	4.2	6.2	µs	26	SG.A	44	
Horizontal pulse timing variable range	HPT3	4.5	6.5	8.5	µs	26	SG.A	44	HPT2 – HPT1
Hold down function threshold voltage	HDOWN	3.0	3.1	3.2	V	26	SG.A	36	While monitoring at pin 44
Shut down function threshold voltage	SDOWN	3.3	3.5	3.7	V	26	SG.A	36	While monitoring at pin 44
Vertical free-running frequency	fV	55	60	65	Hz	—	—	38	
Service mode function	SVC	2.5	2.8	3.1	V	—	—	38	
Vertical pull-in frequency (upper)	FPVU	—	—	63	Hz	17	SG.J	38	Vary frequency of input signal.
Vertical pull-in frequency (lower)	FPVL	57	—	—	Hz	17	SG.J	38	Vary frequency of input signal.
Vertical ramp size	VRsi 1	2.1	2.5	2.9	Vp-p	26	SG.A	38	
Vertical ramp size control range 1	VRsc 1	20	27	35	%	26	SG.A	38	
Vertical ramp size control range 2	VRsc 2	–35	–27	–20	%	26	SG.A	38	
Vertical ramp linearity control range 1	VLin 1	–5	0	5	%	26	SG.A	38	
Vertical ramp linearity control range 2	VLin 2	19	24	29	%	26	SG.A	38	
Vertical ramp position control range 1	VRpo 1	0	50	200	µs	26	SG.A	38	
Vertical ramp position control range 2	VRpo 2	790	940	1090	µs	26	SG.A	38	(Measured value) – (Vrpo 1)
Vertical pulse width	VW	0.35	0.53	0.65	ms	26	SG.A	52	
Vertical blanking width	VBLKW	1.52	1.64	1.76	ms	26	SG.A	28, 30, 32	
Minimum vertical sync detection width	WVSS	13	18	23	µs	26	SG.A	11	

Electrical Characteristics (MCU Part)

(V_{CC} = 5 V ± 10%, Vss = 0 V, f (X_{IN}) = 8 MHz, Ta = –20°C to 65°C, unless otherwise noted)

Item		Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Circuit	Test Conditions	
Power source current	System operation	I_{CC}	—	15	30	mA	1	V_{CC} = 5.5 V, f (X_{IN}) = 8 MHz	OSD OFF Data slicer OFF
			—	30	45				OSD ON
			—	60	200	µA		V_{CC} = 5.5 V, f (X_{IN}) = 0, f (X_{CIN}) = 32 kHz, OSD OFF, Data slicer OFF, Low-power dissipation mode set (CM5 = "0", CM6 = "1")	
	Wait mode		—	2	4	mA		V_{CC} = 5.5 V, f (X_{IN}) = 8 MHz	
			—	25	100	µA		V_{CC} = 5.5 V, f (X_{IN}) = 0, f (X_{CIN}) = 32 kHz, Low-power dissipation mode set (CM5 = "0", CM6 = "1")	
			—	1	10			V_{CC} = 5.5 V, f (X_{IN}) = 0, f (X_{CIN}) = 0	
HIGH output voltage	P10–P16, P20–P27, P30, P31, P52, P53	V_{OH}	2.4	—	—	V	2	V_{CC} = 4.5 V I_{OH} = –0.5 mA	
LOW output voltage	P00–P07, P10, P15, P16, P20–P27, P30, P31, P52, P53	V_{OL}	—	—	0.4	V		V_{CC} = 4.5 V I_{OL} = 0.5 mA	
LOW output voltage	P11–P14		—	—	0.4			V_{CC} = 4.5 V	I_{OL} = 3 mA
			—	—	0.6				I_{OL} = 6 mA
Hysteresis [Note1] $\overline{RESET}$, P50–P51, INT1, INT2, INT3, TIM2, TIM3, S_{IN}, S_{CLK}, SCL1, SCL2, SDA1, SDA2		$V_{T+} – V_{T-}$	—	0.5	1.3	V	3	V_{CC} = 5.0 V	
HIGH input leak current P00–P07, P10–P16, P20–P27, P50, P51, $\overline{RESET}$		I_{IZH}	—	—	5	µA	4	V_{CC} = 5.5 V V_I = 5.5 V	
LOW input leak current P00–P07, P10–P16, P20–P27, P50, P51, $\overline{RESET}$		I_{IZL}	—	—	5	µA	4	V_{CC} = 5.5 V V_I = 0 V	
I^2C-BUS • BUS switch connection resistor (between SCL1 and SCL2, SDA1 and SDA2)		R_{BS}	—	—	130	Ω	5	V_{CC} = 4.5 V	

Notes: 1. P06, P07, P15, P23, P24 have the hysteresis when these pins are used as interrupt input pins or timer input pins. P11–P14 have the hysteresis when these pins are used as multi-master I^2C-BUS interface ports. P20–P22 have the hysteresis when these pins are used as serial I/O pins.

2. Connect 0.1 µF or more capacitor externally between the power source pins V_{CC}–Vss so as to reduce power source noise.
   Also connect 0.1 µF or more capacitor externally between the pins V_{CC}–CNVss.
3. Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit. When using the data slicer, use 8 MHz.
4. Pin names in each parameter is described as bellow.
   (1) Dedicated pin: dedicated pin names.
   (2) Double-/triple-function ports
   - When the same limits: I/O port name.
   - When the limits of functions except ports are different from I/O port limits: function pin name.

I²C Bus Table

Slave Address = BAH (Write), BBH (Read)

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	1	1	1	0	1	1/0

Write Table (Input Bytes)

Sub Address		Data								Initial
HEX	BIN	D7	D6	D5	D4	D3	D2	D1	D0	
00H	00000000	(not asigned)					Power Down Mode		H Stop	02H
		0	0	0	0	0	0	1	0	
01H	00000001	X-ray enable	YUV input	Y/C input	EXT input	TV input	Y/C through	(for evaluation)		08H
		0	0	0	0	1	0	0	0	
02H	00000010	Ped clamp	(not asigned)		VRT voltage		Sync-tip clamp			08H
		0	0	0	0	1	0	0	0	
04H	00000100	Sharpness delay (front)		Sharpness gain (front)						A0H
		V1	V0	V1	V0	V0	V0	V0	V0	
05H	00000101	Sharpness delay (rear)		Sharpness gain (rear)						A0H
		V1	V0	V1	V0	V0	V0	V0	V0	
06H	00000110	(not asigned)	Y DL time adj.		YNR SW	YNR limiter level				00H
		V0	V0	V0	V0	V0	V0	V0	V0	
07H	00000111	(not asigned)		Sharpness limiter level						15H
		V0	V0	V0	V1	V0	V1	V0	V1	
08H	00001000	(not asigned)	Tint control							29H
		V0	V0	V1	V0	V1	V0	V0	V1	
09H	00001001	(not asigned)	Color control							28H
		V0	V0	V1	V0	V1	V0	V0	V0	
0AH	00001010	(not asigned)	Contrast control							3BH
		V0	V0	V1	V1	V1	V0	V1	V1	
0BH	00001011	Half tone		OSD level (R)						1EH
		V0	V0	V0	V1	V1	V1	V1	V0	
0CH	00001100	RGB matrix ratio		OSD level (G)						5EH
		V1	V0	V0	V1	V1	V1	V1	V0	
0DH	00001101	OSD comp		OSD level (B)						0EH
		V0	V0	V0	V1	V1	V1	V1	V0	
0EH	00001110	Brightness control								80H
		V1	V0	V0	V0	V0	V0	V0	V0	
0FH	00001111	(not asigned)	H free	AFC1 gain	H phase control					08H
		0	0	0	0	1	0	0	0	
10H	00010000	(not asigned)		(for evaluation)	2D Y/C	(for evaluation)				00H
		0	0	0	0	0	0	0	0	
11H	00010001	(not asigned)	Black Stre. SW	(for evaluation)						40H
		V0	V1	V0	V0	V0	V0	V0	V0	
12H	00010010	RGB mute	(inhibited)			Gamma control				80H
		1	0	0	0	0	0	0	0	
13H	00010011	Service SW	V-shift			(inhibited)	Hold down level			10H
		0	0	0	1	0	0	0	0	
14H	00010100	V-Blanking Stop	V-ramp size							40H
		0	1	0	0	0	0	0	0	
15H	00010101	V-Ramp Invert	V-ramp linearity							FFH
		1	1	1	1	1	1	1	1	
16H	00010110	Cut off (R)								00H
		V0	V0	V0	V0	V0	V0	V0	V0	
17H	00010111	Cut off (R) MSB	Drive (R)							00H
		V0	V0	V0	V0	V0	V0	V0	V0	
18H	00011000	Cut off (G)								00H
		V0	V0	V0	V0	V0	V0	V0	V0	
19H	00011001	Cut off (G) MSB	Drive (G)							00H
		V0	V0	V0	V0	V0	V0	V0	V0	
1AH	00011010	Cut off (B)								00H
		V0	V0	V0	V0	V0	V0	V0	V0	
1BH	00011011	Cut off (B) MSB	Drive (B)							00H
		V0	V0	V0	V0	V0	V0	V0	V0	
1CH	00011100	(not asigned)				Intelligent monitor (analog)				00H
		0	0	0	0	0	0	0	0	
1DH	00011101	(not asigned)		I/M (D) enable	Intelligent monitor (digital)					00H
		0	0	0	0	0	0	0	0	
51H	01010001	H VCO adjust								00H
		0	0	0	0	0	0	0	0	

Note: V0 / V1 ⇒ V Latch bit

Read Table (Output Bytes)

Sub Address		D7	D6	D5	D4	D3	D2	D1	D0
60H	01100000	KILLER	H COINCI	V COINCI	B_W	IIC_STILL	MV_180	DET NZ	K_MONI
61H	01100001	B2 ROM							
62H	01100010	B2 ROM MSB	(not asigned)					C Gain	
63H	01100011	BLKDETV				(not asigned)			

Bus Function

Write

Function	Bit	Sub Add	Data	Description	Initial	Note
H STOP	1	00H	D0	Horizontal output switch (0: H OUT, 1: H STOP)	0	
Power Down	2	00H	D1-D2	Power down mode control (0: normal, 1: PD0, 2: PD1, 3: PD2)	01	
Input Video SW	4	01H	D3-D6	Video SW Selector (1: TV, 2: EXT, 4: Y/C input, 9: YUV input)	0001	
X-ray Enable	1	01H	D7	X-ray protect function switch (0: X-ray Protect OFF, 1: X-ray Protect ON)	0	
Y/C through	1	01H	D2	Y/C separation input switch (0: Y/C Sep ON, 1: Y/C Sep. through)	0	
Sync-tip Clamp	3	02H	D0-D2	Sync-tip clamp switch (0: Clamp ON, 1: TV clamp OFF, 2: EXT clamp OFF, 4: Y clamp OFF)	000	
Ped Clamp	1	02H	D7	Pedestal clamp switch (0: Pedestal clamp OFF, 1: Pedestal clamp ON)	0	
VRT Voltage	2	02H	D3-D4	Reference voltage adjustment for A/D	01	
Sharpness Gain (Front)	6	04H	D0-D5	Over-shoot gain control by 6 bit	100000	V Latch
Sharpness Delay (Front)	2	04H	D6-D7	Over-shoot width control (0: 0 ns, 1: 70 ns, 2: 140 ns, 3: 210 ns)	10	V Latch
Sharpness Gain (Rear)	6	05H	D0-D5	Pre-shoot gain control by 6 bit	100000	V Latch
Sharpness Delay (Rear)	2	05H	D6-D7	Pre-shoot width control (0: 0 ns, 1: 70 ns, 2: 140 ns, 3: 210 ns)	10	V Latch
YNR SW	7	06H	D4	YNR control switch (0: YNR OFF, 1: YNR ON)	0	V Latch
YNR Limiter Level	1	06H	D0-D3	YNR limiter level control	0000	V Latch
Y DL Time Adj.	2	06H	D5-D6	Delay time adjustment of luminance signal (0: 0 ns, 1: 70 ns, 2: 140 ns, 3: 210 ns)	00	V Latch
Sharpness Limiter Level	6	07H	D0-D5	Maximum level control of sharpness	010101	V Latch
Tint Control	7	08H	D0-D6	Tint Control by 7 bit	0101001	V Latch
Color Control	7	09H	D0-D6	Color Saturation control by 7 bit	0101000	V Latch
Contrast Control	7	0AH	D0-D6	Contrast control by 7 bit	0111011	V Latch
OSD Level (R)	6	0BH	D0-D5	Digital OSD (R) level adjustment by 6 bit	011110	V Latch
Half Tone	2	0BH	D6-D7	Setting of Half Tone mode	00	V Latch
OSD Level (G)	6	0CH	D0-D5	Digital OSD (G) level adjustment by 6 bit	011110	V Latch
RGB Matrix Ratio	2	0CH	D6-D7	RGB Matrix ratio control	10	V Latch
OSD Level (B)	6	0DH	D0-D5	Digital OSD (B) level adjustment by 6 bit	011110	V Latch
OSD Comp	2	0DH	D6-D7	Digital OSD threshold voltage control of input signal	00	V Latch
Brightness Control	8	0EH	D0-D7	Brightness control by 8 bit	10000000	V Latch
AFC2 H Phase	5	0FH	D0-D4	Horizontal phase adjustment by 5 bit	01000	
AFC1 Gain	1	0FH	D5	Horizontal AFC gain switch (0: Low, 1: High)	0	

Write (cont.)

Function	Bit	Sub Add	Data	Description	Initial	Note
H-free	1	0FH	D6	Horizontal forced free-running mode switch (0: OFF, 1: Forced Free-running)	0	
2D Y/C	1	10H	D4	Y/C separation mode switch (0: Y/C Sep ON, 1: Y/C Sep. through)	0	
Black Stretch SW	1	11H	D6	Black Stretch function ON/OFF switch (0: OFF, 1: ON)	0	
Gamma Control	1	12H	D0-D3	RGB gamma threshold control (0:Gamma OFF)	0000	
RGB Mute	1	12H	D7	RGB signal mute ON/OFF switch (0: Mute 1: RGB output)	1	
Hold Down Level	3	13H	D0-D2	Hold Down level adjustment by 3 bit	000	
V Shift	3	13H	D4-D6	V RAMP start timing adjustment 2 Line/Step	001	
Service SW	1	13H	D3	Service mode switch (0: Vertical output ON, 1: Vertical output OFF)	0	
V-Ramp Size	7	14H	D0-D6	V-Ramp amplitude adjustment by 7 bit	1000000	
Test	1	14H	D7	No use for customer (Test mode)	0	
V-Ramp Linearity	7	15H	D0-D6	V-Ramp linearity adjustment by 7 bit	1111111	
V-Ramp Invert	1	15H	D7	V-Ramp polarity switch	1	
Cut Off (R)	9	16H	D0-D7	R OUT pedestal level adjustment by 9 bit	00000000	V Latch
		17H	D7		0	
Drive (R)	7	17H	D0-D6	R OUT amplitude adjustment by 7 bit	0000000	V Latch
Cut Off (G)	9	18H	D0-D7	G OUT pedestal level adjustment by 9 bit	00000000	V Latch
		19H	D7		0	
Drive (G)	7	19H	D0-D6	G OUT amplitude adjustment by 7 bit	0000000	V Latch
Cut Off (B)	9	1AH	D0-D7	B OUT pedestal level adjustment by 9 bit	00000000	V Latch
		1BH	D7		0	
Drive (B)	7	1BH	D0-D6	B OUT amplitude adjustment by 7 bit	0000000	V Latch
Intelligent Monitor (Analog)	4	1CH	D0-D3	Intelligent Monitor (Analog) mode selector	0000	
Intelligent Monitor (Digital)	5	1DH	D0-D4	Intelligent Monitor (Digital) mode selector	00000	
Intelligent Monitor (D) Enable	1	1DH	D5	Intelligent Monitor (Digital) function switch (0: OFF, 1: ON)	0	
H VCO Adj.	8	51H	D0-D7	H VCO free-running frequency adjustment by 8 bit	00000000	

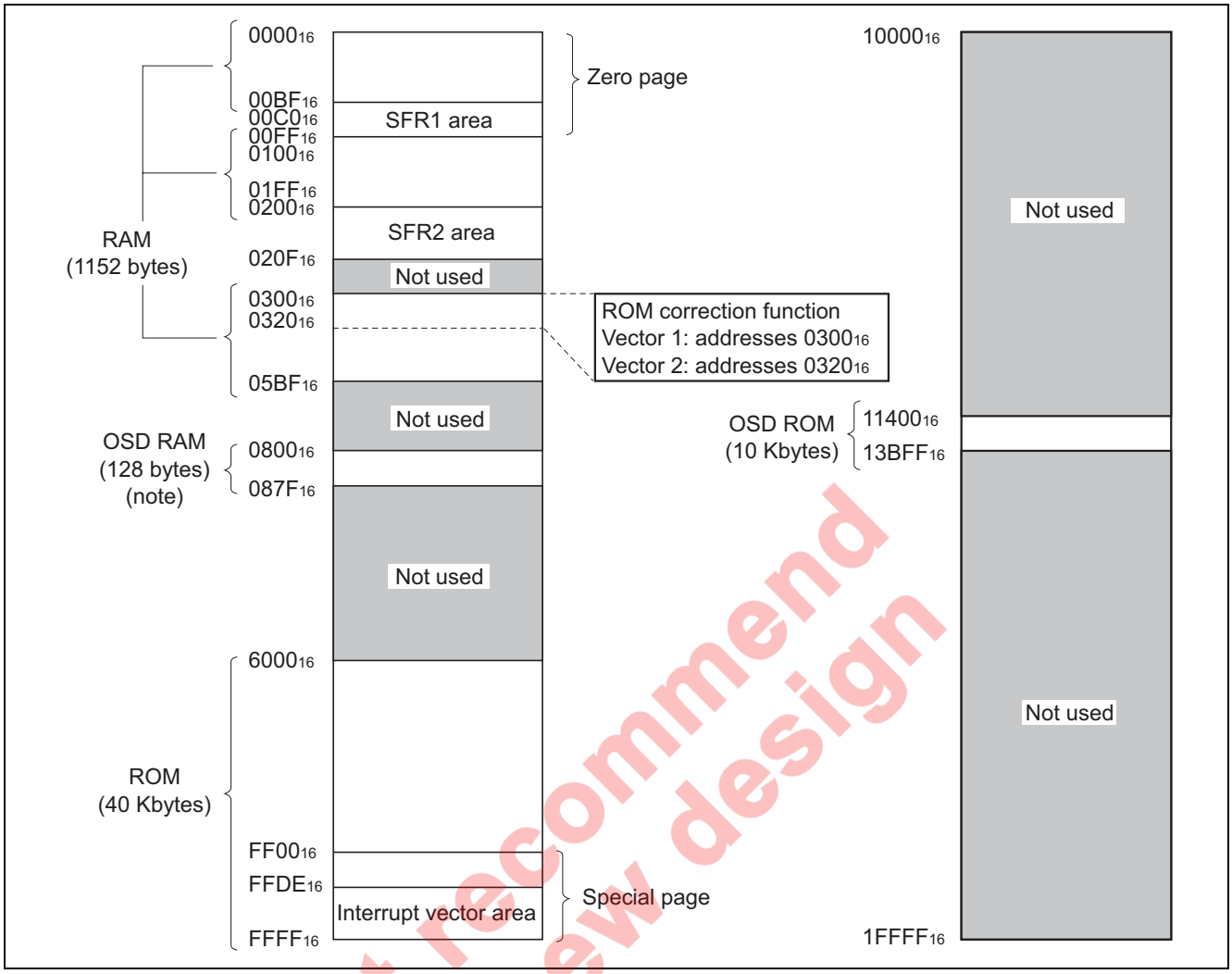
Read

Function	Bit	Sub Add	Data	Description
K_MONI	1	60H	D0	C-processor Killer det. output (1: C-pro Killer ON)
DET_NZ	1	60H	D1	Noise Killer det. output (1: Noise Killer ON)
MV_180	1	60H	D2	Reversed Burst signal (all reversed) det. output (1: Reversed Burst)
IIC_STILL	1	60H	D3	VCR Still mode det. output (1: Still mode)
B_W	1	60H	D4	PLL Killer (Chroma) det. output (1: PLL Killer ON)
V COINCI	1	60H	D5	Vertical Coincidence det. output (1: V Coincident)
H COINCI	1	60H	D6	Horizontal Coincidence det. output (1: H Coincident)
KILLER	1	60H	D7	Color/Killer condition (1: color output, 0: Killer (color off))
B2ROM	9	61H	D0-D7	B2ROM output
		62H	D7	
C Gain	2	62H	D0-D1	ACC amplifier status
BLKDETV	4	63H	D4-D7	Black det. output of Black Stretch circuit

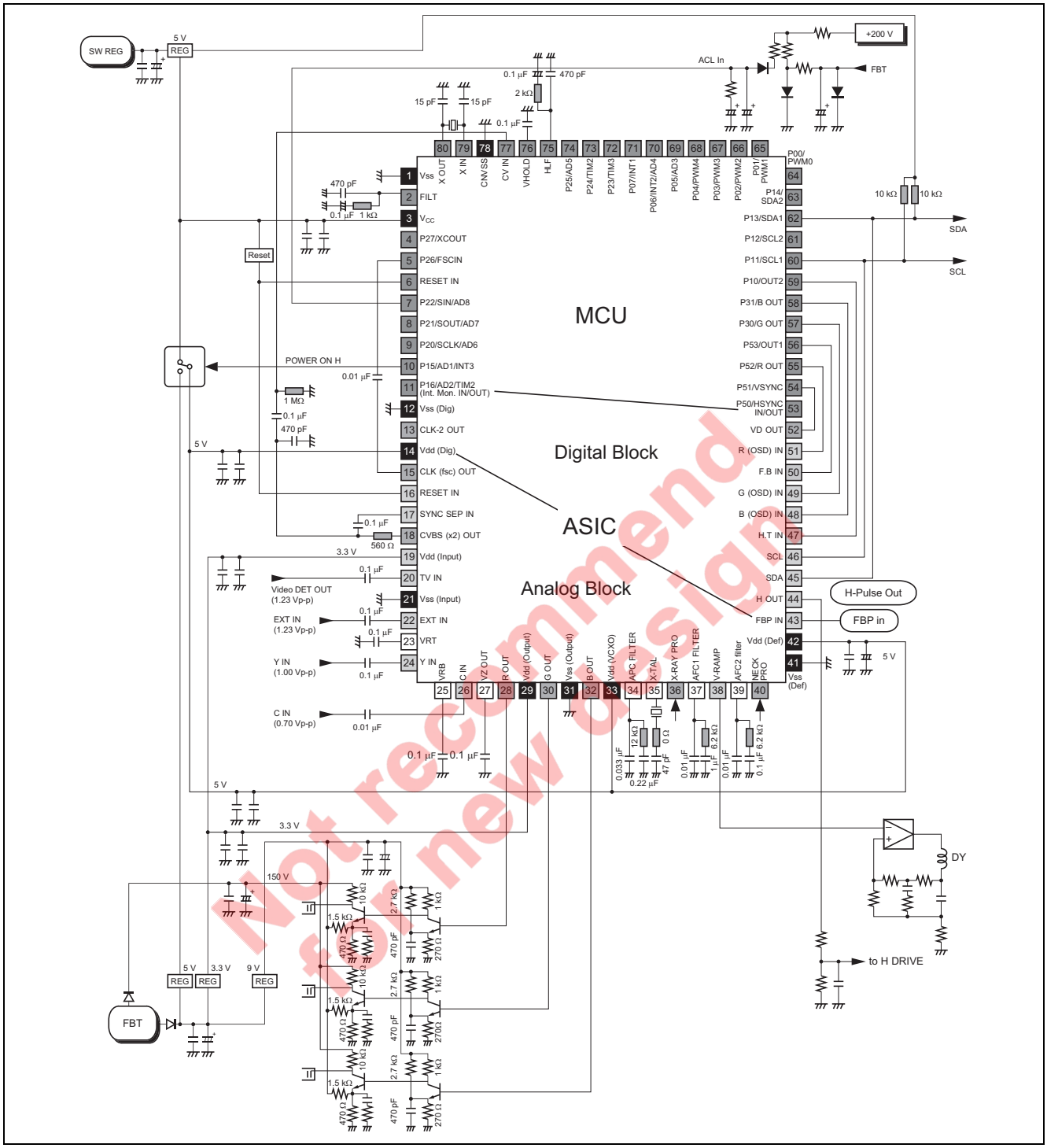
M65580MAP I²C Bus Standard Data

Sub Address	Data	Sub Address	Data	Sub Address	Data
00h	00	30h	20	50h	00
01h	08	31h	05	51h	00
02h	08	32h	04	52h	00
03h	21	33h	81	53h	35
04h	C0	34h	8D	54h	22
05h	C0	35h	63	55h	94
06h	00	36h	79	56h	14
07h	15	37h	50	57h	A6
08h	40	38h	55	58h	00
09h	40	39h	25	59h	A6
0Ah	40	3Ah	21	5Ah	00
0Bh	1E	3Bh	19	5Bh	00
0Ch	9E	3Ch	B3	5Ch	00
0Dh	1E	3Dh	0F	5Dh	80
0Eh	80	3Eh	06		
0Fh	10	3Fh	08		
10h	10	40h	00		
11h	4A	41h	01		
12h	8D	42h	C0		
13h	00	43h	04		
14h	40	44h	64		
15h	40	45h	3D		
16h	00	46h	15		
17h	C0	47h	00		
18h	00	48h	83		
19h	C0	49h	00		
1Ah	00	4Ah	A0		
1Bh	C0	4Bh	00		
1Ch	00	4Ch	15		
1Dh	00	4Dh	01		
		4Eh	6E		
		4Fh	38		

Memory Map

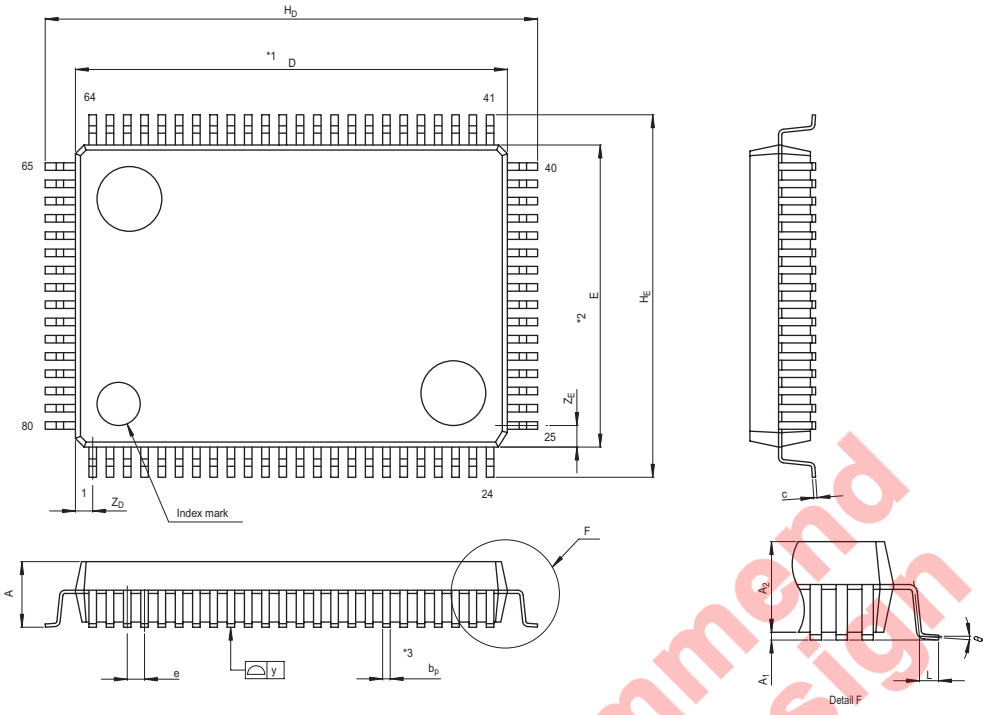


Application Examples



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP80-14x20-0.80	PRQP0080GB-A	80P6N-A	1.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.3	0.35	0.45
c	0.13	0.15	0.2
θ	0°	—	10°
e	0.65	0.8	0.95
y	—	—	0.10
Z_D	—	0.8	—
Z_E	—	1.0	—
L	0.4	0.6	0.8

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