

# HD74LS641

## Octal Bus Transceivers (non-inverted open-collector outputs)

REJ03D0488-0200

Rev.2.00

Feb.18.2005

This octal bus transceivers is designed for asynchronous two-way communication between data buses. The devices transmit data, from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ( $\bar{G}$ ) can be used to disable the device so that the buses are effectively isolated.

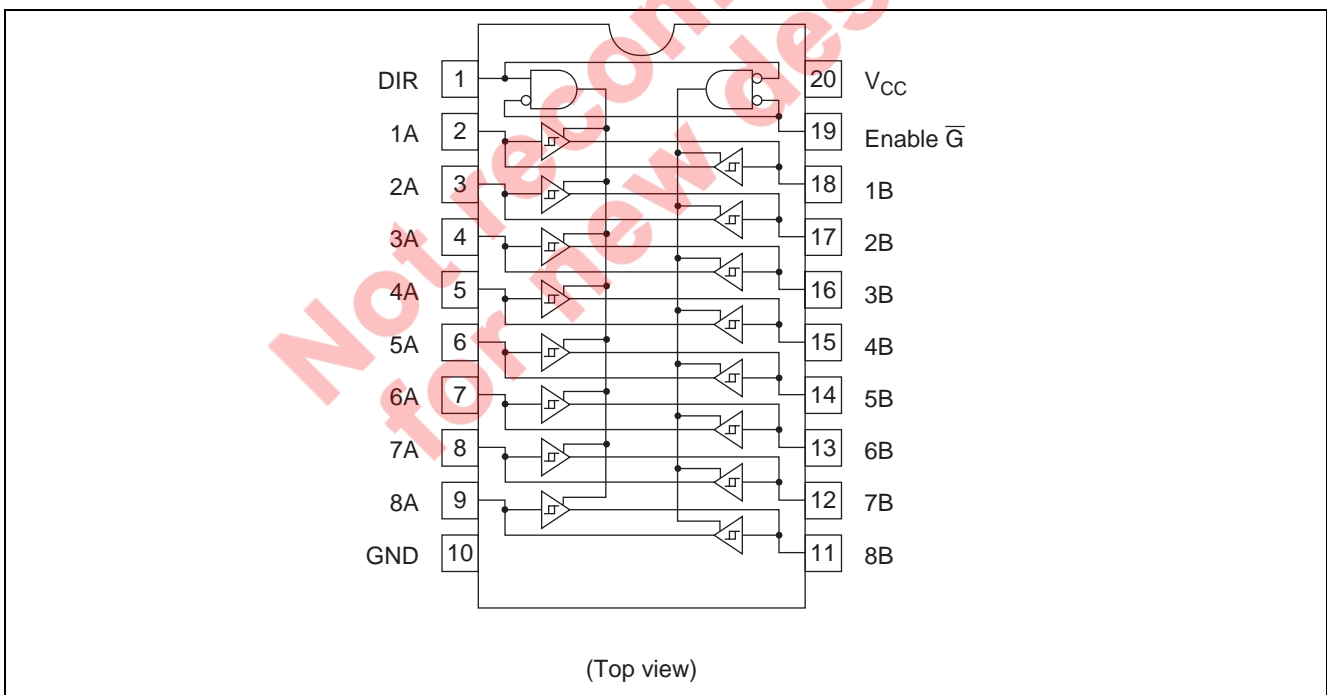
### Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS641P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	P	—
HD74LS641FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

### Pin Arrangement

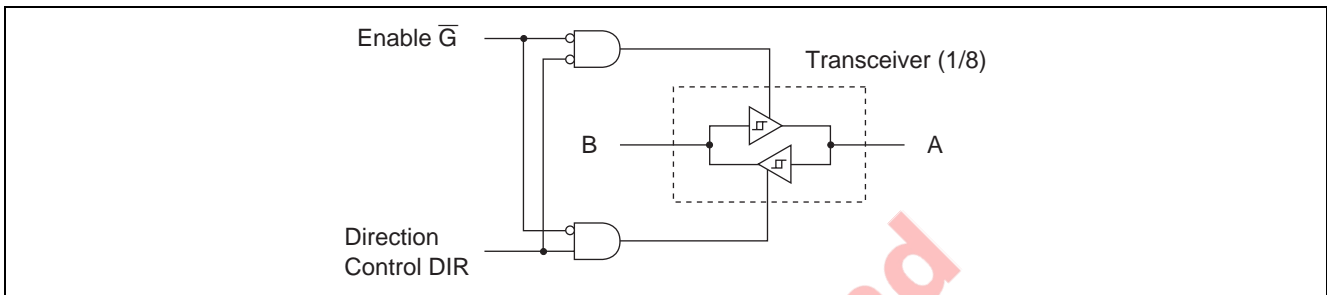


**Function Table**

Enable	Direction Control	Operation
$\bar{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Note: H; high level, L; low level, X; irrelevant

**Block Diagram**



**Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	7	V
Input voltage	$V_{IN}$	7	V
Power dissipation	$P_T$	400	mW
Storage temperature	$T_{stg}$	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

**Recommended Operating Conditions**

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.75	5.00	5.25	V
Output voltage	$V_{OH}$	—	—	5.5	V
Output current	$I_{OL}$	—	—	24	mA
Operating temperature	$T_{opr}$	-20	25	75	°C

**Electrical Characteristics**

(Ta = -20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage	V <sub>IH</sub>	2.0	—	—	V		
	V <sub>IL</sub>	—	—	0.8	V		
Hysteresis	V <sub>T<sup>+</sup></sub> - V <sub>T<sup>-</sup></sub>	0.2	—	—	V	V <sub>CC</sub> = 4.75 V	
Output current	I <sub>OH</sub>	—	—	100	μA	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, V <sub>OH</sub> = 5.5 V	
Output voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 12 mA	
		—	—	0.5	V	I <sub>OL</sub> = 24 mA	
Input current	A or B	I <sub>IH</sub>	—	—	20	μA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 2.7 V
		I <sub>IL</sub>	—	—	-400	μA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0.4 V
	DIR or $\overline{G}$	I <sub>I</sub>	—	—	0.1	mA	V <sub>I</sub> = 5.5 V
			—	—	0.1	mA	V <sub>I</sub> = 7 V
Supply current	I <sub>CCH</sub>	—	48	70	mA	V <sub>CC</sub> = 5.25 V, Output open	
	I <sub>CCL</sub>	—	62	90	mA		
	I <sub>CCZ</sub>	—	64	95	mA		
Input clamp voltage	V <sub>IK</sub>	—	—	-1.5	V	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA	

Note: \* V<sub>CC</sub> = 5 V, Ta = 25°C

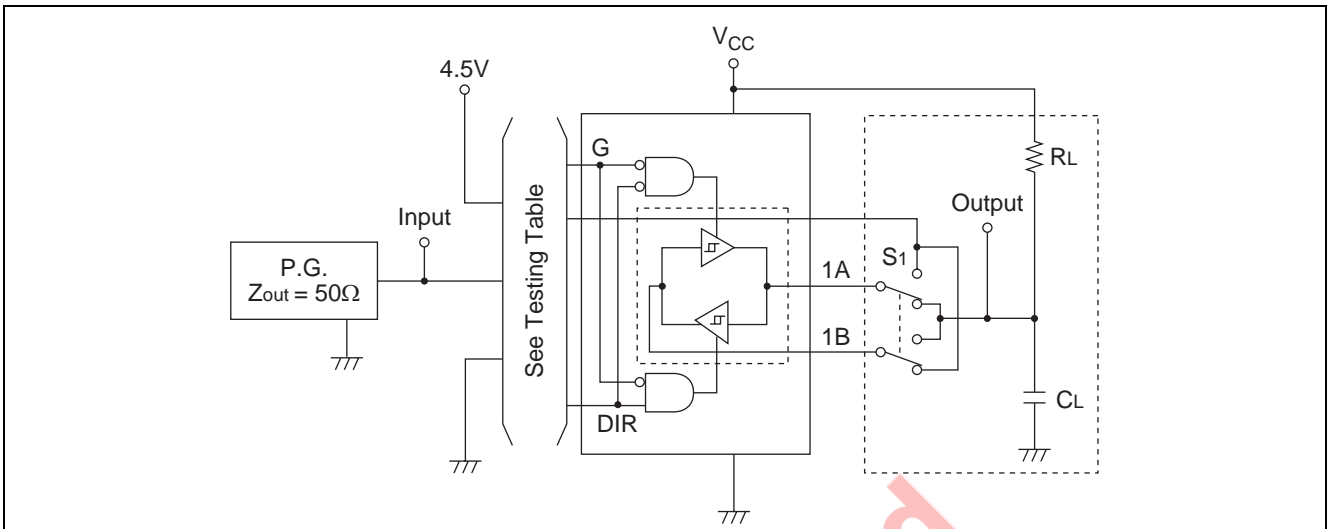
**Switching Characteristics**

(V<sub>CC</sub> = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Propagation delay time	t <sub>PLH</sub>	A	B	—	17	25	ns	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω
		B	A	—	17	25	ns	
	t <sub>PHL</sub>	A	B	—	16	25	ns	
		B	A	—	16	25	ns	
Output enable time	t <sub>PLH</sub>	$\overline{G}$	A	—	23	40	ns	
		$\overline{G}$	B	—	25	40	ns	
	t <sub>PHL</sub>	$\overline{G}$	A	—	34	50	ns	
		$\overline{G}$	B	—	37	50	ns	

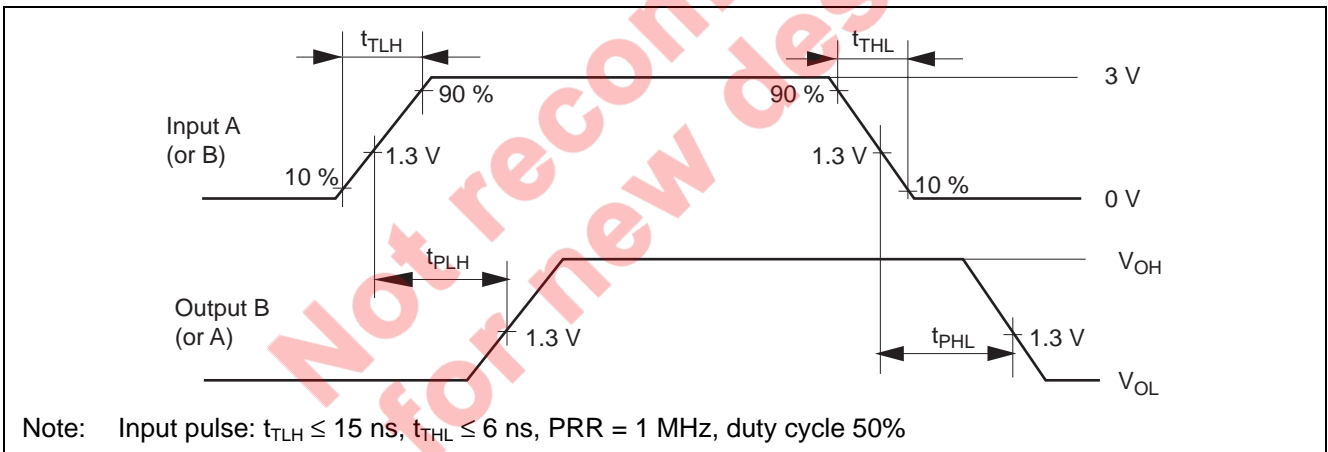
## Testing Method

### Test Circuit

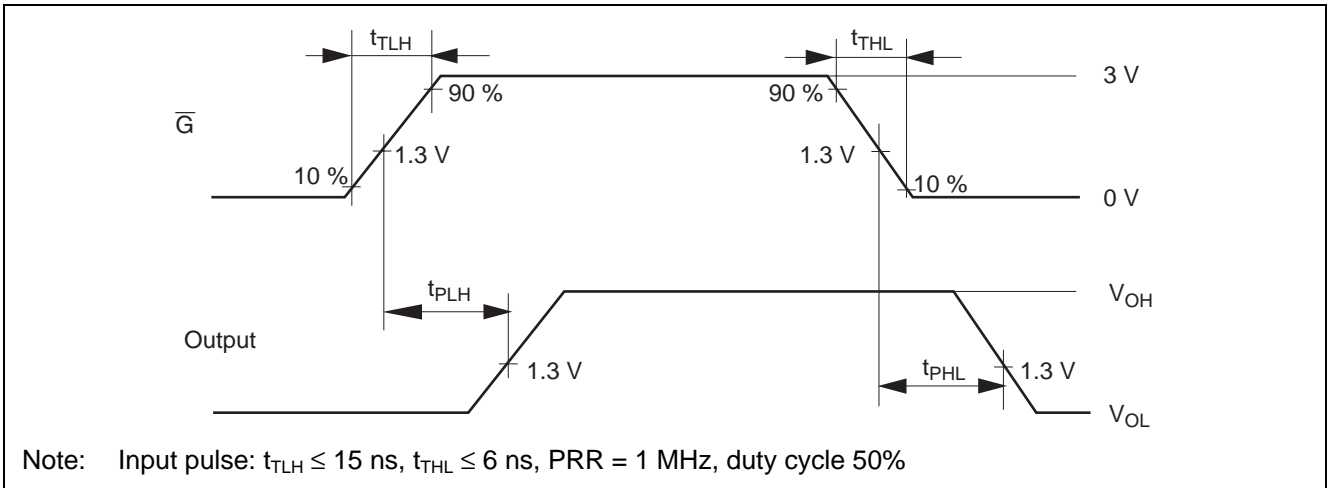


- Notes:
1. 2A-2B, 3A-3B, 4A-4B, 5A-5B, 6A-6B, 7A-7B, 8A-8B, are identical to above load circuit.
  2.  $C_L$  includes probe and jig capacitance.
  3.  $S_1$  is a input-output switch.

### Waveforms 1

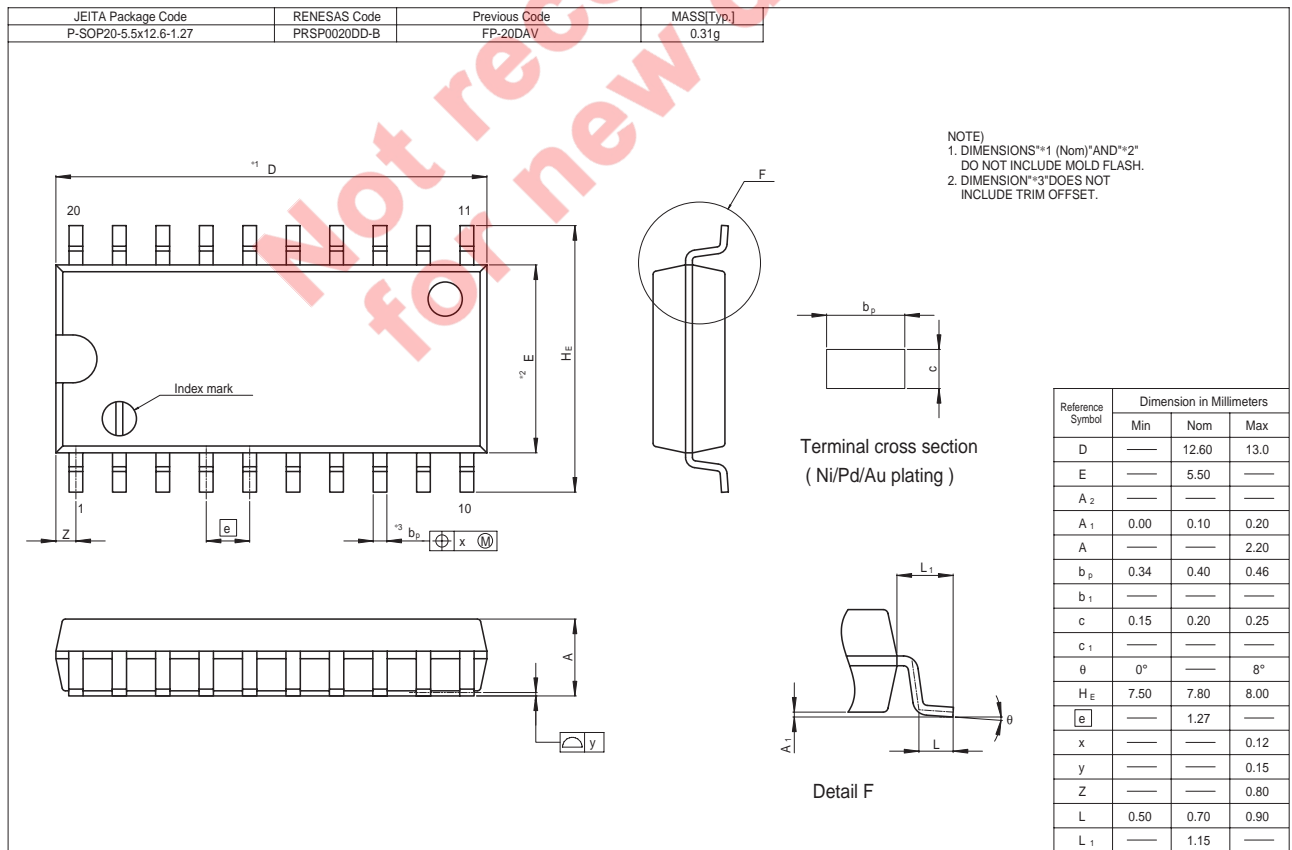
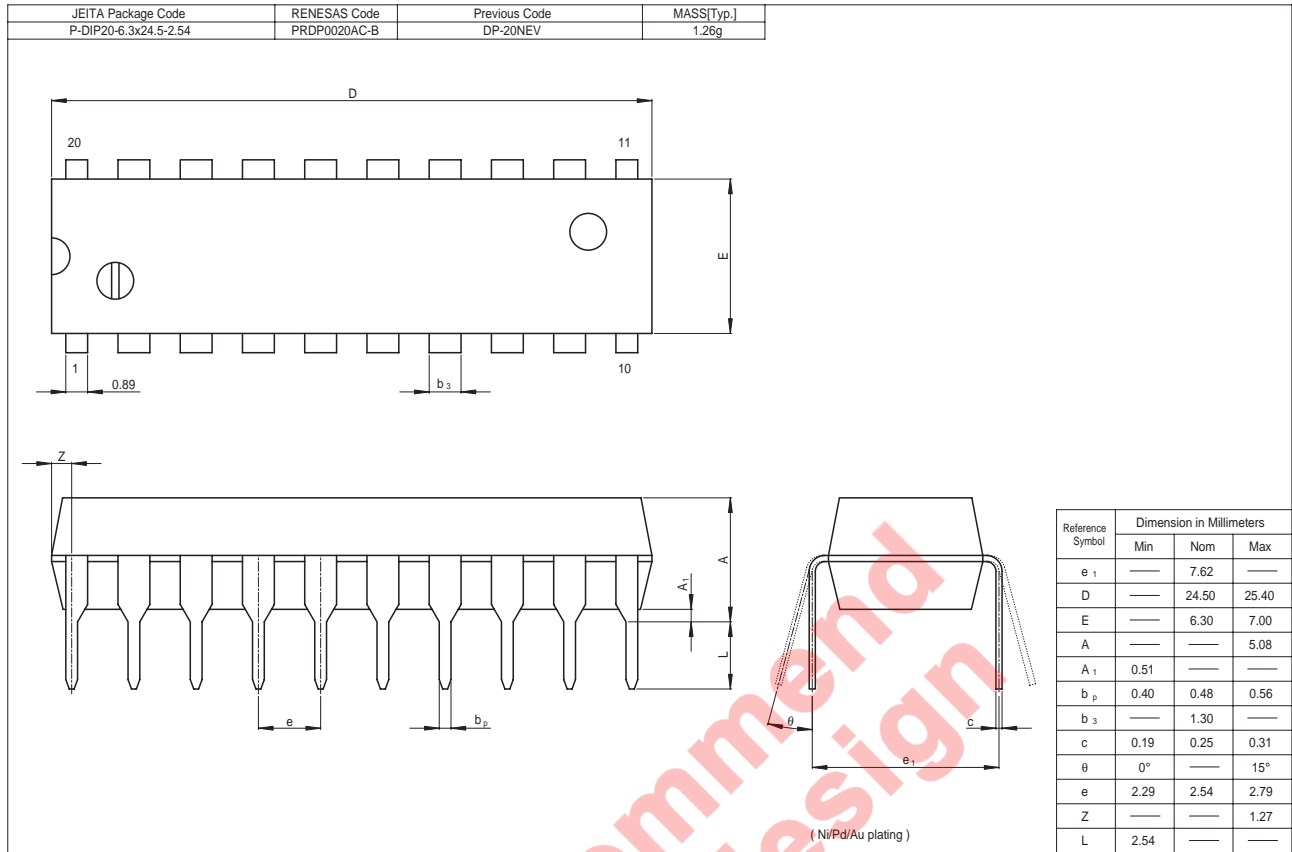


Waveforms 2



Not recommend  
for new design

Package Dimensions



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