



# FAN5355 1A / 0.8A, 3MHz Digitally Programmable TinyBuck™ Regulator

## Features

- 91% Efficiency at 3MHz
- 800mA or 1A Output Current<sup>(1)</sup>
- 2.7V to 5.5V Input Voltage Range
- 6 or 7-bit V<sub>OUT</sub> Programmable from 0.75 to 1.975V
- 3MHz Fixed-Frequency Operation
- Excellent Load and Line Transient Response
- Small Size, 1μH Inductor Solution
- ±2% PWM DC Voltage Accuracy
- 35ns Minimum On-Time
- High-Efficiency, Low-Ripple, Light-Load PFM
- Smooth Transition between PWM and PFM
- 37μA Operating PFM Quiescent Current
- Software Selectable 25kHz Minimum PFM Frequency Prevents Audible Noise in PFM Mode
- I<sup>2</sup>C™-Compatible Interface up to 3.4Mbps
- Pin-Selectable or I<sup>2</sup>C™ Programmable Output Voltage
- On-the-Fly External Clock Synchronization
- 10-lead MLP (3 x 3mm) or 12-bump CSP Packages

## Applications

- SmartReflex™-Compliant Power Supply
- Split Supply DSPs and μP Solutions OMAP™, XSCALE™
- Cell Phones, Smart Phones, PDAs, Digital Cameras, and Portable Media Players
- Micro DC-DC Converter Modules
- Handset Graphic Processors (NVIDIA®, ATI)

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SmartReflex and OMAP are trademarks of Texas Instruments.  
XSCALE is a trademark of Intel Corporation.  
NVIDIA is a registered trademark of NVIDIA Corporation.

## Description

The FAN5355 device is a high-frequency, ultra-fast transient response, synchronous step-down DC-DC converter optimized for low-power applications using small, low-cost inductors and capacitors. The FAN5355 supports up to 800mA or 1A<sup>(1)</sup> load current.

The device is ideal for mobile phones and similar portable applications powered by a single-cell Lithium-Ion battery. With an output voltage range adjustable via I<sup>2</sup>C™ interface from 0.75V to 1.975V, the device supports low-voltage DSPs and processors, core power supplies in smart phones, PDAs, and handheld computers.

The FAN5355 operates at 3MHz (nominal) fixed switching frequency using either its internal oscillator or external SYNC frequency.

During light-load conditions, the regulator includes a PFM mode to enhance light-load efficiency. The regulator transitions smoothly between PWM and PFM modes with no glitches on V<sub>OUT</sub>. Normal PFM (NPFM) mode offers the lowest quiescent current, at the expense of setpoint accuracy. Enhanced PFM (EPFM) mode features higher accuracy, as well as a 25kHz minimum PFM frequency, designed to prevent the regulator from operating in the audible range. In shutdown, the current consumption is reduced to less than 2μA, using software shutdown (EN = 1 with EN\_DCDC = 0), and less than 200nA in hardware shutdown (EN = 0).


The serial interface is compatible with Fast/Standard and High-Speed mode I<sup>2</sup>C specifications, allowing transfers up to 3.4Mbps. This interface is used for dynamic voltage scaling with 12.5mV voltage steps, for reprogramming the mode of operation (PFM or Forced PWM), or to disable/enable the output voltage.

The chip's advanced protection features include short-circuit protection and current and temperature limits. During a sustained over-current event, the IC shuts down and restarts after a delay to reduce average power dissipation into a fault.


During start-up, the IC controls the output slew rate to minimize input current and output overshoot at the end of soft-start. The IC maintains a consistent soft-start ramp, regardless of output load during start-up.

The FAN5355 is available in 10-lead MLP (3x3mm) and 12-bump CSP packages.

## Ordering Information

Order Number <sup>(4)</sup>	Option	Slave Address LSB		V <sub>OUT</sub> Programming			Power-up Defaults		Package <sup>(4)</sup> 
		A1	A0	DAC	MIN.	MAX.	VSEL0	VSEL1	
FAN5355UC00X	00	0	0	6	0.7500	1.5375	1.05	1.35	WLCSP-12, 2.23x1.46mm
FAN5355MP00X	00	0	0	6	0.7500	1.5375	1.05	1.35	MLP-10, 3x3mm
FAN5355UC02X	02	1	0	6	0.7500	1.4375 <sup>(2)</sup>	1.05	1.20	WLCSP-12, 2.23x1.46mm
FAN5355UC03X	03	0	0	6	0.7500	1.5375	1.00	1.20	WLCSP-12, 2.23x1.46mm
FAN5355UC06X	06 <sup>(1)</sup>	0	0	6	1.1875	1.9750	1.80	1.80	WLCSP-12, 2.23x1.46mm
FAN5355UC07X	07 <sup>(1)</sup>	1	1	7	0.7500 <sup>(3)</sup>	1.9750	1.05	1.35	WLCSP-12, 2.23x1.46mm
FAN5355MP07X	07 <sup>(1)</sup>	1	1	7	0.7500 <sup>(3)</sup>	1.9750	1.05	1.35	MLP-10, 3x3mm

### Notes:

- Option 06 and 07 is rated for 1A output current. All other options are rated for 800mA output current.
- V<sub>OUT</sub> is limited to the maximum voltage for all VSEL codes greater than the maximum V<sub>OUT</sub> listed.
- V<sub>OUT</sub> may be programmed down 100mV for option 07. Performance below 0.75V is not guaranteed.
-  All packages are “green” per JEDEC: J-STD-020B standard. The “X” designator specifies tape and reel packaging.

## Typical Application

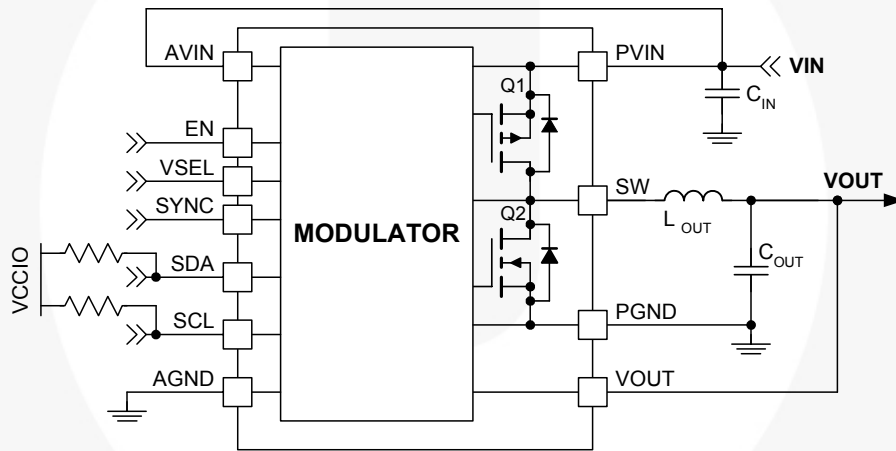


Figure 1. Typical Application

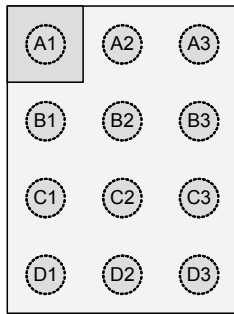
Component	Description	Vendor	Parameter	Min.	Typ.	Max.	Units
L1 (L <sub>OUT</sub> )	1μH nominal	Murata LQM31P or FDK MIPS2520	L <sup>(5)</sup>	0.7	1.0	1.2	μH
			DCR (series R)		100		mΩ
C <sub>OUT</sub>	0603 (1.6x0.8x0.8) 10μF X5R or better	Murata or equivalent GRM188R60G106ME47D	C <sup>(6)</sup>	5.6	10.0	12.0	μF
C <sub>IN</sub>	0603 (1.6x0.8x0.8) 4.7μF X5R or better	Murata or equivalent GRM188R60J475KE19D	C <sup>(6)</sup>	3.0	4.7	5.6	μF

Table 1. Recommended External Components

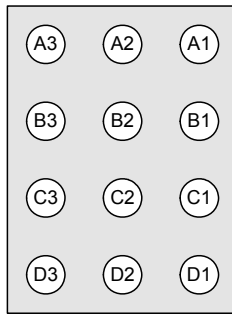
### Notes:

- Minimum L incorporates both tolerance, temperature, and partial saturation effects (L decreases with increasing current).
- Minimum C is a function of initial tolerance, maximum temperature, and the effective capacitance being reduced due to frequency, dielectric, and voltage bias effects.

## Pin Configuration

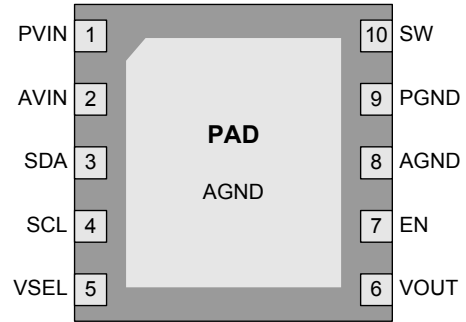


Top View



Bottom View

Figure 2. WLCSP- 12, 2.23x1.46mm



Top View

Figure 3. MLP10, 3x3mm

## Pin Definitions

Pin #		Name	Description
WLCSP	MLP		
A1, B1	9	PGND	<b>Power GND.</b> Power return for gate drive and power transistors. Connect to AGND on PCB. The connection from this pin to the bottom of $C_{IN}$ should be as short as possible.
A2	10	SW	<b>Switching Node.</b> Connect to output inductor.
A3	1	PVIN	<b>Power Input Voltage.</b> Connect to input power source. The connection from this pin to $C_{IN}$ should be as short as possible.
B2	N/A	SYNC	<b>Sync.</b> When toggling and SYNC_EN bit is HIGH, the regulator synchronizes to the frequency on this pin. In PWM mode, when this pin is statically LOW or statically HIGH, or when its frequency is outside of the specified capture range, the regulator's frequency is controlled by its internal 3MHz clock.
B3	2	AVIN	<b>Analog Input Voltage.</b> Connect to input power source as close as possible to the input bypass capacitor.
C1	8, PAD	AGND	<b>Analog GND.</b> This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin.
C2	7	EN	<b>Enable.</b> When this pin is HIGH, the circuit is enabled. When LOW, quiescent current is minimized. This pin should not be left floating.
C3	3	SDA	<b>SDA.</b> I <sup>2</sup> C interface serial data.
D1	6	VOUT	<b>Output Voltage Monitor.</b> Tie this pin to the output voltage. This is a signal input pin to the control circuit and does not carry DC current.
D2	5	VSEL	<b>Voltage Select.</b> When HIGH, $V_{OUT}$ is set by VSEL1. When LOW, $V_{OUT}$ is set by VSEL0. This behavior can be overridden through I <sup>2</sup> C register settings. This pin should not be left floating.
D3	4	SCL	<b>SCL.</b> I <sup>2</sup> C interface serial clock.

### Note:

- All logic inputs (SDA, SCL, SYNC, EN, and VSEL) are high impedance and should not be left floating. For minimum quiescent power consumption, tie unused logic inputs to AVIN or AGND. If I<sup>2</sup>C control is unused, tie SDA and SCL to AVIN.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Units	
V <sub>CC</sub>	AVIN, SW, PVIN Pins	-0.3	6.5	V	
	Other Pins	-0.3	AVIN + 0.3 <sup>(8)</sup>	V	
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114		3.5	KV
		Charged Device Model per JESD22-C101		1.5	KV
T <sub>J</sub>	Junction Temperature	-40	+150	°C	
T <sub>STG</sub>	Storage Temperature	-65	+150	°C	
T <sub>L</sub>	Lead Soldering Temperature, 10 Seconds		+260	°C	

### Note:

8. Lesser of 6.5V or V<sub>CC</sub>+0.3V.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V <sub>IN</sub>	Supply Voltage	2.7	5.5	V
f	Frequency Range	2.7	3.3	MHz
V <sub>SW</sub>	SDA and SCL Voltage Swing <sup>(9)</sup>		2.5	V
T <sub>A</sub>	Ambient Temperature	-40	+85	°C
T <sub>J</sub>	Junction Temperature	-40	+125	°C

### Note:

9. The I<sup>2</sup>C interface operates with t<sub>HD, DAT</sub> = 0 as long as the pull-up voltage for SDA and SCL is less than 2.5V. If voltage swings greater than 2.5V are required (for example if the I<sup>2</sup>C bus is pulled up to V<sub>IN</sub>), the minimum t<sub>HD, DAT</sub> must be increased to 80ns. Most I<sup>2</sup>C masters change SDA near the midpoint between the falling and rising edges of SCL, which provides ample t<sub>HD, DAT</sub>.

## Dissipation Ratings<sup>(10)</sup>

Package	R $\theta_{JA}$ <sup>(11)</sup>	Power Rating at T <sub>A</sub> ≤ 25°C	Derating Factor > T <sub>A</sub> = 25°C
Molded Leadless Package (MLP)	49°C/W	2050mW	21mW/°C
Wafer-Level Chip-Scale Package (WLCSP)	110°C/W	900mW	9mW/°C

### Notes:

10. Maximum power dissipation is a function of T<sub>J(max)</sub>,  $\theta_{JA}$ , and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = [T<sub>J(max)</sub> - T<sub>A</sub>] /  $\theta_{JA}$ .
11. This thermal data is measured with high-K board (four-layer board according to JESD51-7 JEDEC standard).

## Electrical Specifications

$V_{IN} = 3.6V$ ,  $EN = V_{IN}$ ,  $VSEL = V_{IN}$ ,  $SYNC = GND$ ,  $VSEL0(6)$  bit = 1,  $CONTROL2[4:3] = 00$ .  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = 25^{\circ}C$ . Circuit and components according to Figure 1.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>Power Supplies</b>						
$V_{IN}$	Input Voltage Range		2.7		5.5	V
$I_Q$	Quiescent Current	$I_O = 0mA$ , EPFM Mode, $F_{PFM} = 25kHz$		110	150	$\mu A$
		$I_O = 0mA$ , NPFM Mode		37	50	$\mu A$
		$I_O = 0mA$ , 3MHz PWM Mode		4.8		mA
$I_{SD}$	Shutdown Supply Current	$EN = GND$		0.1	2.0	$\mu A$
		$EN = V_{IN}$ , $EN\_DCDC$ bit = 0, $SDA = SCL = V_{IN}$		0.1	2.0	
$V_{UVLO}$	Under-Voltage Lockout Threshold	$V_{IN}$ Rising		2.40	2.60	V
		$V_{IN}$ Falling	2.00	2.15	2.30	V
$V_{UVHYS}$	Under-Voltage Lockout Hysteresis		200	250	300	mV
<b>ENABLE, VSEL, SDA, SCL, SYNC</b>						
$V_{IH}$	HIGH-Level Input Voltage		1.2			V
$V_{IL}$	LOW-Level Input Voltage				0.4	V
$I_{IN}$	Input Bias Current	Input tied to GND or $V_{IN}$		0.01	1.00	$\mu A$
<b>Power Switch and Protection</b>						
$R_{DS(ON)P}$	P-channel MOSFET On Resistance	$V_{IN} = 3.6V$ , CSP Package		145		m $\Omega$
		$V_{IN} = 3.6V$ , MLP Package		165		
		$V_{IN} = 2.7V$ , MLP Package		200		
$I_{LKGP}$	P-channel Leakage Current	$V_{DS} = 6V$			1	$\mu A$
$R_{DS(ON)N}$	N-channel MOSFET On Resistance	$V_{IN} = 3.6V$ , CSP Package		75		m $\Omega$
		$V_{IN} = 3.6V$ , MLP Package		95		
		$V_{IN} = 2.7V$ , MLP Package		101		
$I_{LKGN}$	N-channel Leakage Current	$V_{DS} = 6V$			1	$\mu A$
$R_{DIS}$	Discharge Resistor for Power-down Sequence	Options 03, 06, 07		15	50	$\Omega$
$I_{LIMPK}$	P-MOS Current Limit	$2.7V \leq V_{IN} \leq 4.2V$ , All Options Except 06 and 07	1150	1350	1600	mA
		$2.7V \leq V_{IN} \leq 5.5V$ , All Options Except 06 and 07	1050	1350	1600	
		$2.7V \leq V_{IN} \leq 4.2V$ , 06 and 07 Option	1300	1550	1800	
$T_{LIMIT}$	Thermal Shutdown			150		$^{\circ}C$
$T_{HYST}$	Thermal Shutdown Hysteresis			20		$^{\circ}C$
<b>Frequency Control</b>						
$f_{SW}$	Oscillator Frequency		2.65	3.00	3.35	MHz
$f_{SYNC}$	Synchronization Range		2.7	3.0	3.3	MHz
$D_{SYNC}$	Synchronization Duty Cycle		20		80	%
$f_{SYNCRVAL}$	SYNC Frequency Rejection		1.6		4.3	MHz
$f_{PFM(MIN)}$	Minimum PFM Frequency	EPFM Mode, $I_{LOAD} = 0$		25		kHz

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### Electrical Specifications (Continued)

$V_{IN} = 3.6V$ ,  $EN = V_{IN}$ ,  $VSEL = V_{IN}$ ,  $SYNC = GND$ ,  $VSEL0(6)$  bit = 1,  $CONTROL2[4:3] = 00$ .  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = 25^{\circ}C$ . Circuit and components according to Figure 1

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
<b>Output Regulation</b>							
$V_{OUT}$	$V_{OUT}$ Accuracy	Option 00	$I_{OUT(DC)} = 0$ , Forced PWM, $V_{OUT} = 1.35V$	-1.5		1.5	%
			$2.7V \leq V_{IN} \leq 5.5V$ , $V_{OUT}$ from 0.75 to 1.5375, $I_{OUT(DC)} = 0$ to 800mA, Forced PWM	-2		2	%
			$2.7V \leq V_{IN} \leq 5.5V$ , $V_{OUT}$ from 0.75 to 1.5375, $I_{OUT(DC)} = 0$ to 800mA, NPFM Mode	-1.5		3.5	%
		Option 02	$I_{OUT(DC)} = 0$ , Forced PWM, $V_{OUT} = 1.20V$	-1.5		1.5	%
			$2.7V \leq V_{IN} \leq 5.5V$ , $V_{OUT}$ from 0.75 to 1.4375, $I_{OUT(DC)} = 0$ to 800mA, Forced PWM	-2		2	%
			$2.7V \leq V_{IN} \leq 5.5V$ , $V_{OUT}$ from 0.75 to 1.4375, $I_{OUT(DC)} = 0$ to 800mA, NPFM Mode	-1.5		3.5	%
		Option 03	$I_{OUT(DC)} = 0$ , Forced PWM, $V_{OUT} = 1.20V$	-1.5		1.5	%
			$2.7V \leq V_{IN} \leq 5.5V$ , $V_{OUT}$ from 0.75 to 1.5375, $I_{OUT(DC)} = 0$ to 800mA, Forced PWM	-2		2	%
			$2.7V \leq V_{IN} \leq 5.5V$ , $V_{OUT}$ from 0.75 to 1.5375, $I_{OUT(DC)} = 0$ to 800mA, NPFM Mode	-1.5		3.5	%
			$2.7V \leq V_{IN} \leq 5.5V$ , $V_{OUT}$ from 0.75 to 1.5375, $I_{OUT(DC)} = 0$ to 800mA, EPFM Mode	-0.5		2	%
		Option 06	$I_{OUT(DC)} = 0$ , Forced PWM, $V_{OUT} = 1.800V$	-1.5		1.5	%
			$2.7V \leq V_{IN} \leq 5.5V$ , $V_{OUT}$ from 1.185 to 1.975, $I_{OUT(DC)} = 0$ to 1A, Forced PWM	-2		2	%
			$2.7V \leq V_{IN} \leq 5.5V$ , $V_{OUT}$ from 1.185 to 1.975, $I_{OUT(DC)} = 0$ to 1A, NPFM Mode	-1.5		3.5	%
			$2.7V \leq V_{IN} \leq 5.5V$ , $V_{OUT}$ from 1.185 to 1.975, $I_{OUT(DC)} = 0$ to 1A, EPFM Mode	-0.5		2	%
		Option 07	$I_{OUT(DC)} = 0$ , Forced PWM, $V_{OUT} = 1.35V$	-1.5		1.5	%
			$2.7V \leq V_{IN} \leq 5.5V$ , $V_{OUT}$ from 0.75 to 1.6875, $I_{OUT(DC)} = 0$ to 1A, Forced PWM	-2		2	%
$2.7V \leq V_{IN} \leq 5.5V$ , $V_{OUT}$ from 0.75 to 1.6875, $I_{OUT(DC)} = 0$ to 1A, NPFM Mode	-1.5			3.5	%		
$2.7V \leq V_{IN} \leq 5.5V$ , $V_{OUT}$ from 0.75 to 1.6875, $I_{OUT(DC)} = 0$ to 1A, EPFM Mode	-0.5			2	%		
$\frac{\Delta V_{OUT}}{\Delta I_{LOAD}}$	Load Regulation	$I_{OUT(DC)} = 0$ to 800mA, Forced PWM		-0.5		%/A	
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$2.7V \leq V_{IN} \leq 5.5V$ , $I_{OUT(DC)} = 300mA$		0		%/V	
$V_{RIPPLE}$	Output Ripple Voltage	PWM Mode, $V_{OUT} = 1.35V$		2.2		mVP-P	
		PFM Mode, $I_{OUT(DC)} = 10mA$		20		mVP-P	

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### Electrical Specifications (Continued)

$V_{IN} = 3.6V$ ,  $EN = V_{IN}$ ,  $VSEL = V_{IN}$ ,  $SYNC = GND$ ,  $VSEL0(6)$  bit = 1,  $CONTROL2[4:3] = 00$ .  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = 25^{\circ}C$ . Circuit and components according to Figure 1.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
<b>DAC</b>							
	Resolution	Option 07	7			Bits	
		All Other Options	6			Bits	
	Differential Nonlinearity	Monotonicity Assured by Design			0.8	LSB	
<b>Timing</b>							
$t_{2C_{EN}}$	EN HIGH to $I^2C$ Start		250			$\mu s$	
$t_{V(L-H)}$	$V_{OUT}$ LOW to HIGH Settling	$R_{LOAD} = 75\Omega$ , Transition from 1.0 to 1.5375V $V_{OUT}$ Settled to within 2% of Setpoint		7		$\mu s$	
<b>Soft-Start</b>							
$t_{SS}$	Regulator Enable to Regulated $V_{OUT}$	Option 06	$R_{LOAD} \geq 5\Omega$ , to $V_{OUT} = 1.8000V$		170	210	$\mu s$
		All Other Options	$R_{LOAD} \geq 5\Omega$ , to $V_{OUT} =$ Power-up Default		140	180	$\mu s$
$V_{SLEW}$	Soft-start $V_{OUT}$ Slew Rate <sup>(12)</sup>			18.75		V/ms	

**Note:**

12. Option 06 slew rate is 35.5V/ms during the first 16 $\mu s$  of soft-start.

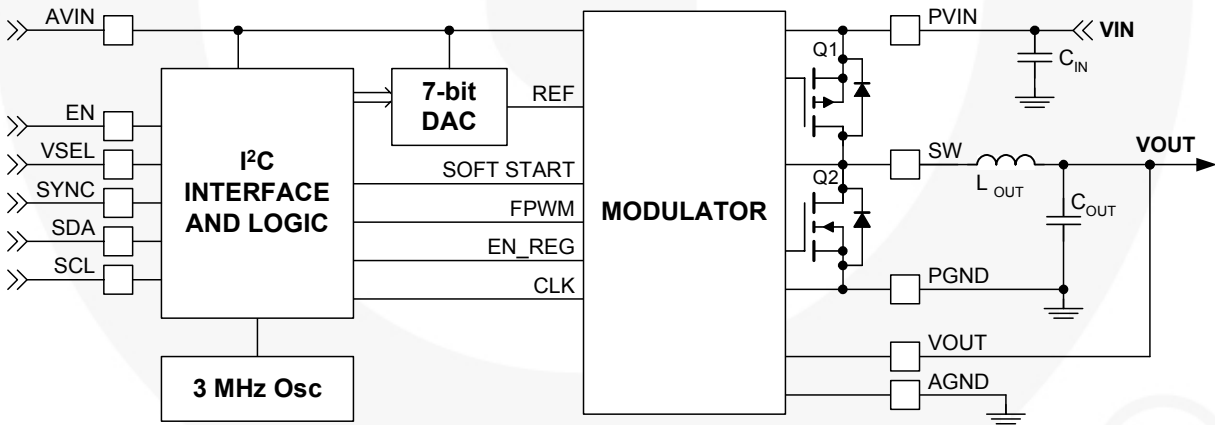


Figure 4. Block Diagram

## I<sup>2</sup>C Timing Specifications

Guaranteed by design.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f <sub>SCL</sub>	SCL Clock Frequency	Standard mode			100	kHz
		Fast mode			400	kHz
		High-Speed mode, C <sub>B</sub> ≤ 100pF			3400	kHz
		High-Speed mode, C <sub>B</sub> ≤ 400pF			1700	kHz
t <sub>BUF</sub>	Bus-free Time between STOP and START Conditions	Standard mode		4.7		μs
		Fast mode		1.3		μs
t <sub>HD,STA</sub>	START or Repeated START Hold Time	Standard mode		4		μs
		Fast mode		600		ns
		High-Speed mode		160		ns
t <sub>LOW</sub>	SCL LOW Period	Standard mode		4.7		μs
		Fast mode		1.3		ns
		High-Speed mode, C <sub>B</sub> ≤ 100pF		160		ns
		High-Speed mode, C <sub>B</sub> ≤ 400pF		320		ns
t <sub>HIGH</sub>	SCL HIGH Period	Standard mode		4		μs
		Fast mode		600		ns
		High-Speed mode, C <sub>B</sub> ≤ 100pF		60		ns
		High-Speed mode, C <sub>B</sub> ≤ 400pF		120		ns
t <sub>SU,STA</sub>	Repeated START Setup Time	Standard mode		4.7		μs
		Fast mode		600		ns
		High-Speed mode		160		ns
t <sub>SU,DAT</sub>	Data Setup Time	Standard mode		250		ns
		Fast mode		100		ns
		High-Speed mode		10		ns
t <sub>HD,DAT</sub>	Data Hold Time <sup>(9)</sup>	Standard mode	0		3.45	μs
		Fast mode	0		900	ns
		High-Speed mode, C <sub>B</sub> ≤ 100pF	0		70	ns
		High-Speed mode, C <sub>B</sub> ≤ 400pF	0		150	ns
t <sub>RCL</sub>	SCL Rise Time	Standard mode	20+0.1C <sub>B</sub>		1000	ns
		Fast mode	20+0.1C <sub>B</sub>		300	ns
		High-Speed mode, C <sub>B</sub> ≤ 100pF		10	80	ns
		High-Speed mode, C <sub>B</sub> ≤ 400pF		20	160	ns
t <sub>FCL</sub>	SCL Fall Time	Standard mode	20+0.1C <sub>B</sub>		300	ns
		Fast mode	20+0.1C <sub>B</sub>		300	ns
		High-Speed mode, C <sub>B</sub> ≤ 100pF		10	40	ns
		High-Speed mode, C <sub>B</sub> ≤ 400pF		20	80	ns
t <sub>RDA</sub> t <sub>RCL1</sub>	SDA Rise Time Rise Time of SCL After a Repeated START Condition and After ACK Bit	Standard mode	20+0.1C <sub>B</sub>		1000	ns
		Fast mode	20+0.1C <sub>B</sub>		300	ns
		High-Speed mode, C <sub>B</sub> ≤ 100pF		10	80	ns
		High-Speed mode, C <sub>B</sub> ≤ 400pF		20	160	ns
t <sub>FDA</sub>	SDA Fall Time	Standard mode	20+0.1C <sub>B</sub>		300	ns
		Fast mode	20+0.1C <sub>B</sub>		300	ns
		High-Speed mode, C <sub>B</sub> ≤ 100pF		10	80	ns
		High-Speed mode, C <sub>B</sub> ≤ 400pF		20	160	ns
t <sub>SU,STO</sub>	Stop Condition Setup Time	Standard mode		4		μs
		Fast mode		600		ns
		High-Speed mode		160		ns
C <sub>B</sub>	Capacitive Load for SDA and SCL				400	pF



## Timing Diagrams

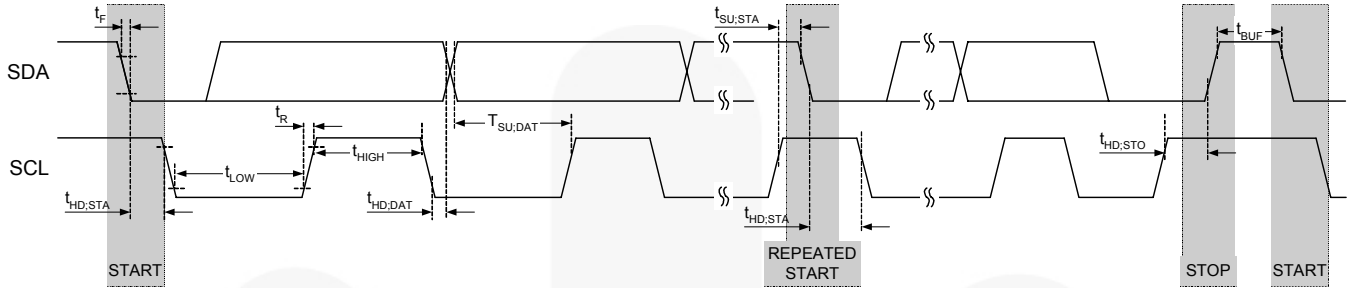
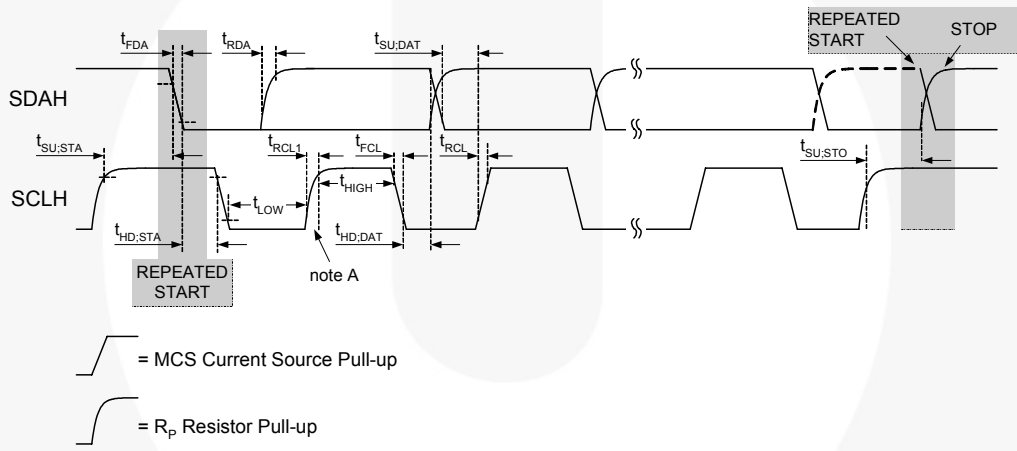


Figure 5. I<sup>2</sup>C Interface Timing for Fast and Slow Modes



Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

Figure 6. I<sup>2</sup>C Interface Timing for High-Speed Mode

## Typical Performance Characteristics

Unless otherwise specified, Auto-PWM/NPFM,  $V_{IN} = 3.6V$ ,  $T_A = 25^\circ C$ , and recommended components as specified in Table 1.

### Efficiency

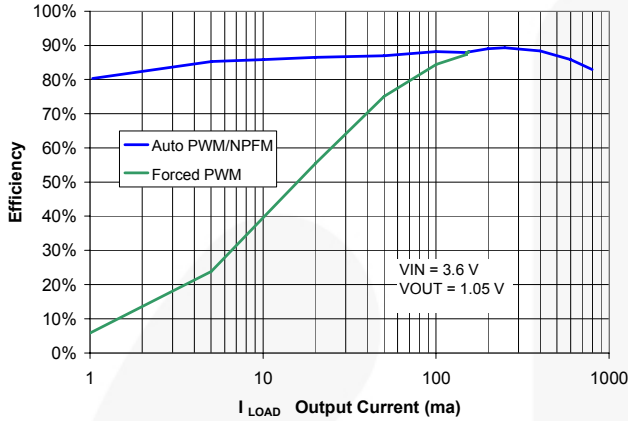


Figure 7. Efficiency vs. Load at  $V_{OUT} = 1.05V$

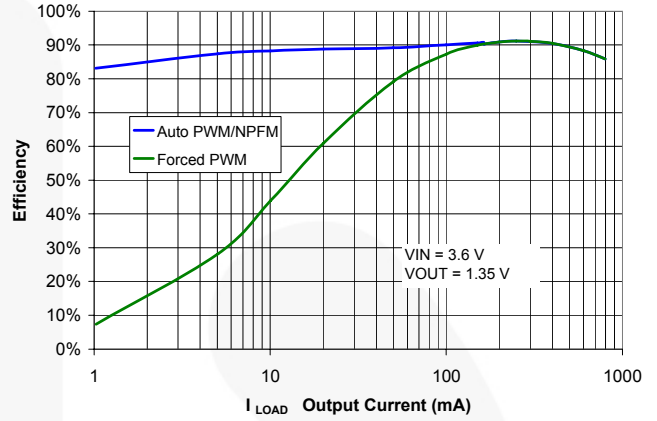


Figure 8. Efficiency vs. Load at  $V_{OUT} = 1.35V$

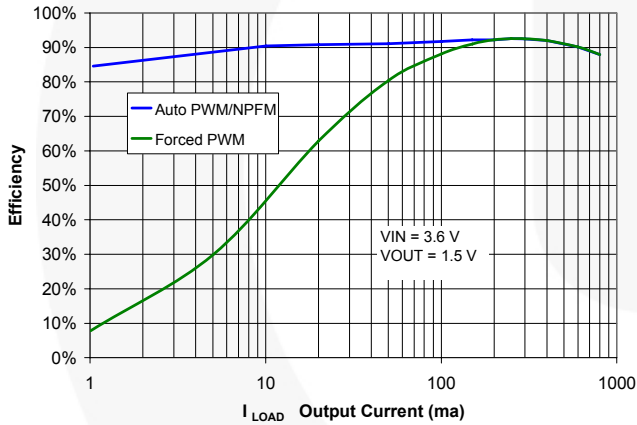


Figure 9. Efficiency vs. Load at  $V_{OUT} = 1.50V$

## Typical Performance Characteristics

Unless otherwise specified, Auto-PWM/NPFM,  $V_{IN} = 3.6V$ ,  $T_A = 25^\circ C$ , and recommended components as specified in Table 1.

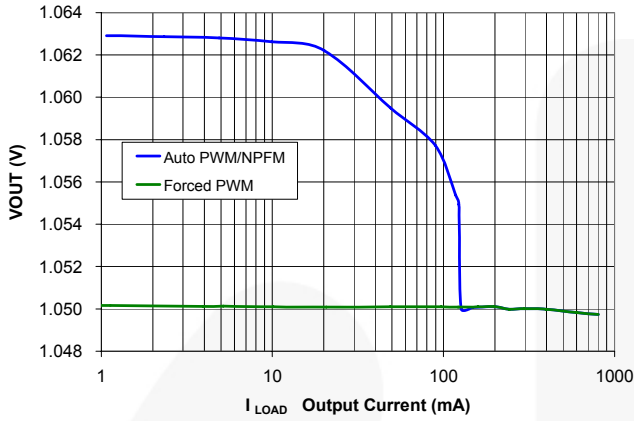


Figure 10. Load Regulation at  $V_{OUT} = 1.05V$

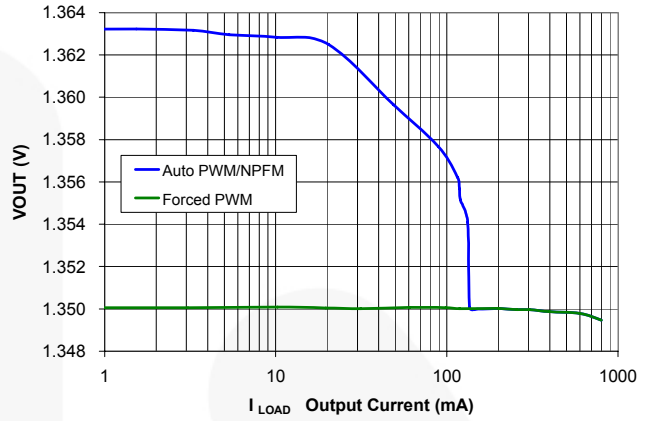


Figure 11. Load Regulation at  $V_{OUT} = 1.35V$

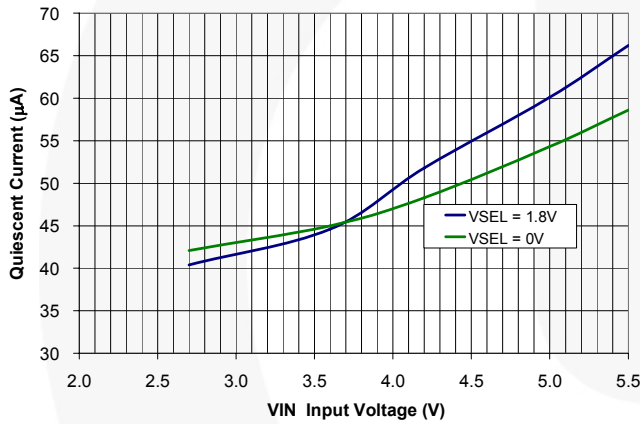


Figure 12. Quiescent Current,  $I_{LOAD} = 0$ ,  $EN = 1.8V$

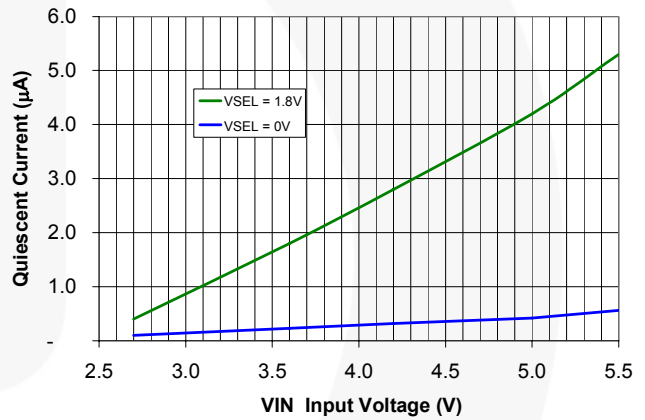


Figure 13. Shutdown Current,  $I_{LOAD} = 0$ ,  $EN = 0$

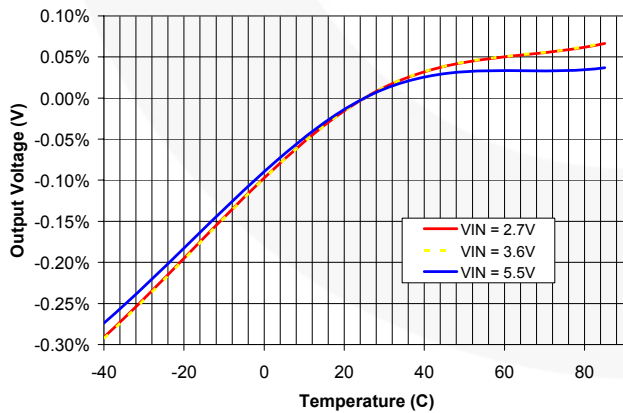


Figure 14. %  $V_{OUT}$  Shift vs. Temperature (Normalized)

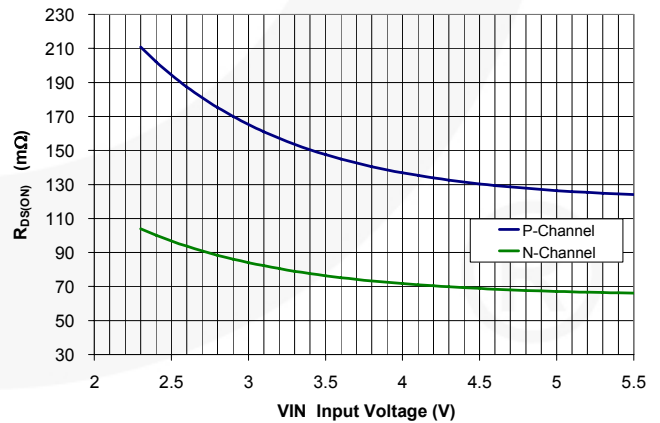


Figure 15. Output Stage  $R_{DS(ON)}$  vs.  $V_{IN}$

### Typical Performance Characteristics (Continued)

Unless otherwise specified,  $V_{IN} = 3.6V$ ,  $V_{OUT} = 1.35V$ , and load step  $t_R = t_F < 100ns$ .

#### Load Transient Response

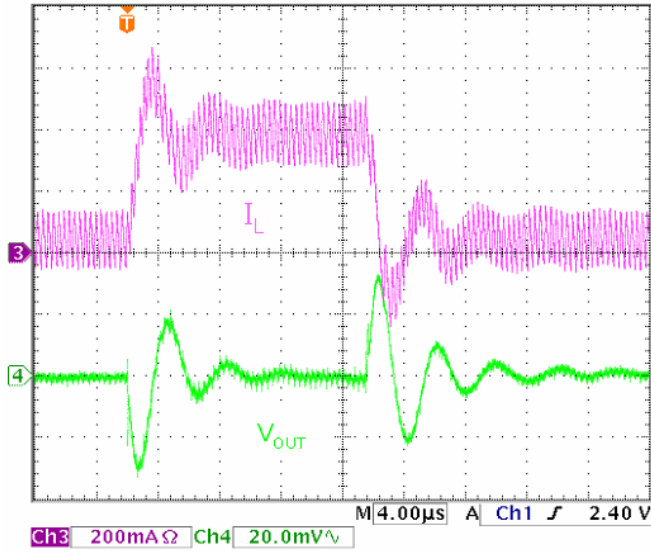


Figure 16. 50mA to 400mA to 50mA, Forced PWM

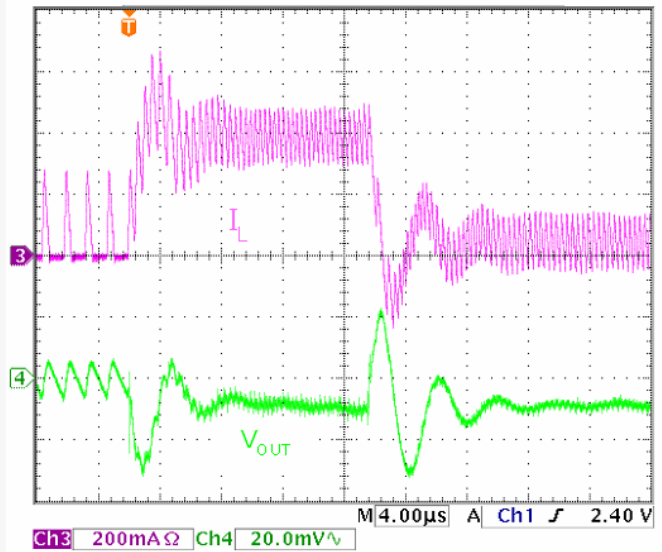


Figure 17. 50mA to 400mA to 50mA, Auto PWM/NPFM

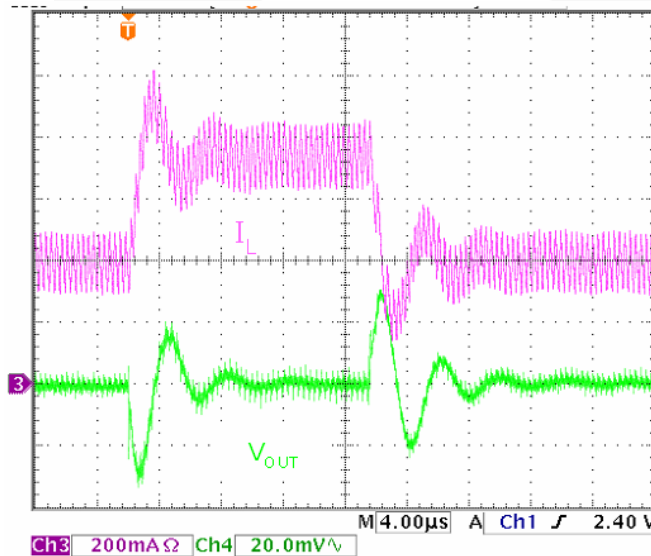


Figure 18. 400mA to 750mA to 400mA, Auto PWM/NPFM

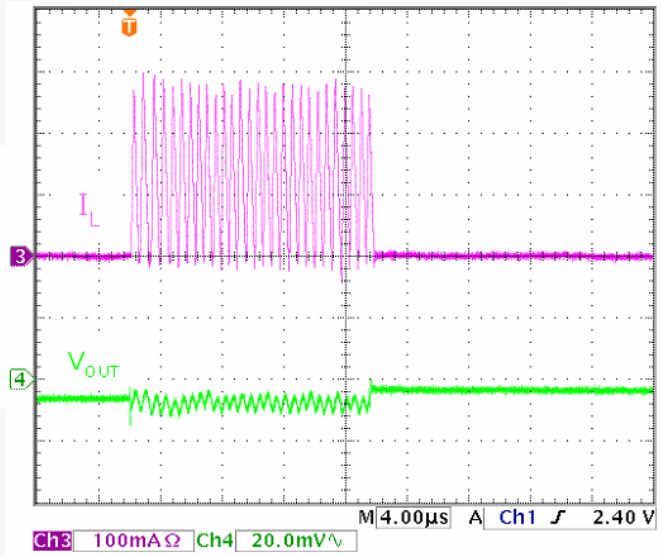


Figure 19. 0mA to 125mA to 0mA, Auto PWM/NPFM

**Typical Performance Characteristics** (Continued)

Unless otherwise specified,  $V_{IN} = 3.6V$ .

**VSEL Transitions**

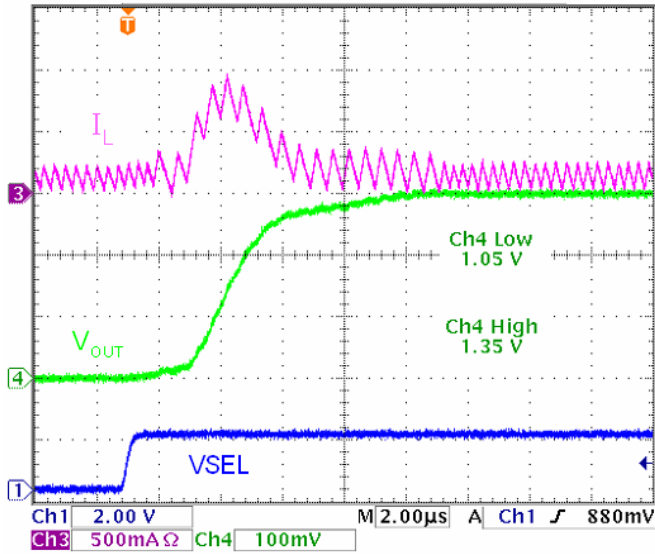


Figure 20. Single-Step,  $R_{LOAD} = 6.2\Omega$

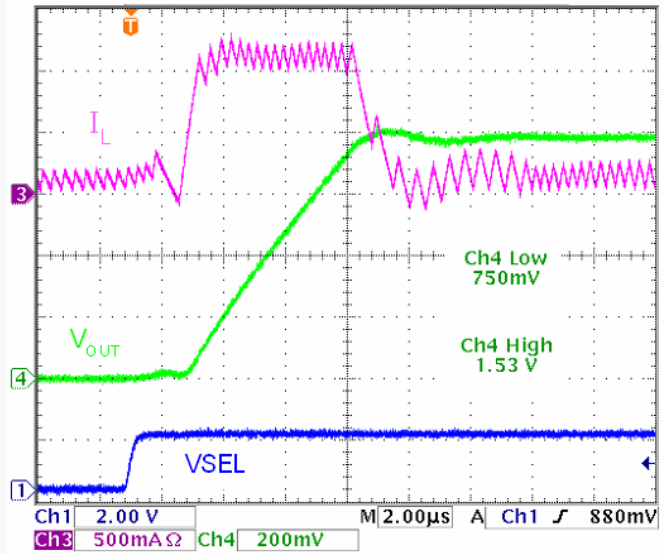


Figure 21. Single-Step,  $R_{LOAD} = 6.2\Omega$

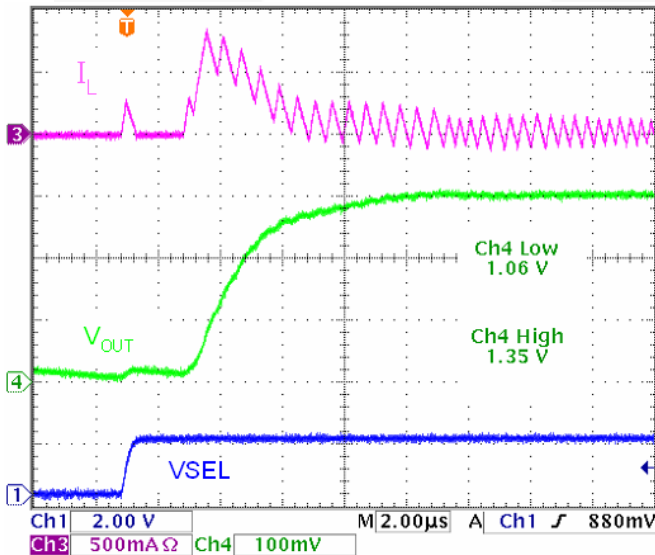


Figure 22. Single-Step,  $R_{LOAD} = 50\Omega$

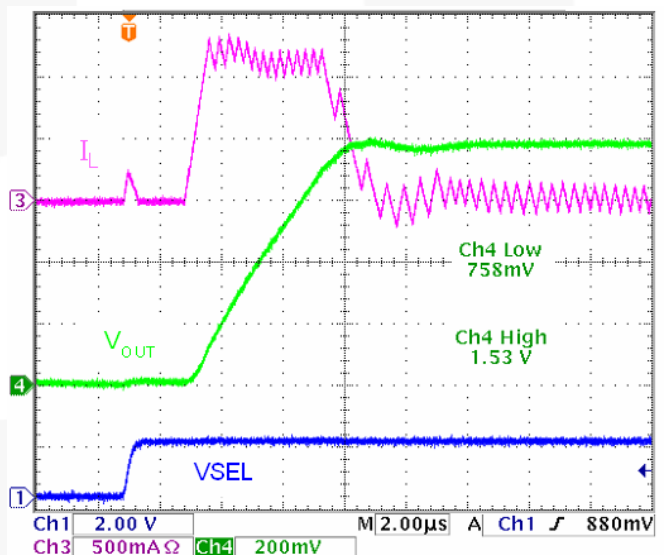


Figure 23. Single-Step,  $R_{LOAD} = 50\Omega$

## Typical Performance Characteristics (Continued)

Unless otherwise specified,  $V_{IN} = 3.6V$ .

### VSEL Transitions

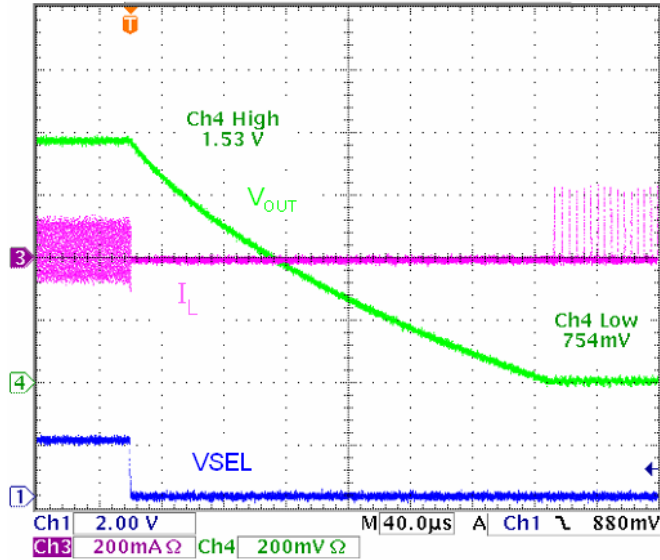


Figure 24. Single-Step from Forced PWM (MODE1=0),  $R_{LOAD} = 50\Omega$

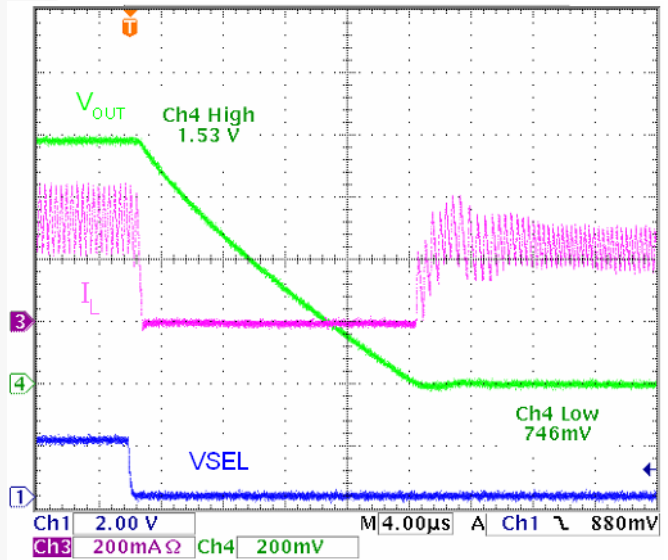


Figure 25. Single Step,  $R_{LOAD} = 6.2\Omega$

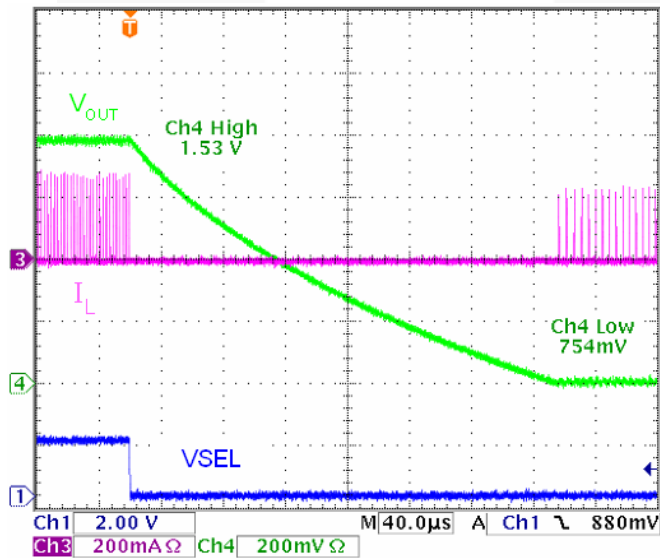


Figure 26. Single-Step from Auto PWM/PFM (MODE1=1),  $R_{LOAD} = 50\Omega$

**Typical Performance Characteristics** (Continued)

$R_{LOAD}$  is switched with N-channel MOSFET from  $V_{OUT}$  to GND.  $V_{IN} = 3.6V$ , initial  $V_{OUT} = 1.35V$ , initial  $I_{LOAD} = 0mA$ .

**Short Circuit and Over-Current Fault Response**

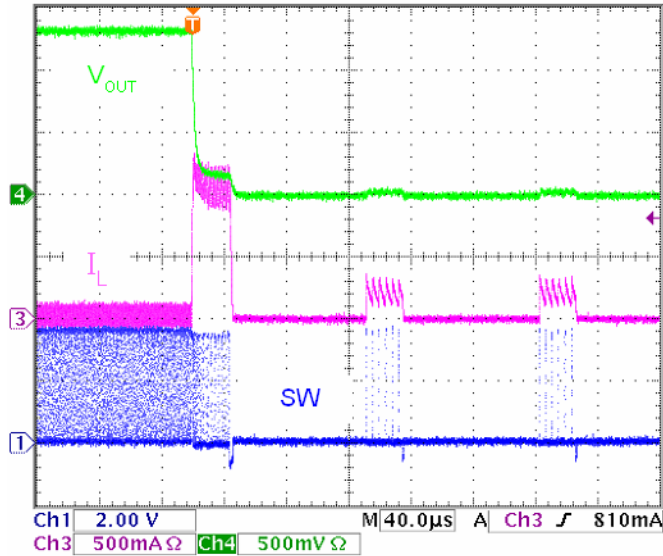


Figure 27. Metallic Short Applied at  $V_{OUT}$

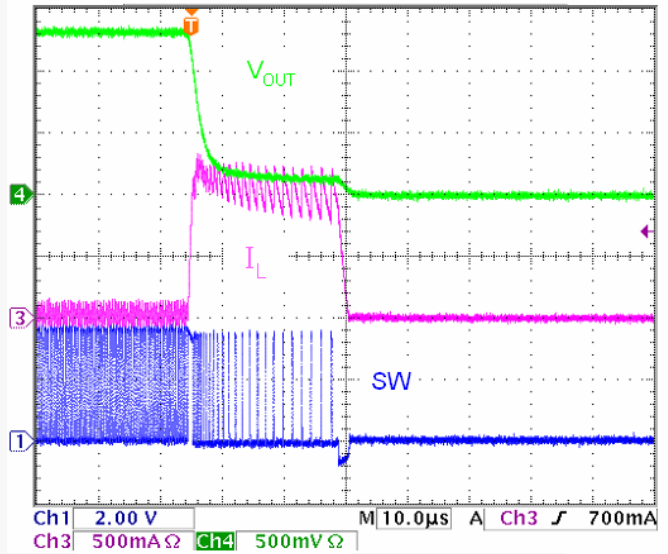


Figure 28. Metallic Short Applied at  $V_{OUT}$

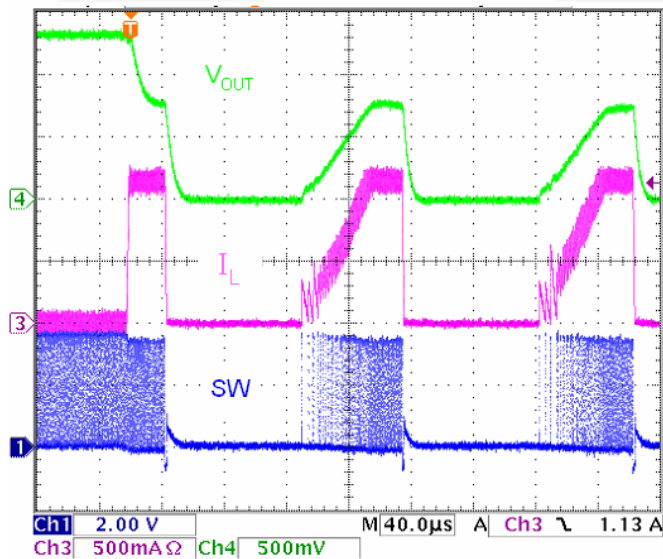


Figure 29.  $R_{LOAD} = 660m\Omega$

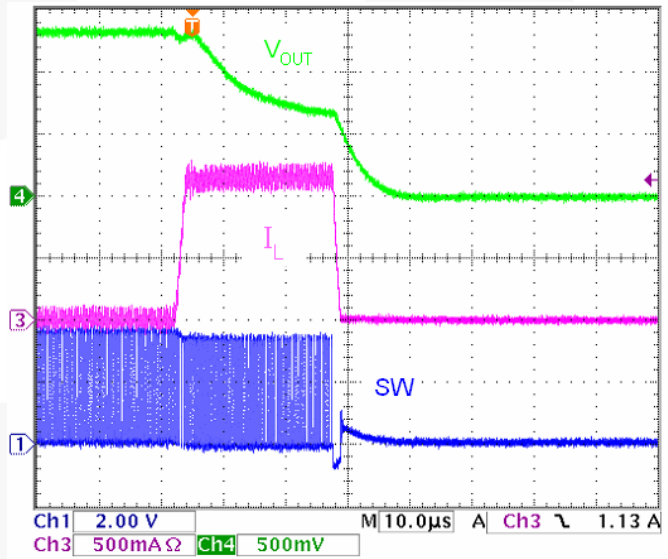
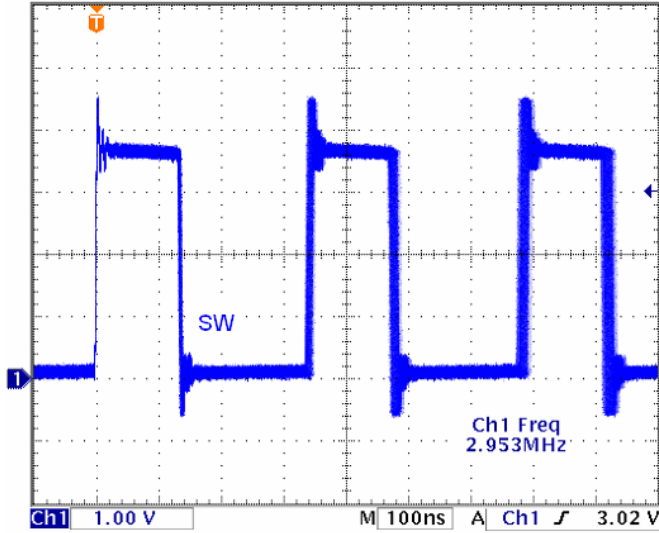


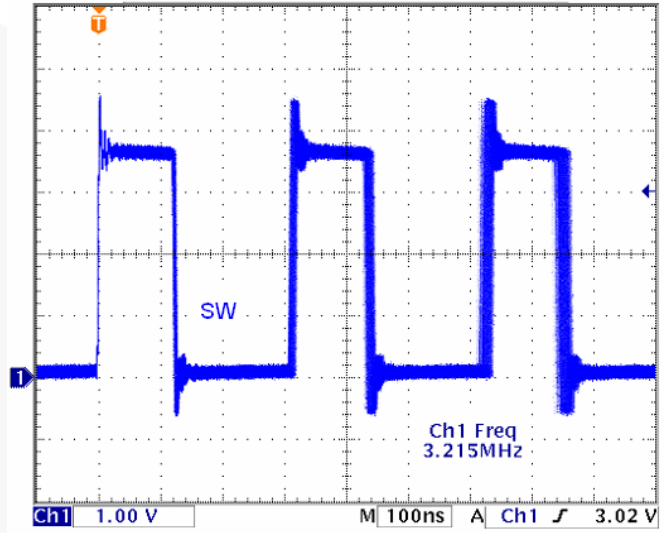
Figure 30.  $R_{LOAD} = 660m\Omega$

**Typical Performance Characteristics** (Continued)

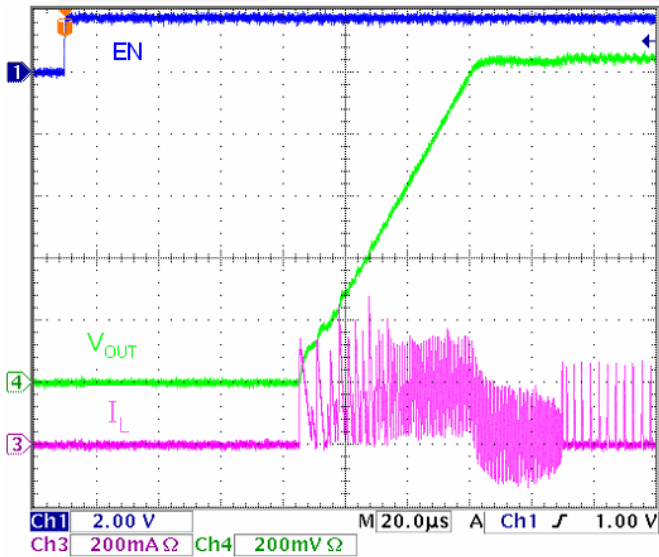
Unless otherwise specified,  $V_{IN} = 3.6V$ .



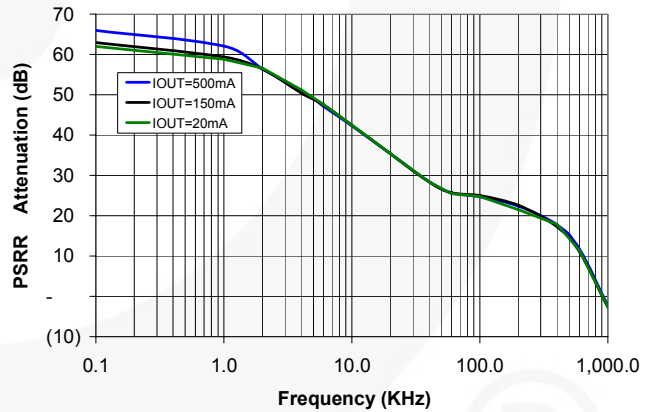
**Figure 31. SW-Node Jitter (Infinite Persistence),  $I_{LOAD} = 200mA$**



**Figure 32. SW-Node Jitter, External Synchronization (Infinite Persistence),  $I_{LOAD} = 200mA$**



**Figure 33. Soft-Start,  $R_{LOAD} = 50\Omega$**



**Figure 34.  $V_{IN}$  Ripple Rejection (PSRR)**



## Circuit Description

### Overview

The FAN5355 is a synchronous buck regulator that typically operates at 3MHz with moderate to heavy load currents. At light load currents, the converter operates in power-saving PFM mode. The regulator automatically transitions between fixed-frequency PWM and variable-frequency PFM mode to maintain the highest possible efficiency over the full range of load current.

The FAN5355 uses a very fast non-linear control architecture to achieve excellent transient response with minimum-sized external components.

The FAN5355 integrates an I<sup>2</sup>C-compatible interface, allowing transfers up to 3.4Mbps. This communication interface can be used to:

1. Dynamically re-program the output voltage in 12.5mV increments.
2. Reprogram the mode of operation to enable or disable PFM mode.
3. Control voltage transition slew rate.
4. Control the frequency of operation by synchronizing to an external clock.
5. Enable / disable the regulator.

For more details, refer to the I<sup>2</sup>C Interface and Register Description sections.

### Output Voltage Programming

Option	V <sub>OUT</sub> Equation	
00, 02, 03	$V_{OUT} = 0.75 + N_{VSEL} \cdot 12.5mV$	(1)
07	$V_{OUT} = 0.100 + N_{VSEL} \cdot 25mV$ for $N_{VSEL} = 0$ to 23  $V_{OUT} = 0.675 + (N_{VSEL} - 23) \cdot 12.5mV$ for $N_{VSEL} > 23$	(2)
06	$V_{OUT} = 1.1875 + N_{VSEL} \cdot 12.5mV$	(3)

where  $N_{VSEL}$  is the decimal value of the setting of the VSEL register that controls  $V_{OUT}$ .

#### Note:

13. Option 02 maximum voltage is 1.4375V (see Table 3).

### Power-up, EN, and Soft-start

All internal circuits remain de-biased and the IC is in a very low quiescent current state until the following are true:

1.  $V_{IN}$  is above its rising UVLO threshold, and
2. EN is HIGH.

At that point, the IC begins a soft-start cycle, its I<sup>2</sup>C interface is enabled, and its registers loaded with their default values.

During the initial soft-start,  $V_{OUT}$  ramps linearly to the setpoint programmed in the VSEL register selected by the VSEL pin. The soft start features a fixed output voltage slew rate of 18.75V/ms, and achieves regulation approximately 90 $\mu$ s after EN rises. PFM mode is enabled during soft-start until the output is in regulation, regardless of the MODE bit settings. This allows the regulator to start into a partially charged output without discharging it; in other words, the regulator does not allow current to flow from the load back to the battery.

As soon as the output has reached its setpoint, the control forces PWM mode for about 85 $\mu$ s to allow all internal control circuits to calibrate.

Symbol	Description	Value ( $\mu$ s)	
$t_{SSDLY}$	Time from EN to start of soft-start ramp	25	
$t_{REG}$	$V_{OUT}$ ramp start to regulation	Opt 06	$16 + (VSEL - 0.7) \times 53$
		Others	$(VSEL - 0.1) \times 53$
$t_{POK}$	PWROK (CONTROL2[5]) rising from $t_{REG}$	11	
$t_{CAL}$	Regulator stays in PWM mode during this time	10	

Table 2. Soft-Start Timing (see Figure 35)

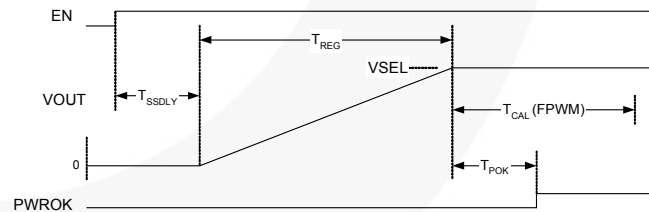


Figure 35. Soft-start Timing

VSEL Value			VOUT		
Dec	Binary	Hex	00, 03	02	06
0	000000	00	0.7500	0.7500	1.1875
1	000001	01	0.7625	0.7625	1.2000
2	000010	02	0.7750	0.7750	1.2125
3	000011	03	0.7875	0.7875	1.2250
4	000100	04	0.8000	0.8000	1.2375
5	000101	05	0.8125	0.8125	1.2500
6	000110	06	0.8250	0.8250	1.2625
7	000111	07	0.8375	0.8375	1.2750
8	001000	08	0.8500	0.8500	1.2875
9	001001	09	0.8625	0.8625	1.3000
10	001010	0A	0.8750	0.8750	1.3125
11	001011	0B	0.8875	0.8875	1.3250
12	001100	0C	0.9000	0.9000	1.3375
13	001101	0D	0.9125	0.9125	1.3500
14	001110	0E	0.9250	0.9250	1.3625
15	001111	0F	0.9375	0.9375	1.3750
16	010000	10	0.9500	0.9500	1.3875
17	010001	11	0.9625	0.9625	1.4000
18	010010	12	0.9750	0.9750	1.4125
19	010011	13	0.9875	0.9875	1.4250
20	010100	14	1.0000	1.0000	1.4375
21	010101	15	1.0125	1.0125	1.4500
22	010110	16	1.0250	1.0250	1.4625
23	010111	17	1.0375	1.0375	1.4750
24	011000	18	1.0500	1.0500	1.4875
25	011001	19	1.0625	1.0625	1.5000
26	011010	1A	1.0750	1.0750	1.5125
27	011011	1B	1.0875	1.0875	1.5250
28	011100	1C	1.1000	1.1000	1.5375
29	011101	1D	1.1125	1.1125	1.5500
30	011110	1E	1.1250	1.1250	1.5625
31	011111	1F	1.1375	1.1375	1.5750
32	100000	20	1.1500	1.1500	1.5875
33	100001	21	1.1625	1.1625	1.6000
34	100010	22	1.1750	1.1750	1.6125
35	100011	23	1.1875	1.1875	1.6250
36	100100	24	1.2000	1.2000	1.6375
37	100101	25	1.2125	1.2125	1.6500
38	100110	26	1.2250	1.2250	1.6625
39	100111	27	1.2375	1.2375	1.6750
40	101000	28	1.2500	1.2500	1.6875
41	101001	29	1.2625	1.2625	1.7000
42	101010	2A	1.2750	1.2750	1.7125
43	101011	2B	1.2875	1.2875	1.7250
44	101100	2C	1.3000	1.3000	1.7375
45	101101	2D	1.3125	1.3125	1.7500
46	101110	2E	1.3250	1.3250	1.7625
47	101111	2F	1.3375	1.3375	1.7750
48	110000	30	1.3500	1.3500	1.7875
49	110001	31	1.3625	1.3625	1.8000
50	110010	32	1.3750	1.3750	1.8125
51	110011	33	1.3875	1.3875	1.8250
52	110100	34	1.4000	1.4000	1.8375
53	110101	35	1.4125	1.4125	1.8500
54	110110	36	1.4250	1.4250	1.8625
55	110111	37	1.4375	1.4375	1.8750
56	111000	38	1.4500	1.4375	1.8875
57	111001	39	1.4625	1.4375	1.9000
58	111010	3A	1.4750	1.4375	1.9125
59	111011	3B	1.4875	1.4375	1.9250
60	111100	3C	1.5000	1.4375	1.9375
61	111101	3D	1.5125	1.4375	1.9500
62	111110	3E	1.5250	1.4375	1.9625
63	111111	3F	1.5375	1.4375	1.9750

Table 3. VSEL vs. VOUT for Options 00, 02, 03, 06

VSEL		
Dec	Hex	VOUT
0	00	0.1000
1	01	0.1250
2	02	0.1500
3	03	0.1750
4	04	0.2000
5	05	0.2250
6	06	0.2500
7	07	0.2750
8	08	0.3000
9	09	0.3250
10	0A	0.3500
11	0B	0.3750
12	0C	0.4000
13	0D	0.4250
14	0E	0.4500
15	0F	0.4750
16	10	0.5000
17	11	0.5250
18	12	0.5500
19	13	0.5750
20	14	0.6000
21	15	0.6250
22	16	0.6500
23	17	0.6750
24	18	0.6875
25	19	0.7000
26	1A	0.7125
27	1B	0.7250
28	1C	0.7375
29	1D	0.7500
30	1E	0.7625
31	1F	0.7750
32	20	0.7875
33	21	0.8000
34	22	0.8125
35	23	0.8250
36	24	0.8375
37	25	0.8500
38	26	0.8625
39	27	0.8750
40	28	0.8875
41	29	0.9000
42	2A	0.9125
43	2B	0.9250
44	2C	0.9375
45	2D	0.9500
46	2E	0.9625
47	2F	0.9750
48	30	0.9875
49	31	1.0000
50	32	1.0125
51	33	1.0250
52	34	1.0375
53	35	1.0500
54	36	1.0625
55	37	1.0750
56	38	1.0875
57	39	1.1000
58	3A	1.1125
59	3B	1.1250
60	3C	1.1375
61	3D	1.1500
62	3E	1.1625
63	3F	1.1750

Table 4. VSEL vs. VOUT for Option 07

VSEL		
Dec	Hex	VOUT
64	00	1.1875
65	01	1.2000
66	02	1.2125
67	03	1.2250
68	04	1.2375
69	05	1.2500
70	06	1.2625
71	07	1.2750
72	08	1.2875
73	09	1.3000
74	0A	1.3125
75	0B	1.3250
76	0C	1.3375
77	0D	1.3500
78	0E	1.3625
79	0F	1.3750
80	10	1.3875
81	11	1.4000
82	12	1.4125
83	13	1.4250
84	14	1.4375
85	15	1.4500
86	16	1.4625
87	17	1.4750
88	18	1.4875
89	19	1.5000
90	1A	1.5125
91	1B	1.5250
92	1C	1.5375
93	1D	1.5500
94	1E	1.5625
95	1F	1.5750
96	20	1.5875
97	21	1.6000
98	22	1.6125
99	23	1.6250
100	24	1.6375
101	25	1.6500
102	26	1.6625
103	27	1.6750
104	28	1.6875
105	29	1.7000
106	2A	1.7125
107	2B	1.7250
108	2C	1.7375
109	2D	1.7500
110	2E	1.7625
111	2F	1.7750
112	30	1.7875
113	31	1.8000
114	32	1.8125
115	33	1.8250
116	34	1.8375
117	35	1.8500
118	36	1.8625
119	37	1.8750
120	38	1.8875
121	39	1.9000
122	3A	1.9125
123	3B	1.9250
124	3C	1.9375
125	3D	1.9500
126	3E	1.9625
127	3F	1.9750

## Software Enable

The EN\_DCDC bit, VSELx[7] can be used to enable the regulator in conjunction with the EN pin. Setting EN\_DCDC with EN HIGH begins the soft-start sequence described above.

EN_DCDC Bit	EN Pin	I <sup>2</sup> C	REGULATOR
0	0	OFF	OFF
1	1	ON	ON
1	0	OFF	OFF
0	1	ON	OFF

**Table 5. EN\_DCDC Behavior**

## Light-Load (PFM) Operation

The FAN5355 offers both a Normal PFM (NPFM) and Enhanced PFM (EPFM) mode. NPFM is normally used when the load current is very low and when quiescent current must be minimized. EPFM provides more accurate DC regulation and limits the minimum frequency to 25kHz typical to prevent operation in the audio band.

V<sub>OUT</sub> ripple is identical in both modes (less than 20mV), and both modes feature very fast response to load transients.

The FAN5355 incorporates a single-pulse, light-load modulation that ensures:

- Smooth transitions between PFM and PWM modes
- Minimum frequency, of 25kHz typical, to avoid audible noise (EPFM only)
- Single-pulse operation for low ripple
- Predictable PFM entry and exit currents.

PFM begins after the inductor current has become discontinuous, crossing zero during the PWM cycle in 32 consecutive cycles. PFM exit occurs when discontinuous current mode (DCM) operation cannot supply sufficient current to maintain regulation. During PFM mode, the inductor current ripple is about 40% higher than in PWM mode. The load current required to exit PFM mode is thereby about 20% higher than the load current required to enter PFM mode, providing sufficient hysteresis to prevent “mode chatter.”

While PWM ripple voltage is typically less than 4mV<sub>P-P</sub>, PFM ripple voltage can be up to 30mV<sub>P-P</sub> during very light load. To prevent significant undershoot when a load transient occurs, the initial DC setpoint for the regulator in PFM mode is set 10mV higher than in PWM mode. This offset decays to about 5mV after the regulator has been in PFM mode for ~100μs. The maximum instantaneous voltage in PFM is 30mV above the setpoint.

In Enhanced PFM (EPFM) mode, the regulator maintains a minimum frequency of 25kHz (typical) to prevent audible noise being generated by the external components. To achieve this, the regulator turns on the low-side MOSFET to

“create demand” for a pulse if no pulse had been required for 40μs. The minimum frequency limit circuit takes effect with load currents below about 3.5mA. Above that load point, the natural PFM period is less than 40μs. This circuit only activates when I<sub>LOAD</sub> is greater than ~3.5mA. If the load remains above 3.5mA, there is no quiescent current penalty for EPFM mode and there is some accuracy advantage.

NPFM allows the switching frequency (f<sub>SW</sub>) to go as low as required to support the load current. This achieves a lower quiescent current than EPFM, but sacrifices up to ±15mV of DC accuracy when compared to EPFM or PWM modes. As shown in Table 6, EPFM and NPFM modes have the same frequency when the load is above 4mA. If the load is above 4mA, EPFM is the preferred mode, since it has tighter DC regulation with the same efficiency.

EPFM can only be enabled by setting the MODE\_CTRL bits to 11. In versions with MODE\_CTRL disabled (see Table 12), the PFM mode is NPFM.

Mode	EPFM	NPFM
I <sub>QUIESCENT</sub> typical at I <sub>LOAD</sub> = 0	110μA	38μA
DC Accuracy	Better	Good
f <sub>SW</sub> at I <sub>LOAD</sub> = 0	25 kHz	to 0 Hz
f <sub>SW</sub> at I <sub>LOAD</sub> > 3.5mA	> 33 kHz	> 33 kHz

**Table 6. PFM Modes Comparison**

PFM mode can be disabled by writing to the mode control bits: CONTROL1[3:0] (see Table 12 for details).

## Switching Frequency Control and Synchronization

The nominal internal oscillator frequency is 3MHz. The regulator runs at its internal clock frequency until these conditions are met:

1. EN\_SYNC bit, CONTROL1[5], is set; and
2. A valid frequency appears on the SYNC pin.

CONTROL2		F <sub>SYNC</sub> Valid		
PLL_MULT	f <sub>SYNC</sub> Divider	Min.	Typ.	Max.
00	1	2.25	3.00	4.00
01	2	1.13	1.50	2.00
10	3	0.75	1.00	1.33
11	4	0.56	0.75	1.00

**Table 7. SYNC Frequency Validation for f<sub>OSC(INTERNAL)</sub>=3.0MHz**

If the EN\_SYNC is set and SYNC fails validation, the regulator continues to run at its internal oscillator frequency. The regulator is functional if f<sub>SYNC</sub> is valid, as defined in Table 7, but its performance is compromised if f<sub>SYNC</sub> is outside the f<sub>SYNC</sub> window in the Electrical Specifications.

When CONTROL1[3:2] = 00 and the VSEL line is LOW, the converter operates according to the MODE0 bit, CONTROL1[0], with synchronization disabled regardless of the state of the EN\_SYNC and HW\_nSW bits.

## Output Voltage Transitions

The IC regulates  $V_{OUT}$  to one of two setpoint voltages, as determined by the VSEL pin and the HW\_nSW bit.

VSEL Pin	HW_nSW Bit	$V_{OUT}$ Setpoint <sup>(14)</sup>	PFM
0	1	VSEL0	Allowed
1	1	VSEL1	Per MODE1
x	0	VSEL1	Per MODE1

**Table 8.  $V_{OUT}$  Setpoint and Mode Control MODE\_CTRL, CONTROL1[3:2] = 00**

### Note:

14. Option 07 uses VSELx[6:0] to set  $V_{OUT}$ , while all other options use VSELx[5:0].

If HW\_nSW = 0,  $V_{OUT}$  transitions are initiated through the following sequence:

1. Write the new setpoint in VSEL1.
2. Write desired transition rate in DEFSLEW, CONTROL2[2:0], and set the GO bit in CONTROL2[7].

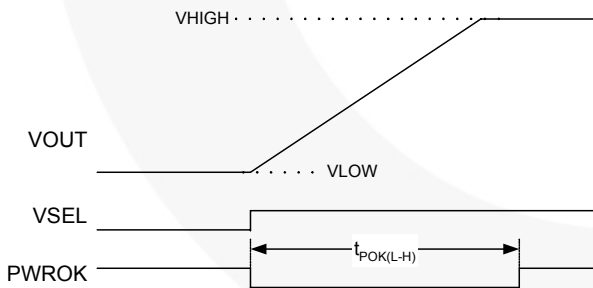
If HW\_nSW = 1,  $V_{OUT}$  transitions are initiated either by changing the state of the VSEL pin or by writing to the VSEL register selected by the VSEL pin.

### Positive Transitions

When transitioning to a higher  $V_{OUT}$ , the regulator can perform the transition using multi-step or single-step mode.

#### Multi-step Mode:

The internal DAC is stepped at a rate defined by DEFSLEW, CONTROL2[2:0], ranging from 000 to 110. This mode minimizes the current required to charge  $C_{OUT}$  and thereby minimizes the current drain from the battery when transitioning. The PWROK bit, CONTROL2[5], remains LOW until about 1.5 $\mu$ s after the DAC completes its ramp.



**Figure 36. Multi-step  $V_{OUT}$  Transition**

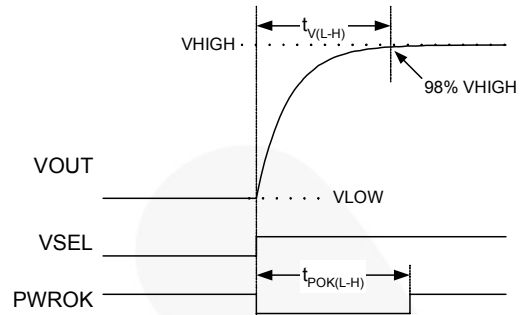
#### Single-step Mode:

Used if DEFSLEW, CONTROL2[2:0] = 111. The internal DAC is immediately set to the higher voltage and the regulator performs the transition as quickly as its current limit circuit allows, while avoiding excessive overshoot.

Figure 37 shows single-step transition timing.  $t_{V(L-H)}$  is the time it takes the regulator to settle to within 2% of the new

setpoint and is typically 7 $\mu$ s for a full-range transition (from 00000 to 11111 for 6-bit DAC options). The PWROK bit, CONTROL2[5], goes LOW until the transition is complete and  $V_{OUT}$  settled. This typically occurs  $\sim$ 2 $\mu$ s after  $t_{V(L-H)}$ .

It is good practice to reduce the load current before making positive VSEL transitions. This reduces the time required to make positive load transitions and avoids current-limit-induced overshoot.



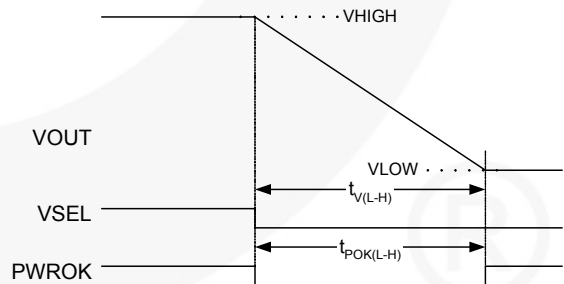
**Figure 37. Single-Step  $V_{OUT}$  Transition**

All positive  $V_{OUT}$  transitions inhibit PFM until the transition is complete, which occurs at the end of  $t_{POK(L-H)}$ .

### Negative Transitions

When moving from VSEL=1 to VSEL=0, the regulator enters PFM mode, regardless of the condition of the SYNC pin or MODE bits, and remains in PFM until the transition is completed. Reverse current through the inductor is blocked, and the PFM minimum frequency control inhibited, until the new setpoint is reached, at which time the regulator resumes control using the mode established by MODE\_CTRL. The transition time from  $V_{HIGH}$  to  $V_{LOW}$  is controlled by the load current and output capacitance as:

$$t_{V(H-L)} = C_{OUT} \cdot \frac{V_{HIGH} - V_{LOW}}{I_{LOAD}} \quad (4)$$



**Figure 38. Negative  $V_{OUT}$  Transition**

## Protection Features

### Current Limit / Auto-Restart

The regulator includes cycle-by-cycle current limiting, which prevents the instantaneous inductor current from exceeding ~1350mA.

The IC enters “fault” mode after sustained over-current. If current limit is asserted for more than 32 consecutive cycles (about 20μs), the IC returns to shutdown state and remains in that condition for ~80μs. After that time, the regulator attempts to restart with a normal soft-start cycle. If the fault has not cleared, it shuts down ~10μs later.

If the fault is a short circuit, the initial current limit is ~30% of the normal current limit, which produces a very small drain on the system power source.

### Thermal Protection

When the junction temperature of the IC exceeds 150°C, the device turns off all output MOSFETs and remains in a low quiescent current state until the die cools to 130°C before commencing a normal soft-start cycle.

### Under-Voltage Lockout (UVLO)

The IC turns off all MOSFETs and remains in a very low quiescent current state until  $V_{IN}$  rises above the UVLO threshold.

## I<sup>2</sup>C Interface

The FAN5355’s serial interface is compatible with standard, fast, and HS mode I<sup>2</sup>C bus specifications. The FAN5355’s SCL line is an input and its SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

SDA and SCL are normally pulled up to a system I/O power supply (VCCIO), as shown in Figure 1. If the I<sup>2</sup>C interface is not used, SDA and SCL should be tied to AVIN to minimize quiescent current consumption.

## Addressing

FAN5355 has four user-accessible registers:

	Address							
	7	6	5	4	3	2	1	0
VSEL0	0	0	0	0	0	0	0	0
VSEL1	0	0	0	0	0	0	0	1
CONTROL1	0	0	0	0	0	0	1	0
CONTROL2	0	0	0	0	0	0	1	1

Table 9. I<sup>2</sup>C Register Addresses

## Slave Address

In Table 10, A1 and A0 are according to the Ordering Information table on page 2.

7	6	5	4	3	2	1	0
1	0	0	1	0	A1	A0	R/W

Table 10. I<sup>2</sup>C Slave Address

## Bus Timing

As shown in Figure 39, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

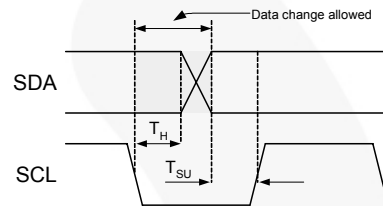


Figure 39. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a “START” condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 40.

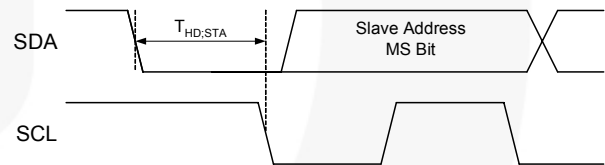


Figure 40. Start Bit

A transaction ends with a “STOP” condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 41.

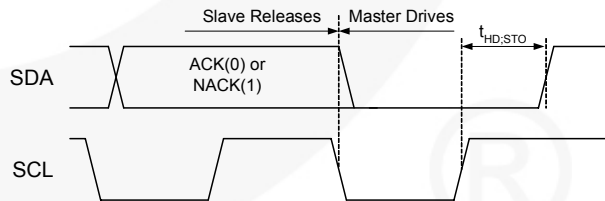


Figure 41. Stop Bit

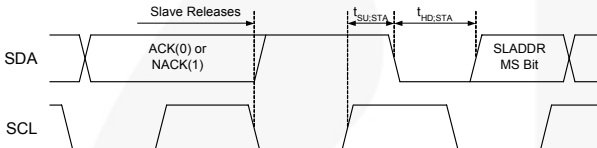
During a read from the FAN5355 (Figure 44), the master issues a “Repeated Start” after sending the register address, and before resending the slave address. The “Repeated Start” is a 1 to 0 transition on SDA while SCL is HIGH, as shown in Figure 42.

## High-Speed (HS) Mode

The protocols for High-Speed (HS), Low-Speed (LS), and Fast-Speed (FS) modes are identical, except the bus speed for HS mode is 3.4MHz. HS mode is entered when the bus master sends the HS master code 00001XXX after a start condition. The master code is sent in FS mode (less than 400kHz clock) and slaves do not ACK this transmission.

The master then generates a repeated start condition (Figure 42) that causes all slaves on the bus to switch to HS mode. The master then sends I<sup>2</sup>C packets, as described above, using the HS mode clock rate and timing.

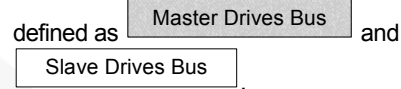
The bus remains in HS mode until a stop bit (Figure 41) is sent by the master. While in HS mode, packets are separated by repeated start conditions (Figure 42).



**Figure 42. Repeated Start Timing**

## Read and Write Transactions

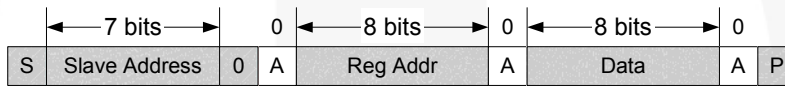
The following figures outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as



All addresses and data are MSB first.

Symbol	Definition
S	START, <i>see Figure 40.</i>
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet.
$\bar{A}$	NACK. The slave sends a 1 to NACK the preceding packet.
R	Repeated START, <i>see Figure 42.</i>
P	STOP, <i>see Figure 41.</i>

**Table 11. I<sup>2</sup>C Bit Definitions for Figure 43 - Figure 44**



**Figure 43. Write Transaction**



**Figure 44. Read Transaction**

## Register Descriptions

### Default Values

Each option of the FAN5355 (see *Ordering Information on page 2*) has different default values for the some of the register bits. Table 12 defines both the default values and the bit's type (as defined in Table 13) for each available option.

VSEL0										VSEL1									
Option	7	6	5	4	3	2	1	0	V <sub>OUT</sub>	Option	7	6	5	4	3	2	1	0	V <sub>OUT</sub>
00	1	1	0	1	1	0	0	0	1.05	00	1	1	1	1	0	0	0	0	1.35
02	1	1	0	1	1	0	0	0	1.05	02	1	1	1	0	0	1	0	0	1.20
03	1	1	0	1	0	1	0	0	1.00	03	1	1	1	0	0	1	0	0	1.20
07	1	1	0	1	1	0	0	0	1.05	07	1	1	1	1	0	0	0	0	1.35
06	1	1	1	1	0	0	0	1	1.80	06	1	1	1	1	0	0	0	1	1.80

CONTROL1										CONTROL2									
Option	7	6	5	4	3	2	1	0		Option	7	6	5	4	3	2	1	0	
00, 02	1	0	0	1	0	0	0	0		00, 02	0	0	0	0	0	1	1	1	
03	0	0	0	1	0	0	0	0		03	0	0	0	0	0	1	1	1	
06, 07	1	0	0	1	0	0	0	0		06, 07	0	0	0	0	0	1	1	1	

**Table 12. Default Values and Bit Types for VSEL and CONTROL Registers**

#	<b>Active bit.</b> Changing this bit changes the behavior of the converter, as described below.
#	<b>Disabled.</b> Converter logic ignores changes made to this bit. Bit can be written to and read-back.
#	<b>Read-only.</b> Writing to this bit through I <sup>2</sup> C does not change the read-back value, nor does it change converter behavior.

**Table 13. Bit Type Definitions for Table 12.**

## Bit Definitions

The following table defines the operation of each register bit. Superscript characters define the default state for each option. Superscripts <sup>0,2,3,6,7</sup> signify the default values for options 00, 02, 03, 06, and 07, respectively. <sup>A</sup> signifies the default for all options.

Bit	Name	Value	Description
<b>VSEL0</b> Register Address: 00			
7	EN_DCDC	0	Device in shutdown regardless of the state of the EN pin. This bit is mirrored in VSEL1. A write to bit 7 in either register establishes the EN_DCDC value.
		1 <sup>A</sup>	Device enabled when EN pin is HIGH, disabled when EN is LOW.
6	Reserved <sup>0,2,3,6</sup> or DAC6 <sup>7</sup>	Table 12	Has no effect in options 00, 02, 03, 06, and defaults to 1. In option 07, it is the MSB of the 7-bit DAC value to set V <sub>OUT</sub> .
5:0	DAC[5:0]		6-bit DAC value to set V <sub>OUT</sub> . The six LSBs of the 7-bit value for option 07.
<b>VSEL1</b> Register Address: 01			
7	EN_DCDC	0	Device in shutdown regardless of the state of the EN pin. This bit is mirrored in VSEL0. A write to bit 7 in either register establishes the EN_DCDC value.
		1 <sup>A</sup>	Device enabled when EN pin is HIGH, disabled when EN is LOW.
6	Reserved <sup>0,2,3,6</sup> or DAC6 <sup>7</sup>	Table 12	Has no effect in options 00, 02, 03, 06, and defaults to 1. In option 07, it is the MSB of the 7-bit DAC value to set V <sub>OUT</sub> .
5:0	DAC[5:0]		6-bit DAC value to set V <sub>OUT</sub> . The six LSBs of the 7-bit value for option 07.
<b>CONTROL1</b> Register Address: 02			
7:6	Reserved	10 <sup>0,2,5,6</sup> 00 <sup>3</sup>	Vendor ID bits. Writing to these bits has no effect on regulator operation. These bits can be used to distinguish between vendors via I <sup>2</sup> C.
5	EN_SYNC	0 <sup>A</sup>	Disables external signal on SYNC from affecting the regulator.
		1	When a valid frequency is detected on SYNC, the regulator synchronizes to it and PFM is disabled, except when MODE = 00, VSEL pin = LOW, and HW_nSW = 1.
4	HW_nSW	0	V <sub>OUT</sub> is controlled by VSEL1. Voltage transitions occur by writing to the VSEL1, then setting the GO bit.
		1 <sup>A</sup>	V <sub>OUT</sub> is programmed by the VSEL pin. V <sub>OUT</sub> = VSEL1 when VSEL is HIGH, and VSEL0 when VSEL is LOW.
3:2	MODE_CTRL	00 <sup>A</sup>	Operation follows MODE0, MODE1.
		01	NPFM with automatically transitions to PWM, regardless of VSEL.
		10	PFM disabled (forced PWM), regardless of VSEL.
		11	EPFM (F <sub>SW(MIN)</sub> = 25kHz) with automatically transitions to PWM, regardless of VSEL.
1	MODE1	0 <sup>A</sup>	PFM disabled (forced PWM) when regulator output is controlled by VSEL1.
		1	NPFM with automatic transitions to PWM when regulator output is controlled by VSEL1.
0	MODE0	0 <sup>A</sup>	NPFM with automatic transitions to PWM when VSEL is LOW. Changing this bit has no effect on the operation of the regulator.
		1	
<b>CONTROL2</b> Register Address: 03			
7	GO	0 <sup>A</sup>	This bit has no effect when HW_nSW = 1. At the end of a V <sub>OUT</sub> transition, this bit is reset to 0.
		1	Starts a V <sub>OUT</sub> transition if HW_nSW = 0.
6	OUTPUT_DISCHARGE	0 <sup>A</sup>	When the regulator is disabled, V <sub>OUT</sub> is not discharged.
		1	When the regulator is disabled, V <sub>OUT</sub> discharges through an internal pull-down.
5	PWROK (read only)	0	V <sub>OUT</sub> is not in regulation or is in current limit.
		1	V <sub>OUT</sub> is in regulation.
4:3	PLL_MULT	00 <sup>A</sup>	f <sub>SW</sub> = f <sub>SYNC</sub> when synchronization is enabled.
		01	f <sub>SW</sub> = 2 X f <sub>SYNC</sub> when synchronization is enabled.
		10	f <sub>SW</sub> = 3 X f <sub>SYNC</sub> when synchronization is enabled.
		11	f <sub>SW</sub> = 4 X f <sub>SYNC</sub> when synchronization is enabled.
2:0	DEFSLEW	000	V <sub>OUT</sub> slews at 0.15mV/μs during positive V <sub>OUT</sub> transitions.
		001	V <sub>OUT</sub> slews at 0.30mV/μs during positive V <sub>OUT</sub> transitions.
		010	V <sub>OUT</sub> slews at 0.60mV/μs during positive V <sub>OUT</sub> transitions.
		011	V <sub>OUT</sub> slews at 1.20mV/μs during positive V <sub>OUT</sub> transitions.
		100	V <sub>OUT</sub> slews at 2.40mV/μs during positive V <sub>OUT</sub> transitions.
		101	V <sub>OUT</sub> slews at 4.80mV/μs during positive V <sub>OUT</sub> transitions.
		110	V <sub>OUT</sub> slews at 9.60mV/μs during positive V <sub>OUT</sub> transitions.
		111 <sup>A</sup>	Positive V <sub>OUT</sub> transitions use single-step mode (see Figure 37).



## Physical Dimensions

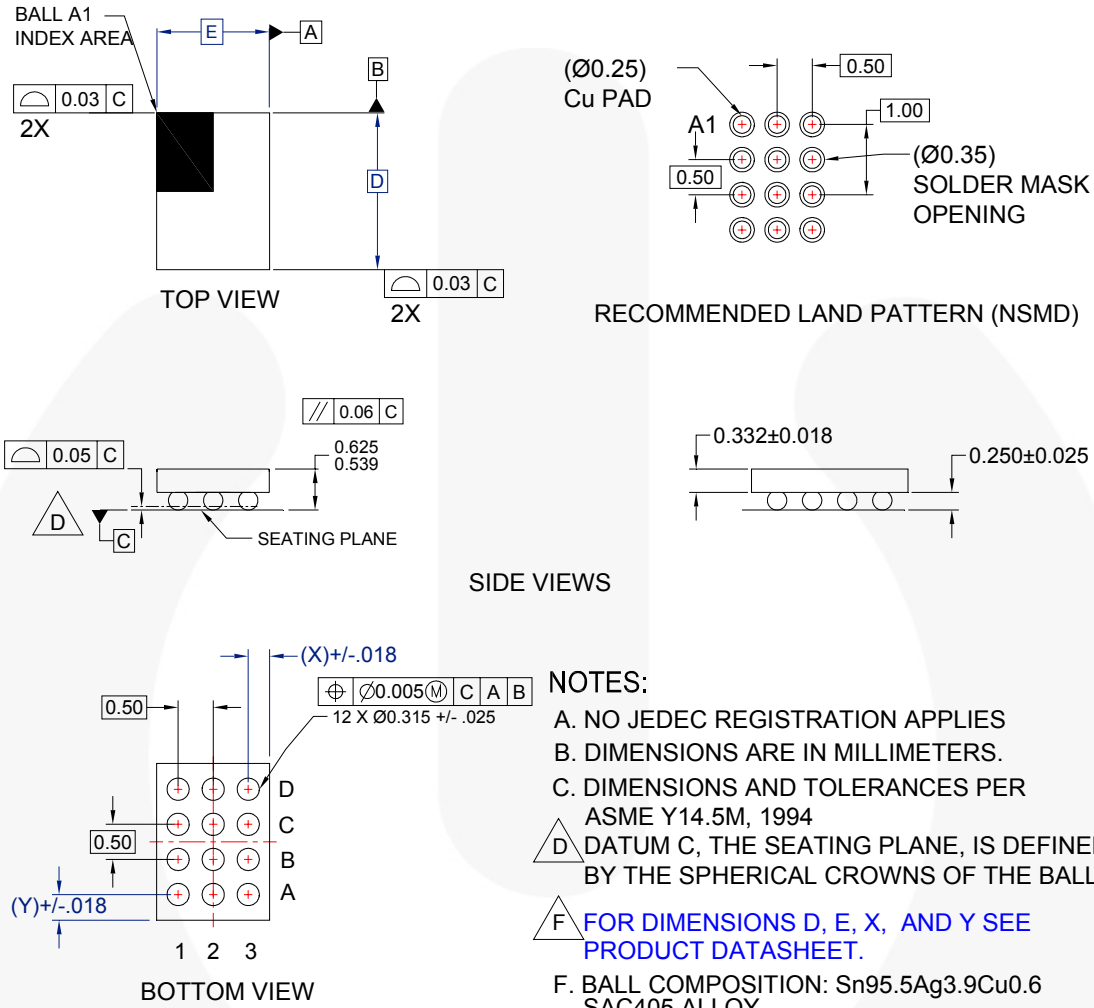


Figure 45. 12-Bump WLCSP, 0.5mm Pitch

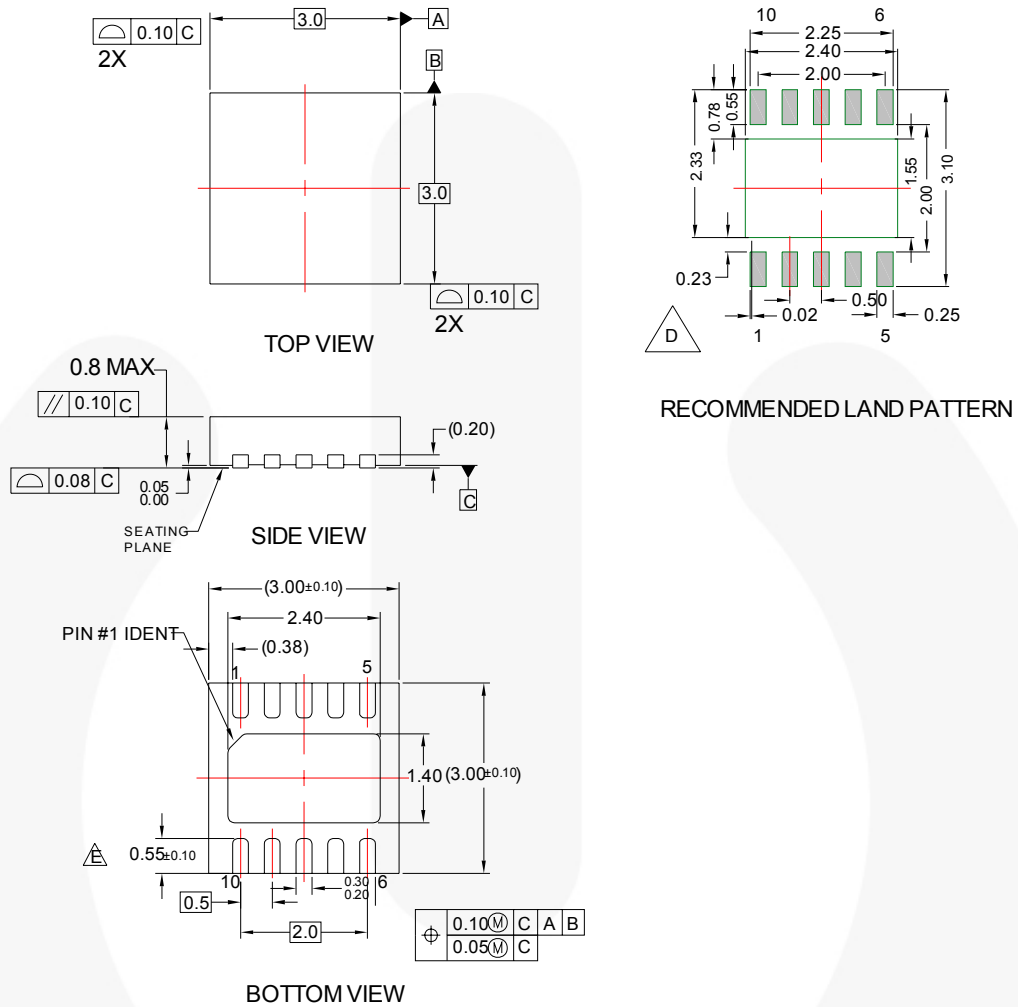
## Product-Specific Dimensions

Product	D	E	X	Y
FAN5355UC	2.230 +/-0.030	1.460 +/-0.030	0.230	0.365

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## Physical Dimensions



### NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION WEED-5 EXCEPT WHERE NOTED
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- △ LAND PATTERN DIMENSIONS ARE NOMINAL REFERENCE VALUES ONLY
- △ NOT COMPLIANT

MLP10ArevB

**Figure 46. 10-pin, 3x3mm Molded Leadless Package (MLP)**

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|  | MICROCOUPLER™          | SMART START™  | µSerDes™  |
|  | MicroFET™              | SPM®  |  |
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| Fairchild Semiconductor®  | MillerDrive™           | SuperFET™   | Ultra FRFET™  |
| FACT Quiet Series™  | MotionMax™             | SuperSOT™-3   | UniFET™   |
| FACT®   | Motion-SPM™            | SuperSOT™-6   | VCX™  |
| FAST®   | OPTOLOGIC®             | SuperSOT™-8   | VisualMax™  |
| FastvCore™  | OPTOPLANAR®            | SupreMOS™   |   |
| FlashWriter® *  |                        | SyncFET™  |   |
|   |                        |  |   |

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