

# 1M x 1 Static RAM

## Features

- High speed
  - $t_{AA} = 15 \text{ ns}$
- CMOS for optimum speed/power
- Automatic power-down when deselected
- TTL-compatible inputs and outputs

## Functional Description

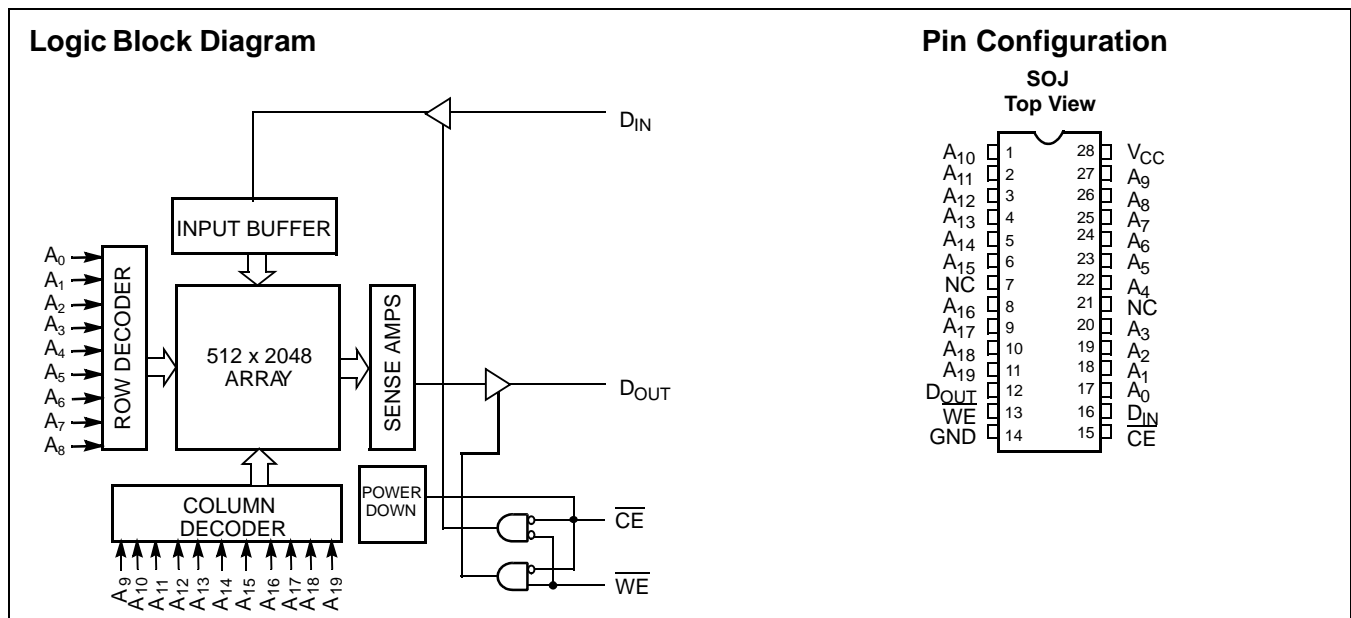
The CY7C107BN and CY7C1007BN are high-performance CMOS static RAMs organized as 1,048,576 words by 1 bit. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ) and three-state drivers. These devices have an automatic power-down feature that reduces power consumption by more than 65% when deselected.

Writing to the devices is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the input pin ( $D_{IN}$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{19}$ ).

Reading from the devices is accomplished by taking Chip Enable ( $\overline{CE}$ ) LOW while Write Enable ( $\overline{WE}$ ) remains HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the data output ( $D_{OUT}$ ) pin.

The output pin ( $D_{OUT}$ ) is placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH) or during a write operation ( $\overline{CE}$  and  $\overline{WE}$  LOW).

The CY7C107BN is available in a standard 400-mil-wide SOJ; the CY7C1007BN is available in a standard 300-mil-wide SOJ



## Selection Guide

	<b>7C107BN-15</b> <b>7C1007BN-15</b>
Maximum Access Time (ns)	15
Maximum Operating Current (mA)	80
Maximum CMOS Standby Current $I_{SB2}$ (mA)	2

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied..... -55°C to +125°C  
 Supply Voltage on  $V_{CC}$  Relative to GND<sup>[1]</sup> ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$   
 DC Input Voltage<sup>[1]</sup>..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current..... >200 mA

### Operating Range

Range	Ambient Temperature <sup>[2]</sup>	$V_{CC}$
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

### Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C107BN-15 7C1007BN-15		Unit
			Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	V
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1	+1	mA
$I_{OZ}$	Output Leakage Current	$GND \leq V_I \leq V_{CC}$ , Output Disabled	-5	+5	mA
$I_{OS}$	Output Short Circuit Current <sup>[3]</sup>	$V_{CC} = \text{Max.}, V_{OUT} = GND$		-300	mA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}$ , $f = f_{MAX} = 1/t_{RC}$		80	mA
$I_{SB1}$	Automatic $\overline{CE}$ Power-Down Current— TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$		20	mA
$I_{SB2}$	Automatic $\overline{CE}$ Power-Down Current — CMOS Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , $f = 0$		2	mA

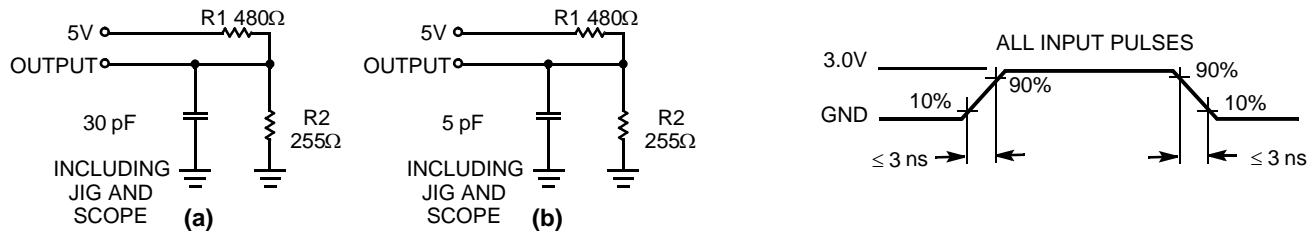
### Capacitance<sup>[4]</sup>

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$ : Addresses	Input Capacitance	$T_A = 25 \times C$ , $f = 1 \text{ MHz}$ , $V_{CC} = 5.0V$	7	pF
$C_{IN}$ : Controls			10	pF
$C_{OUT}$	Output Capacitance		10	pF

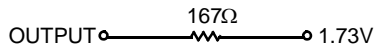
**Notes:**

- $V_{IL}(\text{min.}) = -2.0V$  for pulse durations of less than 20 ns.
- $T_A$  is the "Instant On" case temperature.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



## Switching Characteristics<sup>[5]</sup> Over the Operating Range

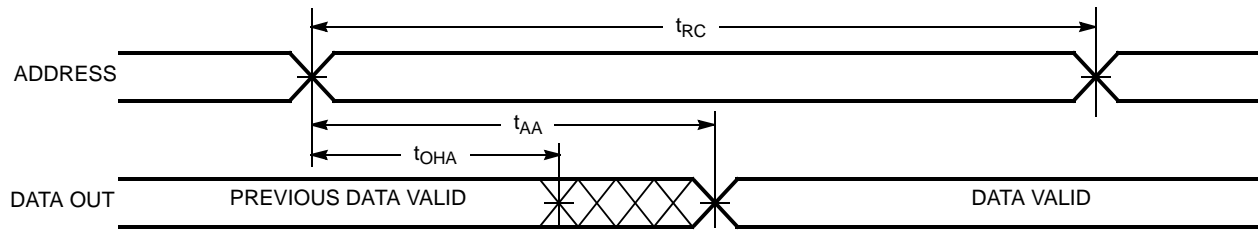
Parameter	Description	7C107BN-15 7C1007BN-15		Unit
		Min.	Max.	
<b>READ CYCLE</b>				
$t_{RC}$	Read Cycle Time	15		ns
$t_{AA}$	Address to Data Valid		15	ns
$t_{OHA}$	Data Hold from Address Change	3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		15	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low $Z^{[6]}$	3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High $Z^{[6, 7]}$		7	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		15	ns
<b>WRITE CYCLE<sup>[8]</sup></b>				
$t_{WC}$	Write Cycle Time	15		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	12		ns
$t_{AW}$	Address Set-Up to Write End	12		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-Up to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	12		ns
$t_{SD}$	Data Set-Up to Write End	8		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low $Z^{[6]}$	3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High $Z^{[6, 7]}$		7	ns

### Notes:

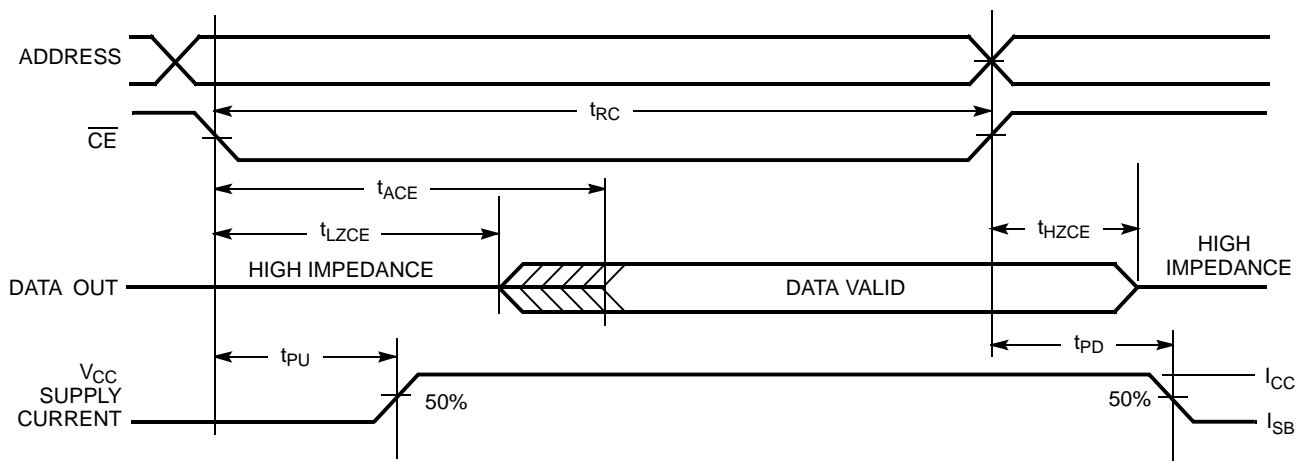
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$  and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZCE}$  and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

## Switching Waveforms

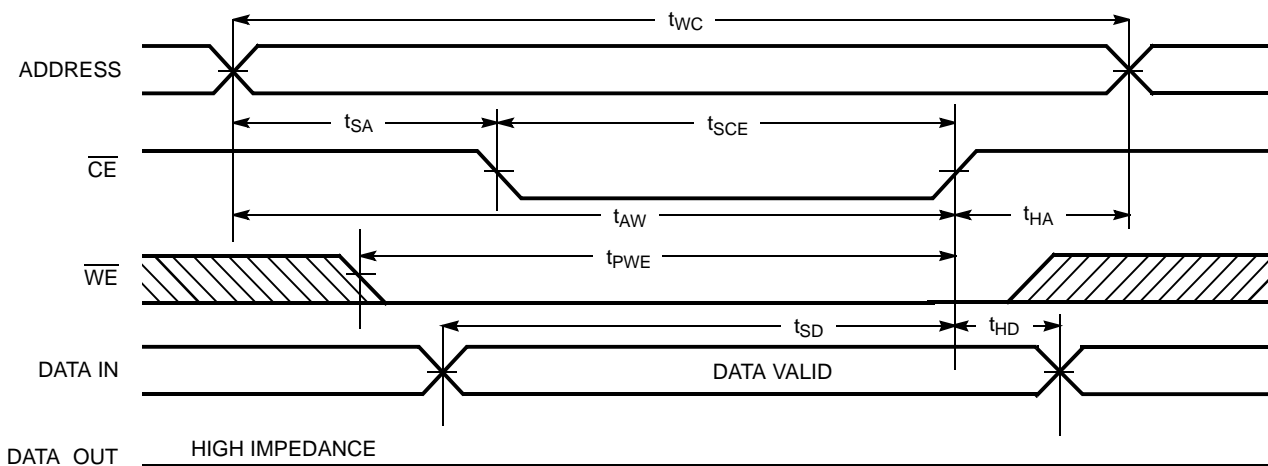
### Read Cycle No. 1<sup>[10, 11]</sup>



### Read Cycle No. 2<sup>[11, 12]</sup>



### Write Cycle No. 1 (CE Controlled)<sup>[13]</sup>

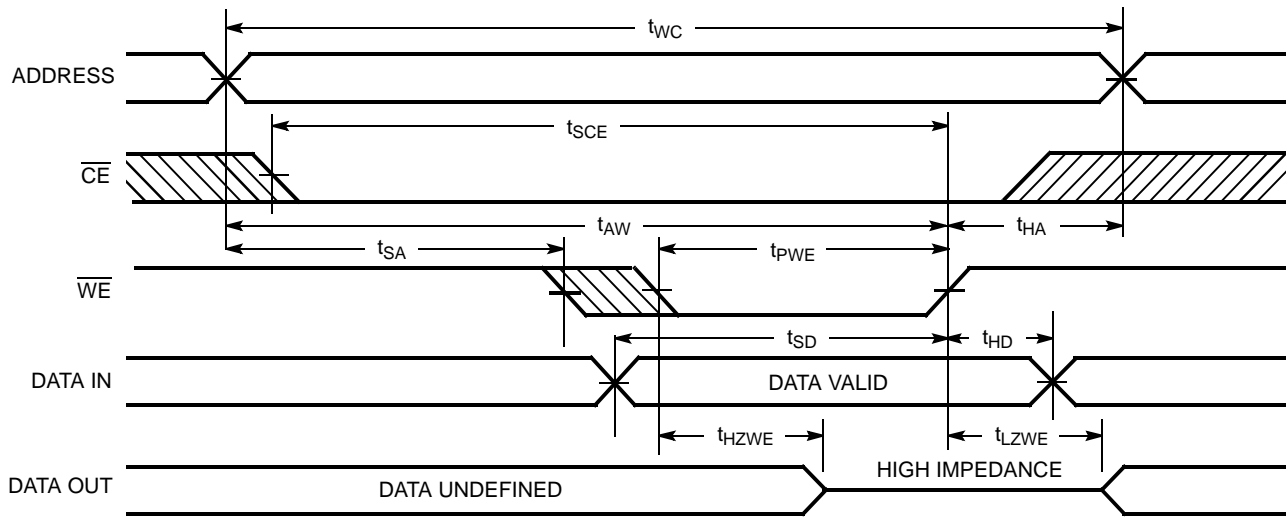


**Notes:**

9. No input may exceed  $V_{CC} + 0.5V$ .
10. Device is continuously selected,  $\overline{CE} = V_{IL}$ .
11. WE is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
13. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

**Switching Waveforms** (continued)

**Write Cycle No. 2 ( $\overline{WE}$  Controlled)<sup>[13]</sup>**



**Truth Table**

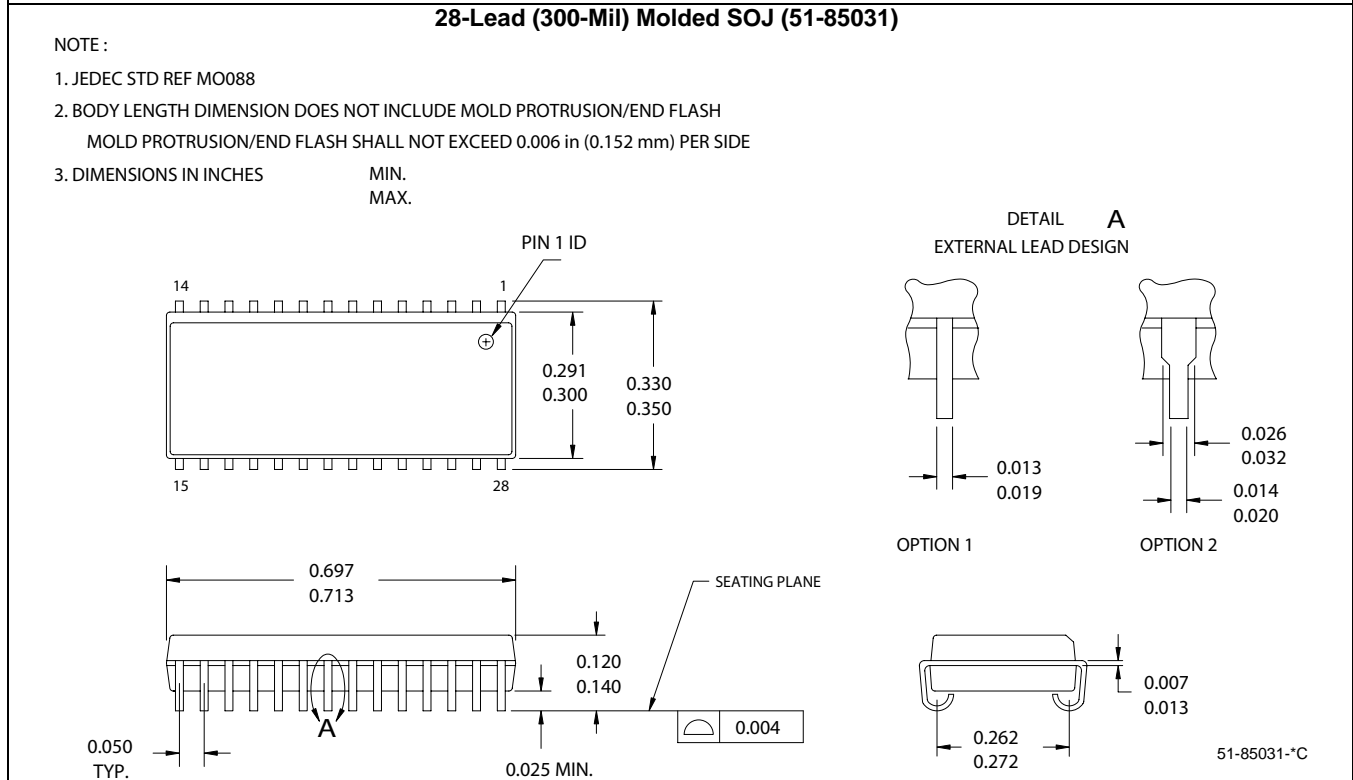
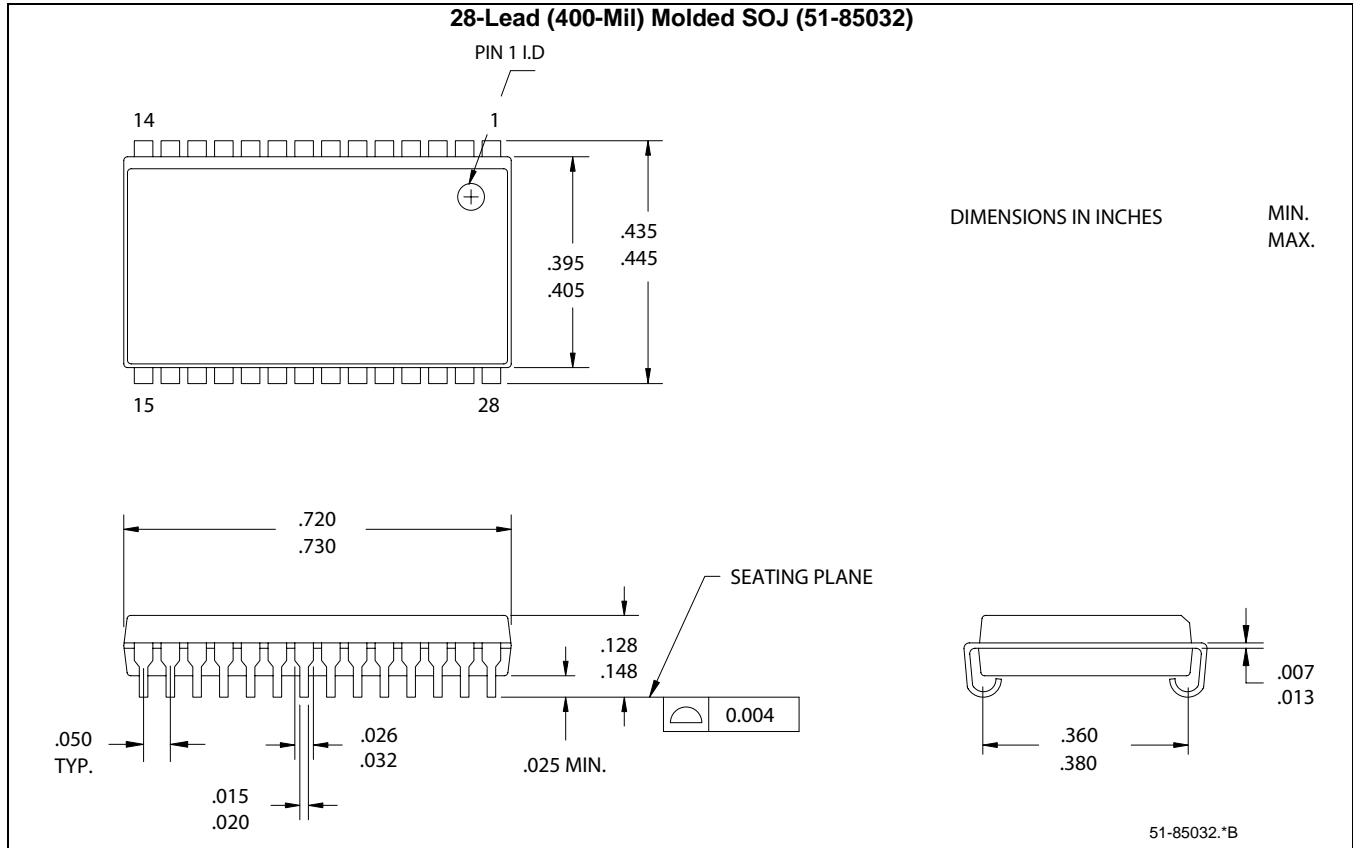
$\overline{CE}$	$\overline{WE}$	D <sub>OUT</sub>	Mode	Power
H	X	High Z	Power-Down	Standby (I <sub>SB</sub> )
L	H	Data Out	Read	Active (I <sub>CC</sub> )
L	L	High Z	Write	Active (I <sub>CC</sub> )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C107BN-15VC	51-85032	28-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1007BN-15VC	51-85031	28-Lead (300-Mil) Molded SOJ	
	CY7C1007BN-15VXC	51-85031	28-Lead (300-Mil) Molded SOJ (Pb-free)	
	CY7C107BN-15VI	51-85032	28-Lead (400-Mil) Molded SOJ	Industrial

Please contact local sales representative regarding availability of these parts

**Package Diagrams**



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## Document History Page

<b>Document Title: CY7C107BN/CY7C1007BN 1M x 1 Static RAM</b> <b>Document Number: 001-06426</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	423847	See ECN	NXR	New Data Sheet