1 MHz to 4 GHz, 80 dB Logarithmic Detector/Controller

ADL5513

Preliminary Technical Data

FEATURES

Wide bandwidth: 1 MHz to 4 GHz
80 dB dynamic range (±3 dB)
Stability over temperature: < ±0.5 dB
Low noise measurement/controller output (VOUT)
Pulse response time: 10 ns
Small footprint package: 3 mm x 3 mm LFCSP
Supply operation: 2.7 to 5.5 V at 30 mA
Fabricated using high speed SiGe process

APPLICATIONS

RF transmitter PA setpoint control and level monitoring
Power monitoring in radiolink transmitters
RSSI measurement in base stations, WLAN, WiMAX, radar

FUNCTIONAL BLOCK DIAGRAM

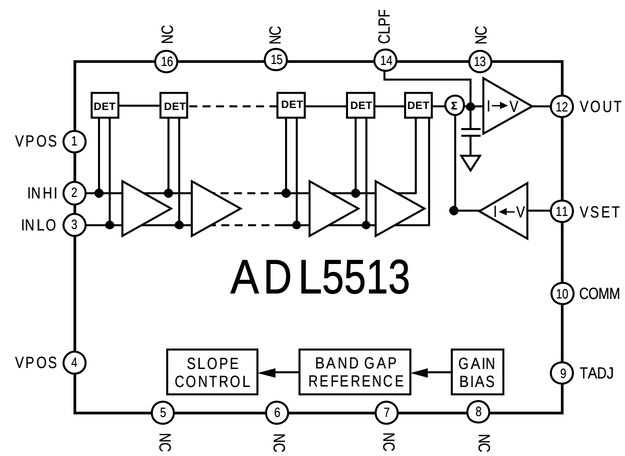

Figure 1.

GENERAL DESCRIPTION

The ADL5513 is a demodulating logarithmic amplifier, capable of accurately converting an RF input signal to a corresponding decibel-scaled output. It employs the progressive compression technique over a cascaded amplifier chain, each stage of which is equipped with a detector cell. The device can be used in either measurement or controller modes. The ADL5513 maintains accurate log conformance for signals greater than 4 GHz. The input dynamic range is typically 80 dB (re: 50 Ω) with error less than ±3 dB. The ADL5513 has 10 ns response time which enables RF burst detection to a pulse rate of beyond 50 MHz. The device provides unprecedented logarithmic intercept stability vs. ambient temperature conditions. A supply of 2.7 V to 5.5 V is required to power the device. Current consumption is less than 30 mA, and decreases to TBD µA when the device is disabled.

The ADL5513 can be configured to provide a control voltage to a power amplifier or a measurement output from the VOUT pin. Because the output can be used for controller applications, special attention has been paid to minimize wideband noise. In this mode, the setpoint control voltage is applied to the VSET pin.

The feedback loop through an RF amplifier is closed via VOUT, the output of which regulates the amplifier's output to a magnitude corresponding to V_{SET}. The ADL5513 provides 0 V to (V_{POS} – 0.1 V) output capability at the VOUT pin, suitable for controller applications. As a measurement device, VOUT is externally connected to VSET to produce an output voltage V_{OUT} that increases linear-in-dB with RF input signal amplitude.

The logarithmic slope is 20 mV/dB, determined by the VSET interface. The intercept is -95 dBm (re: 50 Ω, CW input, 900 MHz) using the INHI input. These parameters are very stable against supply and temperature variations.

Rev. PrA 6/08

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REVISION HISTORY

SPECIFICATIONS

V_S = 5 V, T = 25°C, Z_O = 50 Ω, Pins INHI, INLO, ac-coupled , Single-ended drive, VOUT tied to VSET, Error referred to best-fit line (linear regression), unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Maximum Input Frequency		0.001		4	GHz
100 MHz					
Output Voltage: High Power in	P_{IN} = -10 dBm,		1.578		V
Output Voltage: Low Power in	P_{IN} = -60 dBm		0.589		V
±3.0 dB Dynamic Range	CW input, T_A = +25°C		75		dB
±1.0 dB Dynamic Range	CW input, T_A = +25°C		67		dB
±0.5 dB Dynamic Range	CW input, T_A = +25°		58		dB
Maximum Input Level, ±1.0 dB			9		
Minimum Input Level, ±1.0 dB			-66		
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; P_{IN} = -10 dBm		±0.421		dB
	-40°C < T_A < +85°C; P_{IN} = –30 dBm		±0.467		dB
	-40°C < T_A < +85°C; P_{IN} = -50 dBm		±0.496		dB
	-40°C < T_A < +125°C; P_{IN} = -10 dBm		±0.63		dB
	-40°C < T_A < +125°C; P_{IN} = – 30 dBm		±0.696		dB
	-40°C < T_A < +125°C; P_{IN} = -50 dBm		±0.0.556		dB
Logarithmic Slope			21		mV/dB
Logarithmic Intercept			-88.18		dBm
Input Impedance			1500/TBD		Ω/pF
900 MHz					
Output Voltage: High Power in	P_{IN} = -10 dBm,		1.59		V
Output Voltage: Low Power in	P_{IN} = -60 dBm		0.59		V
±3.0 dB Dynamic Range	CW input, T_A = +25°C		78		dB
±1.0 dB Dynamic Range	CW input, T_A = +25°C		71		dB
±0.5 dB Dynamic Range	CW input, T_A = +25°		68		dB
Maximum Input Level, ±1.0 dB			8		
Minimum Input Level, ±1.0 dB			-68		
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; P_{IN} = -10 dBm		±0.45		dB
	-40°C < T_A < +85°C; P_{IN} = –30 dBm		±0.40		dB
	-40°C < T_A < +85°C; P_{IN} = -50 dBm		±0.515		dB
	-40°C < T_A < +125°C; P_{IN} = -10 dBm		±0.525		dB
	-40°C < T_A < +125°C; P_{IN} = – 30 dBm		±0.62		dB
	-40°C < T_A < +125°C; P_{IN} = -50 dBm		±0.67		dB
Logarithmic Slope			21		mV/dB
Logarithmic Intercept			-89.07		dBm
Input Impedance			1500/TBD		Ω/pF

Parameter	Conditions	Min	Typ	Max	Unit
1900 MHz					
Output Voltage: High Power in	P_{IN} = -10 dBm		1.61		V
Output Voltage: Low Power in	P_{IN} = -60 dBm		0.6		V
±3.0 dB Dynamic Range	CW input, T_A = +25°C		78		dB
±1.0 dB Dynamic Range	CW input, T_A = +25°C		71		dB
±0.5 dB Dynamic Range	CW input, T_A = +25°		68		dB
Maximum Input Level, ±1.0 dB			7		
Minimum Input Level, ±1.0 dB			-64		
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; P_{IN} = -10 dBm		±0.46		dB
	-40°C < T_A < +85°C; P_{IN} = −30 dBm		±0.515		dB
	-40°C < T_A < +85°C; P_{IN} = -50 dBm		±0.66		dB
	-40°C < T_A < +125°C; P_{IN} = -10 dBm		±0.41		dB
	-40°C < T_A < +125°C; P_{IN} = − 30 dBm		±0.73		dB
	-40°C < T_A < +125°C; P_{IN} = -50 dBm		±0.785		dB
Logarithmic Slope			21		mV/dB
Logarithmic Intercept			-89.87		dBm
Input Impedance			1500/TBD		Ω/pF
2140 MHz					
Output Voltage: High Power in	P_{IN} = -10 dBm,		1.61		V
Output Voltage: Low Power in	P_{IN} = -60 dBm		0.61		V
±3.0 dB Dynamic Range	CW input, T_A = +25°C		78		dB
±1.0 dB Dynamic Range	CW input, T_A = +25°C		70		dB
±0.5 dB Dynamic Range	CW input, T_A = +25°		66		dB
Maximum Input Level, ±1.0 dB			7		
Minimum Input Level, ±1.0 dB			-63		
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; P_{IN} = -10 dBm		±0.43		dB
	-40°C < T_A < +85°C; P_{IN} = −30 dBm		±0.497		dB
	-40°C < T_A < +85°C; P_{IN} = -50 dBm		±0.598		dB
	-40°C < T_A < +125°C; P_{IN} = -10 dBm		±0.635		dB
	-40°C < T_A < +125°C; P_{IN} = − 30 dBm		±0.727		dB
	-40°C < T_A < +125°C; P_{IN} = -50 dBm		±0.676		dB
Logarithmic Slope			21		mV/dB
Logarithmic Intercept			-90.01		dBm
Input Impedance			1500/TBD		Ω/pF
2600 MHz					
Output Voltage: High Power in	P_{IN} = -10 dBm,		1.62		V
Output Voltage: Low Power in	P_{IN} = -60 dBm		0.61		V
±3.0 dB Dynamic Range	CW input, T_A = +25°C		80		dB
±1.0 dB Dynamic Range	CW input, T_A = +25°C		74		dB
±0.5 dB Dynamic Range	CW input, T_A = +25°		72		dB
Maximum Input Level, ±1.0 dB			7		
Minimum Input Level, ±1.0 dB			-60		
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; P_{IN} = -10 dBm		±0.47		dB
	-40°C < T_A < +85°C; P_{IN} = −30 dBm		±0.605		dB
	-40°C < T_A < +85°C; P_{IN} = -50 dBm		±0.715		dB
	-40°C < T_A < +125°C; P_{IN} = -10 dBm		±0.575		dB
	-40°C < T_A < +125°C; P_{IN} = − 30 dBm		±0.8		dB
	-40°C < T_A < +125°C; P_{IN} = -50 dBm		±0.853		dB
Logarithmic Slope			21		mV/dB
Logarithmic Intercept			-90.56		dBm
Input Impedance			1500/TBD		Ω/pF

Parameter	Conditions	Min	Typ	Max	Unit
3.6 GHz					
Output Voltage: High Power in	P_{IN} = -10 dBm,		1.6		V
Output Voltage: Low Power in	P_{IN} = -60 dBm		0.6		V
±3.0 dB Dynamic Range	CW input, T_A = +25°C		78		dB
±1.0 dB Dynamic Range	CW input, T_A = +25°C		71		dB
±0.5 dB Dynamic Range	CW input, T_A = +25°		66		dB
Maximum Input Level, ±1.0 dB			5		
Minimum Input Level, ±1.0 dB			-66		
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; P_{IN} = -10 dBm		±0.64		dB
	-40°C < T_A < +85°C; P_{IN} = –30 dBm		±0.64		dB
	-40°C < T_A < +85°C; P_{IN} = -50 dBm		±0.62		dB
	-40°C < T_A < +125°C; P_{IN} = -10 dBm		±0.856		dB
	-40°C < T_A < +125°C; P_{IN} = – 30 dBm		±0.926		dB
	-40°C < T_A < +125°C; P_{IN} = -50 dBm		±0.937		dB
Logarithmic Slope			21		mV/dB
Logarithmic Intercept			-90.57		dBm
Input Impedance			TBD		Ω/pF
SETPOINT INPUT	Pin VSET				
Voltage Range	Log conformance error ≤1 dB Min		TBD		V
	Log conformance error ≤1 dB Max		TBD		
Current Limit Source/Sink	1% change		TBD		mA
OUTPUT INTERFACE					
Rise Time	Input level = no signal to –10dBm, 10% to 90% C_{LPF} = 10 pF		10		nS
Fall Time	Input level = no signal to –10dBm, 10% to 90% C_{LPF} = 10 pF		20		nS
POWER SUPPLY INTERFACE	Pin VPOS				
Supply Voltage		2.7	5	5.5	V
Quiescent Current	25C RF in =-55 dBm		30		mA
Supply Current	When disabled		TBD		µA
POWER-DOWN INTERFACE	Pin PWDN				
Logic Level Threshold	Logic LO enables Logic HI disables		VPOS – 0.7 V		V
Enable Time	PWDN LO to OUT at 100% final value, C_{LPF} = 10pF, RF in = –10 dBm		143		ns
Disable Time	PWDN HI to OUT at 10% final value, C_{LPF} = 10pF, RF in = –10 dBm		100		ns

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage: V_{POS}	5.5V
V_{SET} Voltage	0 V to VPOS
Input Power (Single-Ended, Re: 50 Ω)	TBD dBm
Internal Power Dissipation	TBD W
θ_{JA}	TBD°C/W
Maximum Junction Temperature	TBD°C
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

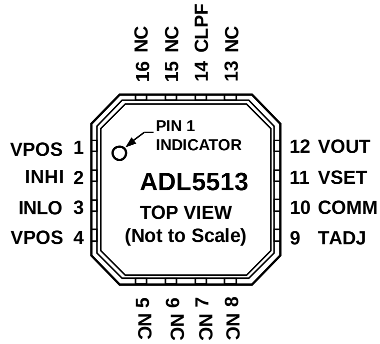

Figure 2.

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4	VPOS	Positive supply Voltage (VPOS), 2.7 V to 5.5 V
2	INHI	RF input. AC –coupled RF input.
3	INLO	RF common for INHI. AC- coupled RF common.
10	COMM	Device Common.
9	TADJ	Temperature Compensation Adjustment. Frequency Dependant Temperature Compensation is set by connecting a ground referenced resistor to this pin.
11	VSET	Setpoint Input for Operation in Controller Mode. To operate in RSSI mode short VSET to VOUT.
12	VOUT	Logarithmic/ Error Output.
5, 6, 7, 8, 13, 15, 16	NC	No Connect. These pins may be left open or soldered to a low impedance ground plane.
14	CLPF	Loop Filter Capacitor. In measurement mode, this capacitor sets the pulse response time and video bandwidth. In controller mode, the capacitance on this node sets the response time of the error amplifier/integrator.
	Exposed Paddle	Internally connected to COMM; solder to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{POS} = 5 V; T_A = +25°C, −40°C, +85°C; +125°C, unless otherwise noted. Black: +25°C, Blue: −40°C; Red: +85°C, Orange: +125°C. Error is calculated by using the best-fit line between P_{IN} = −40 dBm and P_{IN} = −10 dBm at the specified input frequency, unless otherwise noted.

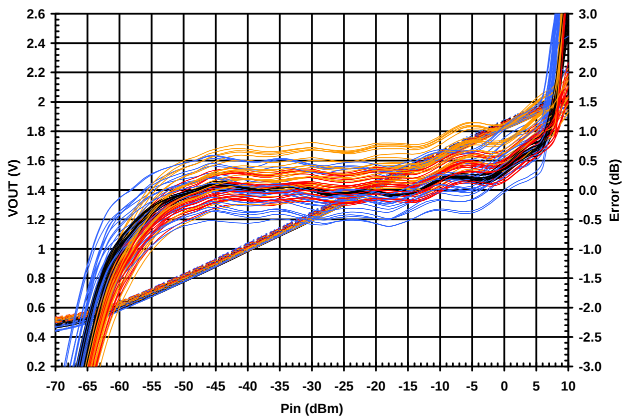

Figure 3 V_{OUT} and Log Conformance vs. Input Amplitude at 100 MHz, Multiple Devices, V_{TADJ} = 1.0 V

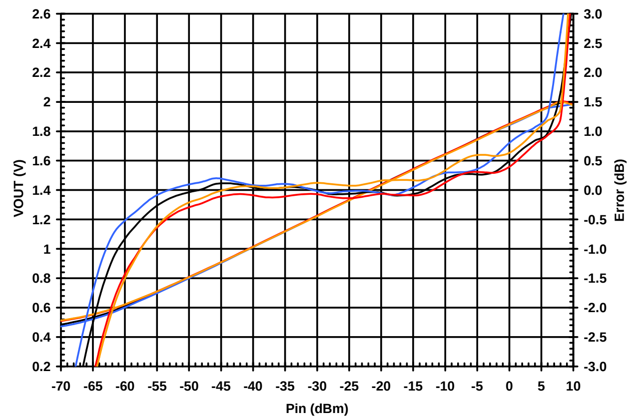

Figure 6 V_{OUT} and Log Conformance vs. Input Amplitude at 100 MHz, V_{TADJ} = 1.0 V

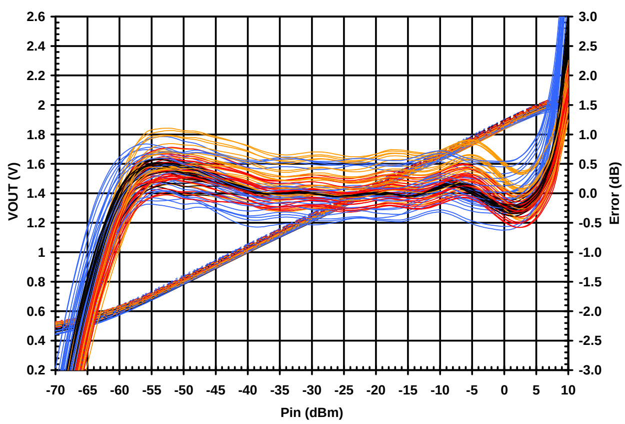

Figure 4 V_{OUT} and Log Conformance vs. Input Amplitude at 900 MHz, Multiple Devices, V_{TADJ} = 0.975 V

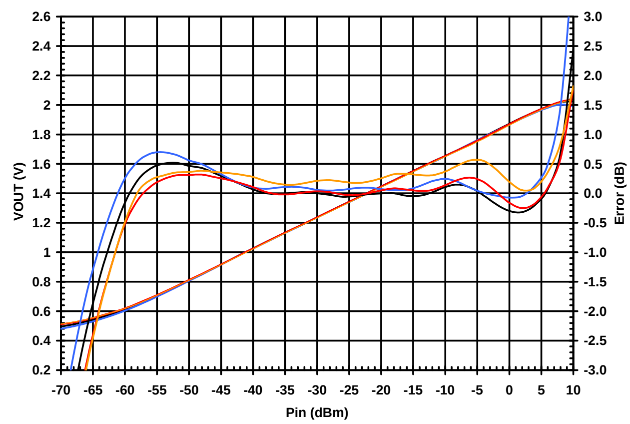

Figure 7 V_{OUT} and Log Conformance vs. Input Amplitude at 900 MHz, V_{TADJ} = 0.975 V

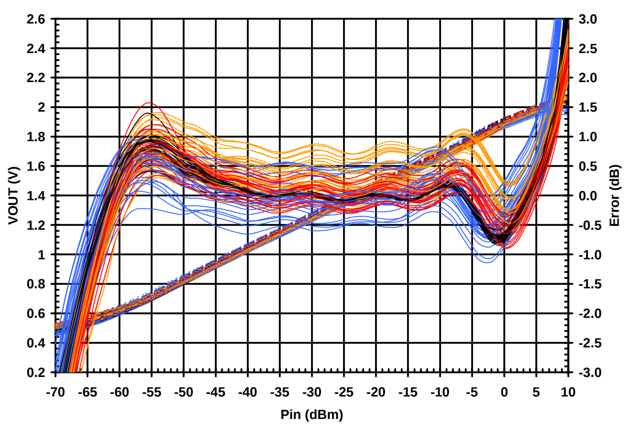

Figure 5 V_{OUT} and Log Conformance vs. Input Amplitude at 1900 MHz, Multiple Devices, V_{TADJ} = 0.925 V

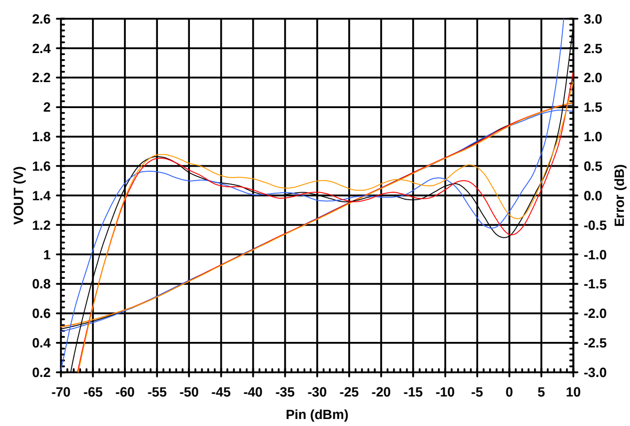

Figure 8. V_{OUT} and Log Conformance vs. Input Amplitude at 1900 MHz, V_{TADJ} = 0.925 V

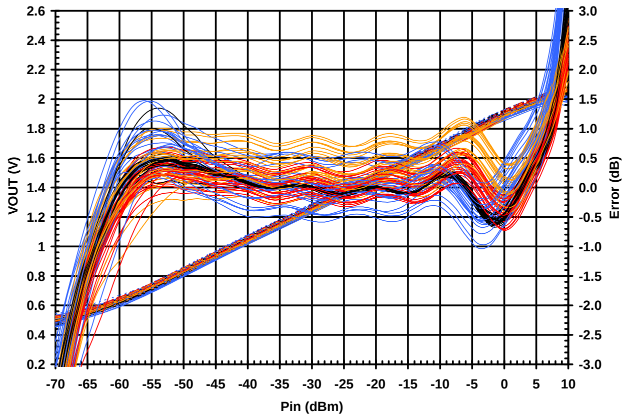

Figure 9. V_{OUT} and Log Conformance vs. Input Amplitude at 2140 MHz, Multiple Devices, V_{TADJ} = 0.925 V

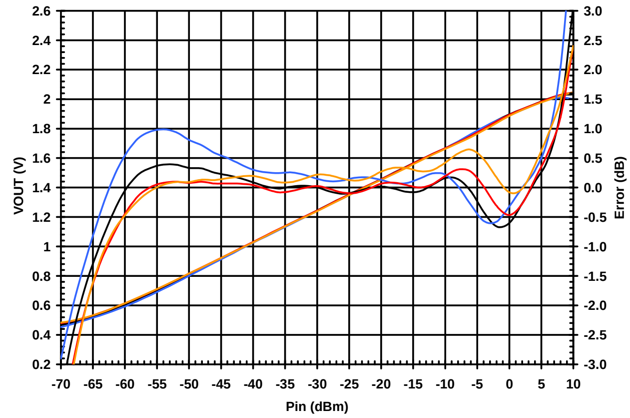

Figure 12. V_{OUT} and Log Conformance vs. Input Amplitude at 2140 MHz, V_{TADJ} = 0.925 V

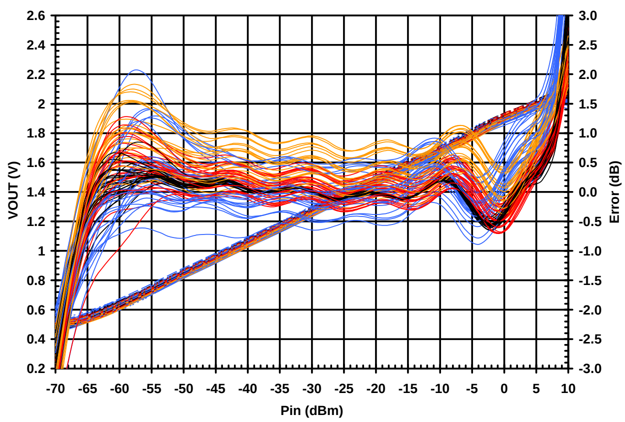

Figure 10. V_{OUT} and Log Conformance vs. Input Amplitude at 2600 MHz, Multiple Devices, V_{TADJ} = 0.9 V

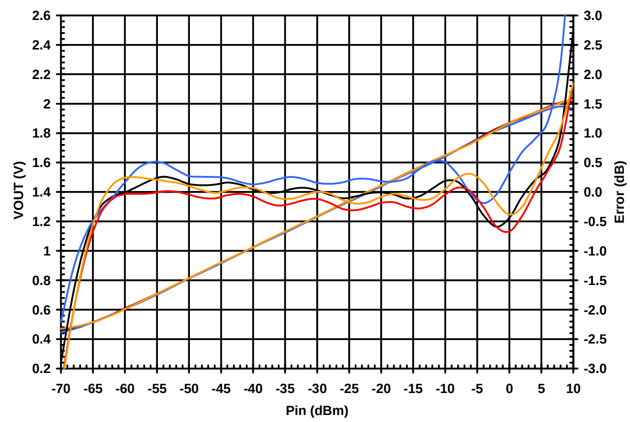

Figure 13. V_{OUT} and Log Conformance vs. Input Amplitude at 2600 MHz, V_{TADJ} = 0.9 V

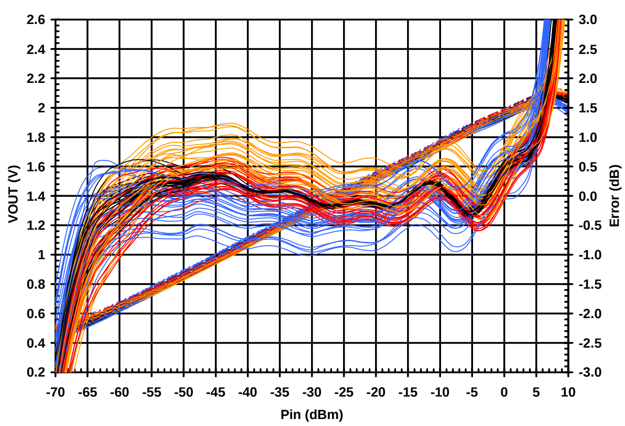

Figure 11. V_{OUT} and Log Conformance vs. Input Amplitude at 3600 MHz, Multiple Devices, V_{TADJ} = 0.9 V

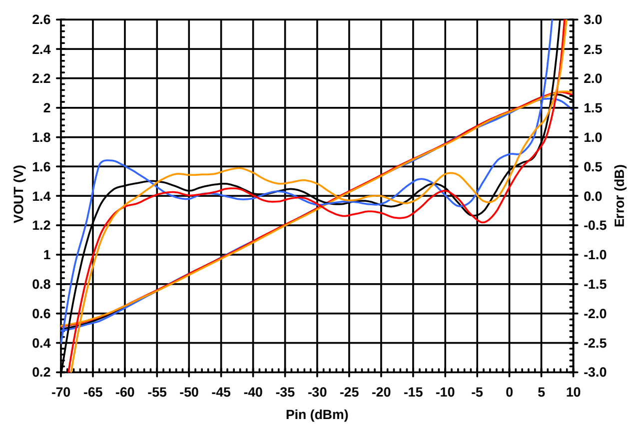

Figure 14. V_{OUT} and Log Conformance vs. Input Amplitude at 3600 MHz, V_{TADJ} = 0.9 V

EVALUATION BOARD CONFIGURATION OPTIONS

Table 4. Evaluation Board Configuration Options

Component	Function	Default Value
C1, C2, R1	Input Interface. The 52.3 Ω resistor in Position R1 combines with the internal input impedance of the ADL5513 to give a broadband input impedance of about 50 Ω. C1 and C2 are dc-blocking capacitors. A reactive impedance match can be implemented by replacing R1 with an inductor and C1 and C2 with appropriately valued capacitors.	R1 = 52.3 Ω (Size 0402) C1 = 47 nF (Size 0402) C2 = 47 nF (Size 0402)
C3, C4, C5, C6, R11, R12	Power Supply Decoupling The nominal supply decoupling consists of a 100 pF filter capacitor placed physically close to the ADL5513 and a 0.1 μF capacitor placed nearer to the power supply input pin. If additional isolation from the power supply is required, a small resistance maybe installed in between the power supply and the ADL5513. (R11, R12)	C3 = 0.1 μF (Size 0402) C4 = 100 pF (Size 0402) C5 = 100 pF (Size 0402) C6 = 0.1 μF (Size 0402) R11 = 0 Ω (Size 0402) R12 = 0 Ω (Size 0402)
C7	Filter Capacitor The low-pass corner frequency of the circuit that drives the VOUT pin can be lowered by placing a capacitor between CLPF and ground. Increasing this capacitor increases the overall rise/fall time of the ADL5513 for pulsed input signals.	C7= 1000 pF (Size 0402)
R2, R3 R4, R5, R10, RL, CL	Output Interface—Measurement Mode. In measurement mode, a portion of the output voltage is fed back to the VSET pin via R4. The magnitude of the slope of the VOUT output voltage response can be increased by reducing the portion of V_{OUT} that is fed back to VSET. R3 can be used as a back-terminating resistor or as part of a single-pole, low-pass filter.	R2 = open (Size 0402) R3 = 1 kΩ (Size 0402) R4 = 0 Ω (Size 0402) R5 = open (Size 0402) R10 = open (Size 0402) RL = CL = open (Size 0402)
R4, R5, R10	Output Interface—Controller Mode. In this mode, R4 must be open. In controller mode, the ADL5513 can control the gain of an external component. A setpoint voltage is applied to Pin VSET, the value of which corresponds to the desired RF input signal level applied to the ADL5513 RF input. A sample of the RF output signal from this variable gain component is selected, typically via a directional coupler, and applied to ADL5513 RF input. The voltage at the VOUT pin is applied to the gain control of the variable gain element. A control voltage is applied to the VSET pin. The magnitude of the control voltage can optionally be attenuated via the voltage divider comprising R4 and R5, or a capacitor can be installed in Position R5 to form a low-pass filter along with R4.	R4 = open (Size 0402) R5 = open (Size 0402) R10 = 0 Ω (Size 0402)
R6, R7, R8, R9	Temperature Compensation Interface. A voltage source can be used to optimize the temperature performance for various input frequencies. The pads for R8/R9 can be used for a voltage divider from the VPOS node to set the T_{ADJ} voltage at different frequencies. The ADL5513 may be disabled by by applying a voltage of V_{POS} −0.7 V to this node.	R6 = open (Size 0402) R7= 0 Ω (Size 0402) R8 = open (Size 0402) R9 = open Ω (Size 0402)
VPOS, GND	Supply and Ground Connections	Not Applicable

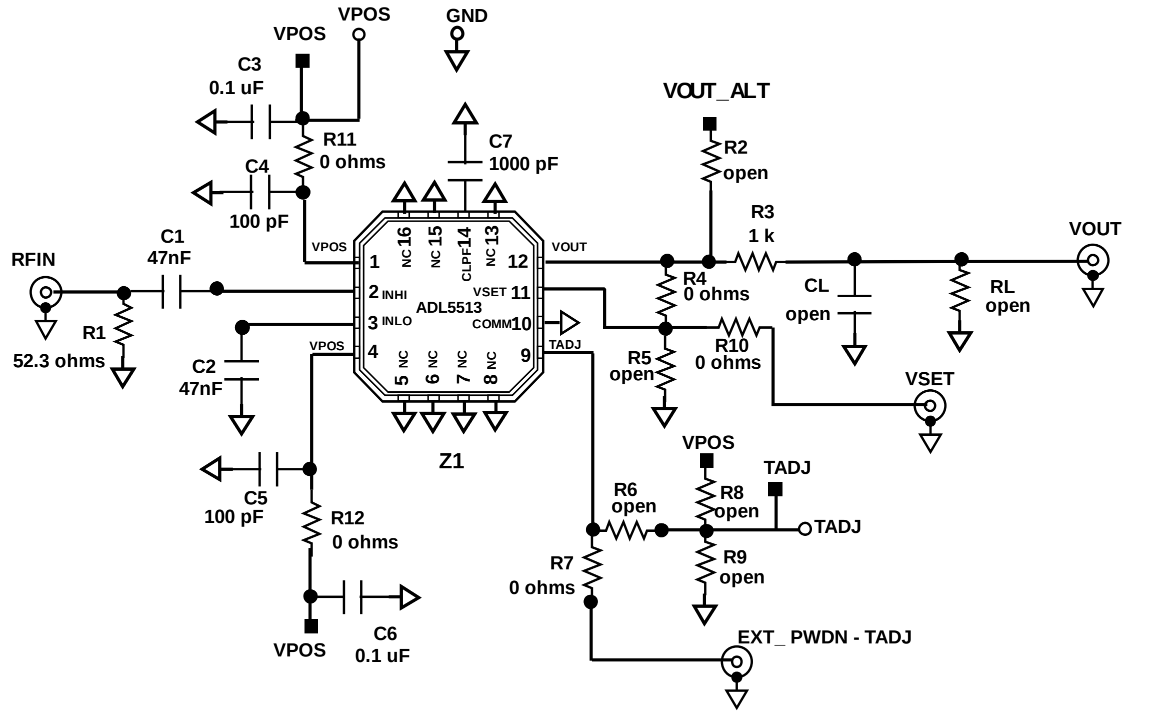

Figure 15. Evaluation Board Schematic

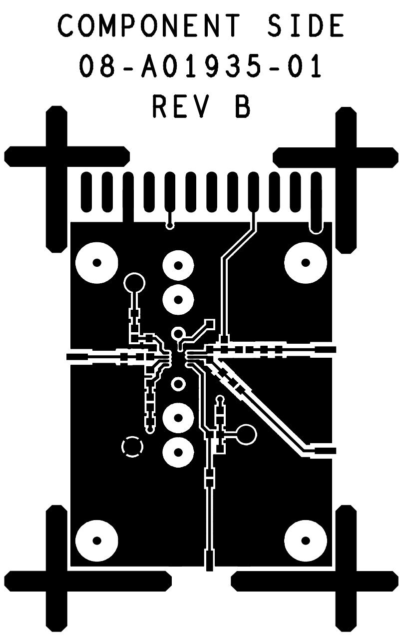

Figure 16.Component Side Layout

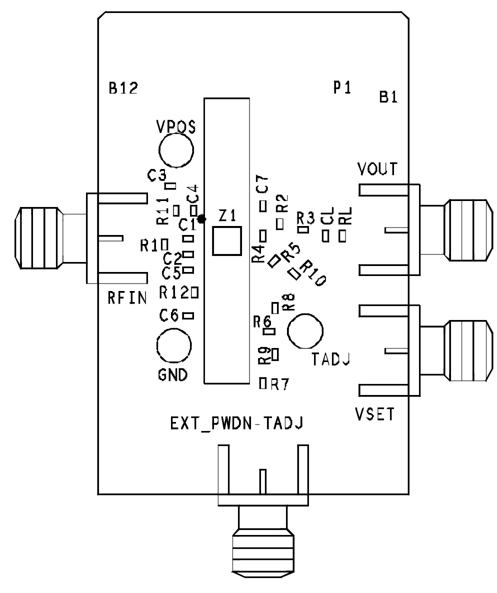

Figure 17. Component Side Silkscreen

OUTLINE DIMENSIONS

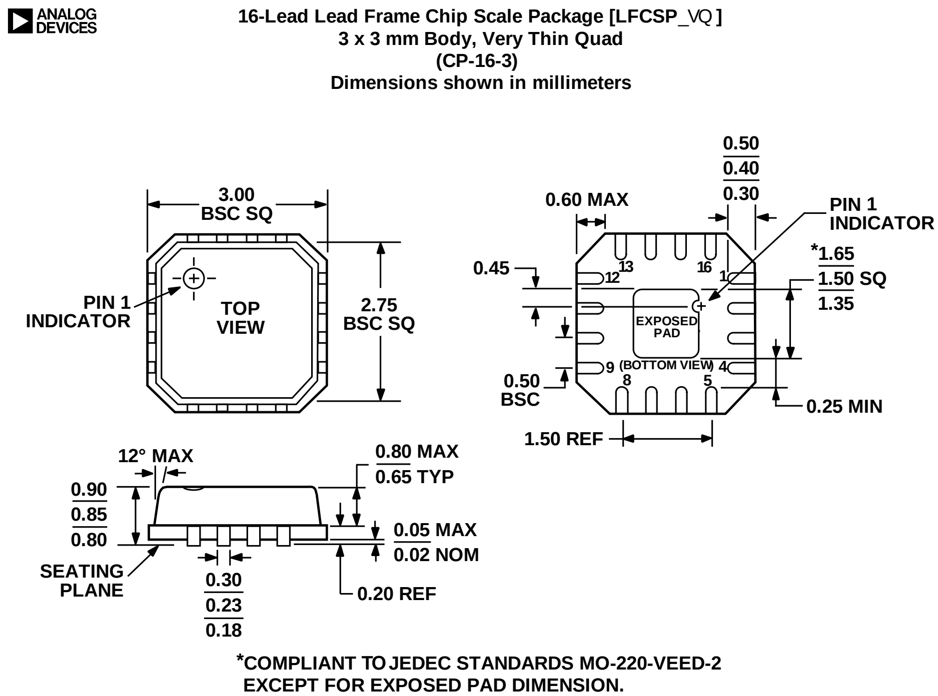

Figure 18. -Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-16-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADL5513-ACPZ-R7[1]	−40°C to +125°C	16-Lead LFCSP_VQ, Reel	CP-16-3	TBD
ADL5513-ACPZ-R2[1]	−40°C to +125°C	16-Lead LFCSP_VQ, Reel	CP-16-3	TBD
ADL5513-ACPZ-WP[1 2]	−40°C to +125°C	16-Lead LFCSP_VQ, Waffle Pack	CP-16-3	TBD
ADL5513-EVALZ[1]		Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] WP = waffle pack

PR07514-0-6/08(PrA)