

FDFMA3N109

Integrated N-Channel PowerTrench® MOSFET and Schottky Diode

General Description

This device is designed specifically as a single package solution for a boost topology in cellular handset and other ultra-portable applications. It features a MOSFET with low input capacitance, total gate charge and on-state resistance, and an independently connected schottky diode with low forward voltage and reverse leakage current to maximize boost efficiency.

The MicroFET 2x2 package offers exceptional thermal performance for its physical size and is well suited to switching and linear mode applications.

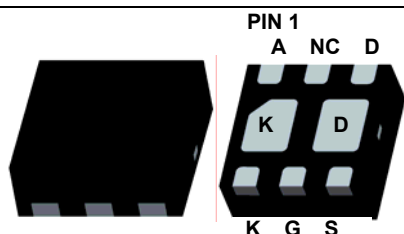
Features

MOSFET:

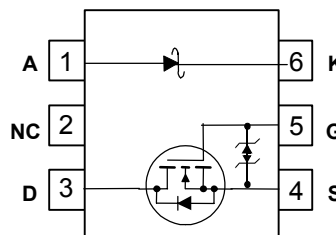
- 2.9 A, 30 V $R_{DS(ON)} = 123 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
- $R_{DS(ON)} = 140 \text{ m}\Omega @ V_{GS} = 3.0 \text{ V}$
- $R_{DS(ON)} = 163 \text{ m}\Omega @ V_{GS} = 2.5 \text{ V}$

Schottky:

- $V_F < 0.46 \text{ V @ } 500\text{mA}$
- Low profile – 0.8 mm maximum – in the new package MicroFET 2x2 mm
- HBM ESD protection level = 1.8kV typical (Note 3)
- RoHS Compliant



MicroFET 2x2



Absolute Maximum Ratings

$T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 4.5\text{V}$)	2.9	A
	– Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 2.5\text{V}$)	2.7	
	– Pulsed	10	
P_D	Power Dissipation for Single Operation (Note 1a)	1.5	W
	Power Dissipation for Single Operation (Note 1b)	0.65	
T_J, T_{STG}	Operating and Storage Temperature	-55 to $+150$	$^\circ\text{C}$
V_{RRM}	Schottky Repetitive Peak Reverse Voltage	28	V
I_o	Schottky Average Forward Current	1	A

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	83	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	193	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1c)	101	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1d)	228	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
109	FDFMA3N109	7"	8mm	3000 units

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		25		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate–Body Leakage Current	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.4	1.0	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		-3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 2.9\text{ A}$		75	123	m Ω
		$V_{GS} = 3.0\text{ V}, I_D = 2.7\text{ A}$		84	140	
		$V_{GS} = 2.5\text{ V}, I_D = 2.5\text{ A}$		92	163	
		$V_{GS} = 4.5\text{ V}, I_D = 2.9\text{ A}, T_C = 85^\circ\text{C}$		95	166	
		$V_{GS} = 3.0\text{ V}, I_D = 2.7\text{ A}, T_C = 150^\circ\text{C}$		138	203	
		$V_{GS} = 2.5\text{ V}, I_D = 2.5\text{ A}, T_C = 150^\circ\text{C}$		150	268	

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		190	220	pF
C_{oss}	Output Capacitance			30	40	pF
C_{rss}	Reverse Transfer Capacitance			20	30	pF
R_G	Gate Resistance	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		4.6		Ω

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		6	12	ns
t_r	Turn–On Rise Time			8	16	ns
$t_{d(off)}$	Turn–Off Delay Time			12	21	ns
t_f	Turn–Off Fall Time			2	4	ns
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 2.9\text{ A},$ $V_{GS} = 4.5\text{ V}$		2.4	3.0	nC
Q_{gs}	Gate–Source Charge			0.35		nC
Q_{gd}	Gate–Drain Charge			0.75		nC

Drain–Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain–Source Diode Forward Current			2.9		A
V_{SD}	Drain–Source Diode Forward Voltage	$I_S = 2.0\text{ A}$		0.9	1.2	V
		$I_S = 1.1\text{ A}$		0.8	1.2	
t_{rr}	Diode Reverse Recovery Time	$I_F = 2.9\text{ A},$		10		ns
Q_{rr}	Diode Reverse Recovery Charge	$di_F/dt = 100\text{ A}/\mu\text{s}$		2		nC

Schottky Diode Characteristics

I_R	Reverse Leakage	$V_R = 28\text{ V}$	$T_J = 25^\circ\text{C}$	10	100	μA
			$T_J = 85^\circ\text{C}$	0.07	4.7	mA
V_F	Forward Voltage	$I_F = 1\text{ A}$	$T_J = 25^\circ\text{C}$	0.50	0.57	V
			$T_J = 85^\circ\text{C}$	0.49	0.60	
V_F	Forward Voltage	$I_F = 500\text{ mA}$	$T_J = 25^\circ\text{C}$	0.40	0.46	V
			$T_J = 85^\circ\text{C}$	0.36	0.43	

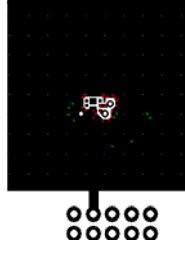
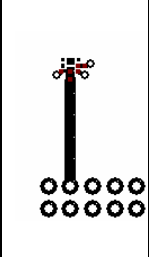
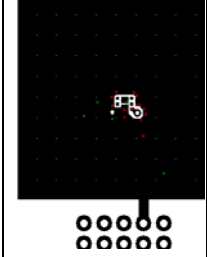
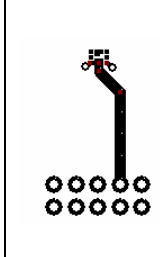
Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

- (a) MOSFET $R_{\theta JA} = 83^\circ\text{C/W}$ when mounted on a 1in² pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB
- (b) MOSFET $R_{\theta JA} = 193^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper
- (c) Schottky $R_{\theta JA} = 101^\circ\text{C/W}$ when mounted on a 1in² pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB
- (d) Schottky $R_{\theta JA} = 228^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper

	<p>a) 83°C/W when mounted on a 1in² pad of 2 oz copper</p>		<p>b) 193°C/W when mounted on a minimum pad of 2 oz copper</p>		<p>c) 101°C/W when mounted on a 1in² pad of 2 oz copper</p>		<p>d) 228°C/W when mounted on a minimum pad of 2 oz copper</p>
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Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

3: The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics

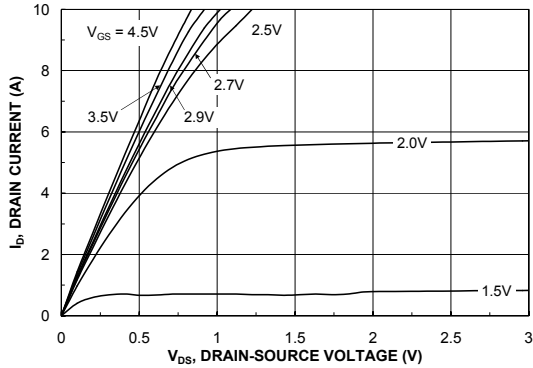


Figure 1. On-Region Characteristics.

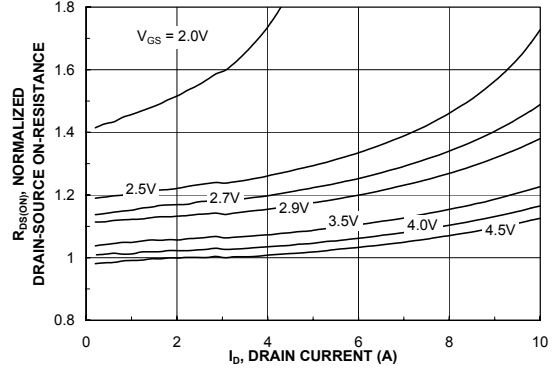


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

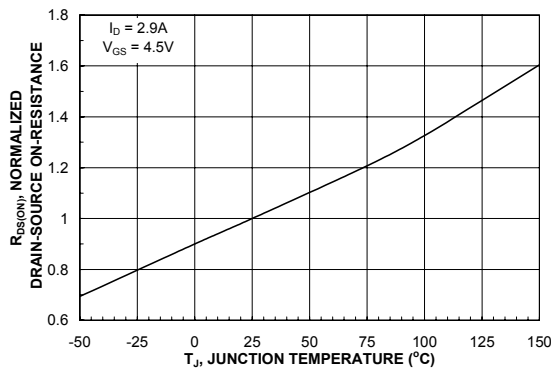


Figure 3. On-Resistance Variation with Temperature.

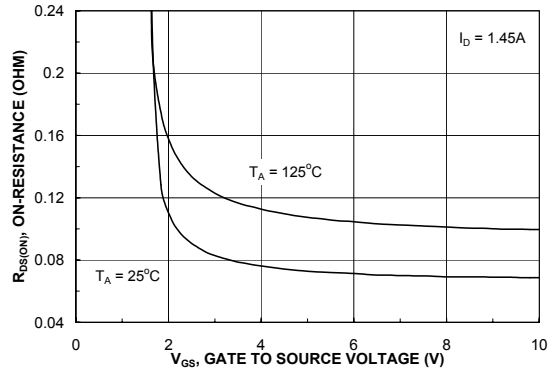


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

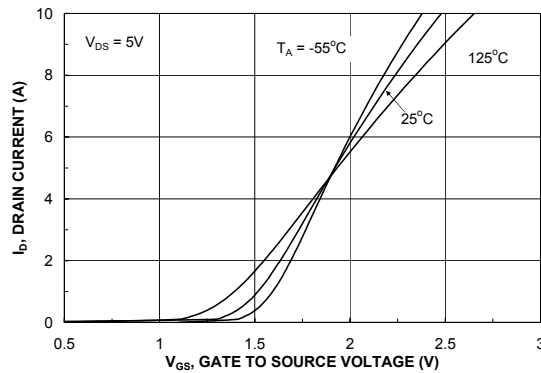


Figure 5. Transfer Characteristics.

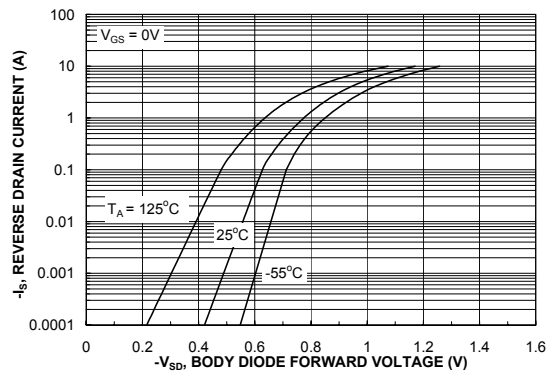


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

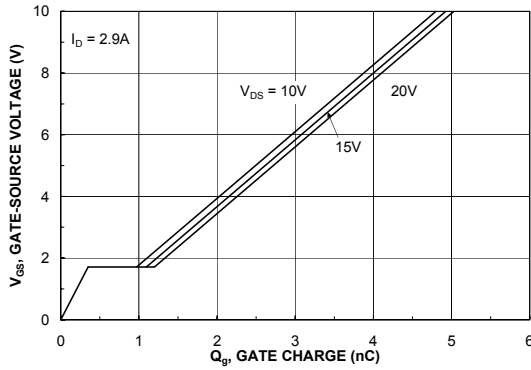


Figure 7. Gate Charge Characteristics.

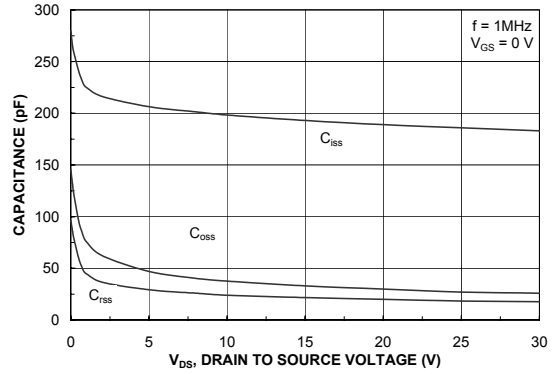


Figure 8. Capacitance Characteristics.

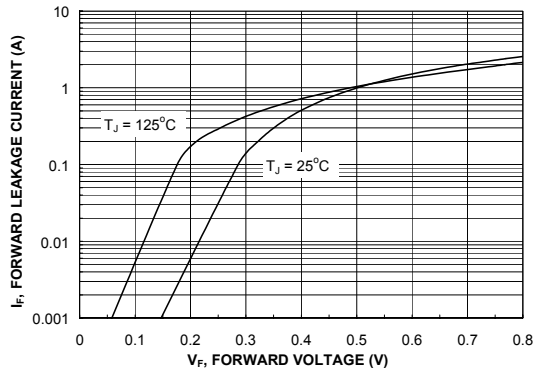


Figure 9. Schottky Diode Forward Voltage.

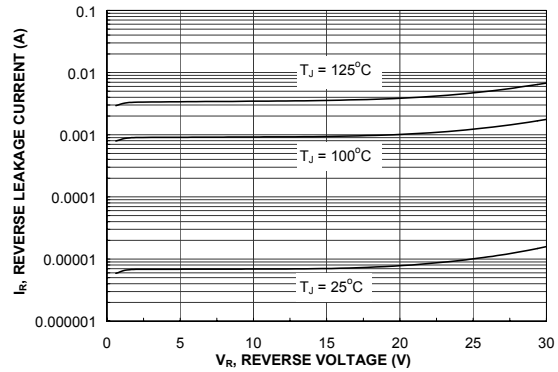


Figure 10. Schottky Diode Reverse Current.

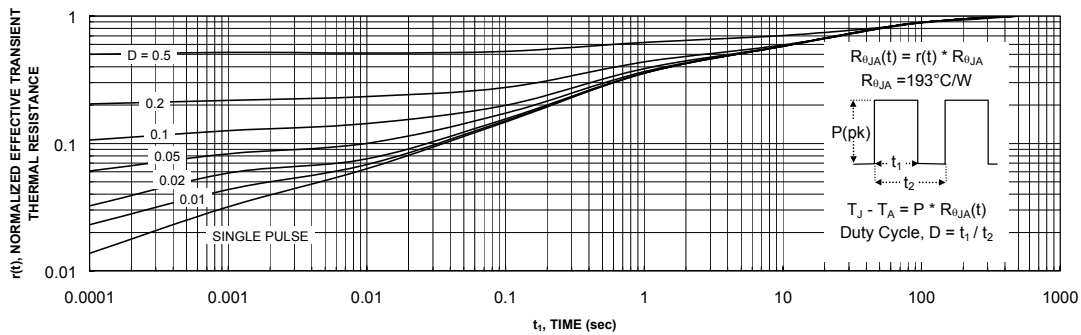
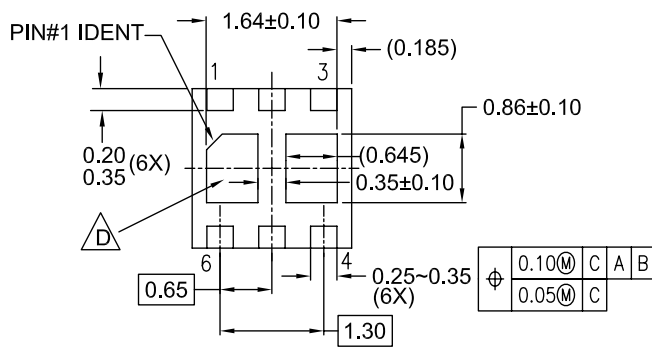
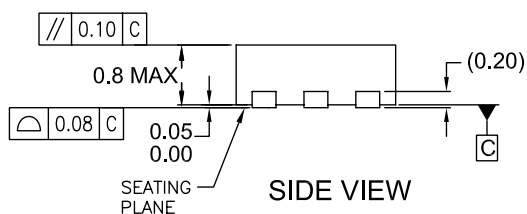
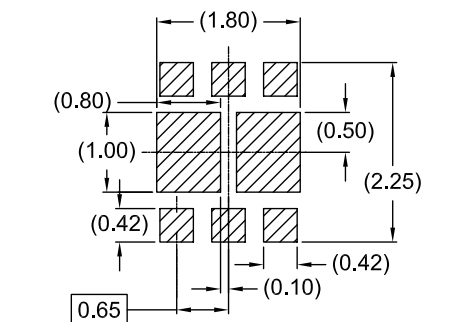
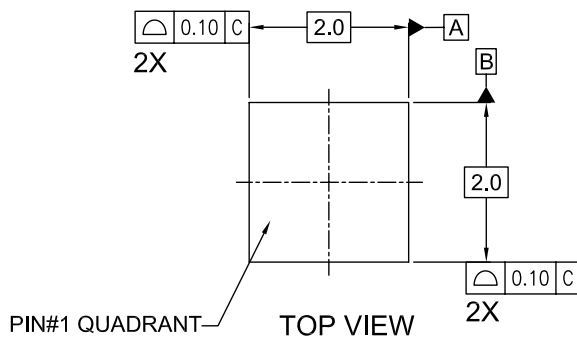


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout








NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION VCCC EXCEPT AS NOTED.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. NON-JEDEC DUAL DAP
- E. DRAWING FILE NAME : MLP06J rev3



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