2 Mbit (256K x 8)
5V Only CMOS Flash Memory

1. FEATURES

- Single supply voltage 5V ±10%
- Fast access time: 70/90 ns
- Compatible with JEDEC standard
  - Pin-out, packages and software commands compatible with single-power supply Flash
- Low power consumption
  - 25mA maximum active current
  - 25uA typical standby current
- 100,000 program/erase cycles typically
- Command register architecture
  - Byte programming (10us typical)
  - Sector Erase(sector structure: 16KB, 8KB, 8KB, 96KB, 128KB)
- Auto Erase (chip & sector) and Auto Program
  - Sector erase and Chip erase.
  - Automatically program and verify data at specified address

- End of program or erase detection
  - Data polling
  - Toggle bits
- Boot Sector Architecture
  - U = Upper Boot Sector
- Packages available:
  - 32-pin PDIP
  - 32-pin PLCC

2. ORDERING INFORMATION

Part No	Boot	Speed	Package	Part No	Boot	Speed	Package
F49B002UA-70D	Upper	70 ns	PDIP	F49B002UA-90D	Upper	90 ns	PDIP
F49B002UA-70N	Upper	70 ns	PLCC	F49B002UA-90N	Upper	90 ns	PLCC

3. GENERAL DESCRIPTION

The F49B002UA is a 2 Megabit, 5V only CMOS Flash memory device organized as 256K bytes of 8 bits. This device is packaged in standard 32-pin PDIP and 32-pin PLCC. It is designed to be programmed and erased both in system and can in standard EPROM programmers.

With access times of 70 ns and 90 ns, the F49B002UA allows the operation of high-speed microprocessors. The device has separate chip enable $\overline{CE}$, write enable $\overline{WE}$, and output enable $\overline{OE}$ controls. EFST's memory devices reliably store memory data even after 10,000 program and erase cycles.

The F49B002UA is entirely pin and command set compatible with the JEDEC standard for 2 Megabit Flash memory devices. Commands are written to the command register using standard microprocessor write timings.

The F49B002UA features a sector erase architecture. The device memory array is divided into 16 Kbytes, 8K bytes, 8Kbytes, 96Kbytes, 128Kbytes. Erase capabilities provide the flexibility to revise the data in the device.

A low V_{CC} detector inhibits write operations on loss of power. End of program or erase is detected by the Data Polling of DQ7, or by the Toggle Bit feature on DQ6. Once the program or erase cycle has been successfully completed, the device internally resets to the Read mode.

4. PIN CONFIGURATIONS

4.1   32-pin PDIP

```
              ┌─────────────┐
      N C  ┤ 1  ◯    ⌣   32 ├ V DD
      A16  ┤ 2           31 ├ W̄Ē
      A15  ┤ 3           30 ├ A17
      A12  ┤ 4           29 ├ A14
       A7  ┤ 5           28 ├ A13
       A6  ┤ 6           27 ├ A8
       A5  ┤ 7           26 ├ A9
       A4  ┤ 8  32-Pin  25 ├ A11
       A3  ┤ 9   DIP     24 ├ ŌĒ
       A2  ┤ 10          23 ├ A10
       A1  ┤ 11          22 ├ C̄Ē
       A0  ┤ 12          21 ├ DQ7
      DQ0  ┤ 13          20 ├ DQ6
      DQ1  ┤ 14          19 ├ DQ5
      DQ2  ┤ 15          18 ├ DQ4
      GND  ┤ 16          17 ├ DQ3
              └─────────────┘
```

4.2   32-pin PLCC

```
           A12 A15 A16 NC Vcc W̄Ē A17
            4   3   2   1  32  31  30
       A7 ┤ 5                     29 ├ A14
       A6 ┤ 6           ◯         28 ├ A13
       A5 ┤ 7                     27 ├ A8
       A4 ┤ 8                     26 ├ A9
       A3 ┤ 9                     25 ├ A11
       A2 ┤ 10                    24 ├ ŌĒ
       A1 ┤ 11                    23 ├ A10
       A0 ┤ 12                    22 ├ C̄Ē
      DQ0 ┤ 13                    21 ├ DQ7
            14  15  16  17 18  19  20
           DQ1 DQ2 GND DQ3 DQ4 DQ5 DQ6
```
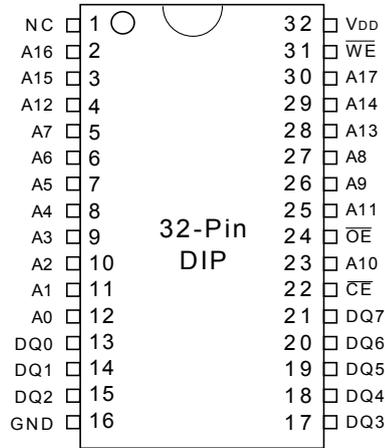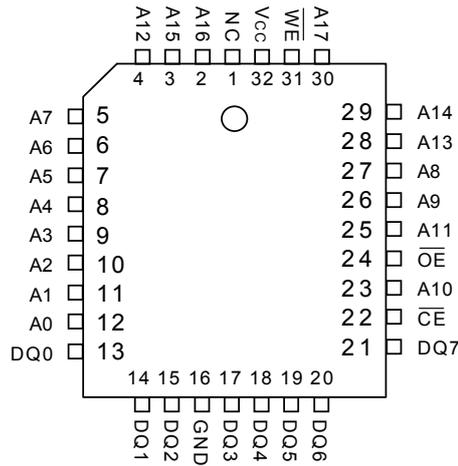
4.3 Pin Description

Symbol	Pin Name	Functions
A0~A17	Address Input	To provide memory addresses.
DQ0~DQ7	Data Input/Output	To output data when Read and receive data when Write. The outputs are in tri-state when $\overline{OE}$ or $\overline{CE}$ is high.
$\overline{CE}$	Chip Enable	To activate the device when $\overline{CE}$ is low.
$\overline{OE}$	Output Enable	To gate the data output buffers.
$\overline{WE}$	Write Enable	To control the Write operations.
NC	No connection	Unconnected pin
V_{CC}	Power Supply	To provide power
GND	Ground	

5. SECTOR STRUCTURE

Table 1: F49B002UA Sector Address Table

Sector	Sector Size (Kbytes)	Address range	Sector Address				
			A17	A16	A15	A14	A13
SA4	16	3C000H-3FFFFH	1	1	1	1	X
SA3	8	3A000H-3BFFFH	1	1	1	0	1
SA2	8	38000H-39FFFH	1	1	1	0	0
SA1	96	20000H-37FFFH	1	X	X	X	X
SA0	128	00000H-1FFFFH	0	X	X	X	X

6. FUNCTIONAL BLOCK DIAGRAM
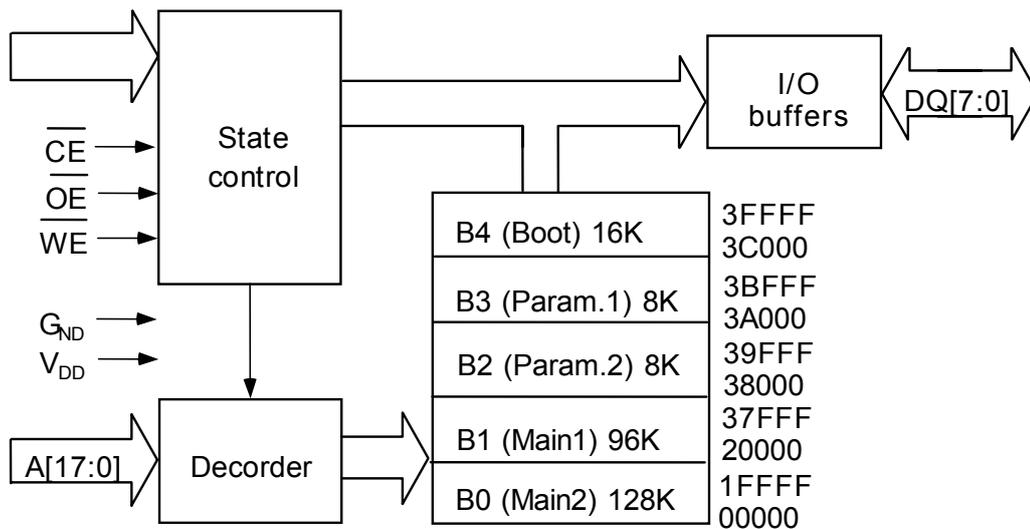
7. FUNCTIONAL DESCRIPTION

7.1 Device operation

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The register is composed of latches that store the command, address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The F49B002UA features various bus operations as Table 2.

Table 2. F49B002UA Operation Modes Selection

DESCRIPTION	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A17 | A13	A12 | A10	A9	A8 | A7	A6	A5 | A2	A1	A0	DQ0~DQ7
				ADDRESS								
Read	L	L	H	AIN								Dout
Write	L	H	L	AIN								DIN
Output Disable	L	H	H	X								High Z
Standby	H	X	X	X								High Z
Auto-select	See Table 3											

Notes:

1. L= Logic Low = V_{IL}, H= Logic High = V_{IH}, X= Don't Care, SA= Sector Address, AIN= Address In, DIN = Data In, Dout = Data Out.

Table 3. F49B002UA Auto-Select Mode (High Voltage Method)

DESCRIPTION	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A17 | A13	A12 | A10	A9	A8 | A4	A6	A3	A2	A1	A0	DQ0~DQ7
				ADDRESS									
(Manufacturer ID:EFST)	L	L	H	X	X	V_{ID}	X	X	L	H	L	L	7FH
	L	L	H	X	X	V_{ID}	X	X	H	L	L	L	7FH
	L	L	H	X	X	V_{ID}	X	X	H	H	L	L	7FH
	L	L	H	X	X	V_{ID}	X	X	L	L	L	L	8CH
(Device ID: F49B002UA)	L	L	H	X	X	V_{ID}	X	X	L	L	L	H	00H

Notes :

1. Manufacturer and device codes may also be accessed via the software command sequence in Table 4.
2. V_{ID}=11.5V to 12.5V.

Read Mode

To read array data from the outputs, the system must drive the $\overline{CE}$ and $\overline{OE}$ pins to V_{IL}. $\overline{CE}$ is the power control and selects the device. $\overline{OE}$ is the output control and gates array data to the output pins. $\overline{WE}$ should remain at V_{IH}. The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition.

No command is necessary in this mode to obtain array data. Standard microprocessor's read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Read Command" section for more information. Refer to the AC Read Operations Table 9 for timing specifications and to Figure 5 for the timing diagram. I_{CC1} in the DC Characteristics Table 8 represents the active current specification for reading array data.

Write Mode

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive $\overline{WE}$ and $\overline{CE}$ to V_{IL}, and $\overline{OE}$ to V_{IH}. The "Program Command" section has details on programming data to the device using standard command sequences.

An erase operation can erase one sector, or the entire device. Table 1 indicate the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Software Command Definitions" section has details on erasing a sector or the entire chip.

When the system writes the auto-select command sequence, the device enters the auto-select mode. The system can then read auto-select codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the Auto-select Mode and Auto-select Command sections for more information. I_{CC2} in the DC Characteristics Table 8 represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification Table 10 and timing diagrams for write operations.

Resetting the device

The reset command returns the device to Read mode. This is a necessary step after reading the device or manufacturer ID. Note: In these cases, if VID is removed from the A9 pin, the device automatically returns to Read mode and an explicit is not required.

Boot block looking

To keep any system kernel code secure in the boot block, the F49B002UA provides a command to lock the boot block and prevent any accidental erasure or reprogramming. The command sequence is similar to the chip erase sequence except for the last cycle, where 40H must be written into DQ0~DQ7 instead of 10H. The boot block is the only block that can be locked in this way.

Whether or not the boot block has been locked can be detected by the command sequence shown in Table 4. This command sequence returns a "1" on DQ0 if the boot block is locked; a "0" if the boot block has not been locked and it is open to erasing and programming.

Output Disable Mode

With the $\overline{OE}$ is at a logic high level (V_{IH}), outputs from the devices are disabled. This will cause the output pins in a high impedance state

Standby Mode

When $\overline{CE}$ held at $V_{CC} \pm 0.3V$, the device enter CMOS Standby mode. If $\overline{CE}$ held at V_{IH}, but not within the range of $V_{CC} \pm 0.3V$, the device will still be in the standby mode, but the standby current will be larger.

If the device is deselected during auto algorithm of erasure or programming, the device draws active current I_{CC2} until the operation is completed. I_{CC3} in the DC Characteristics Table 8 represents the standby current specification.

The device requires standard access time (t_{CE}) for read access from either of these standby modes, before it is ready to read data.

Auto-select Mode

The auto-select mode provides manufacturer and device identification and sector protection verification, through outputs on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the auto-select codes can also be accessed in-system through the command register.

When using programming equipment, this mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. While address pins A3, A2, A1, and A0 must be as shown in Table 3.

To verify sector protection, all necessary pins have to be set as required in Table 3, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the auto-select codes in-system, the host system can issue the auto-select command via the command register, as shown in Table 4. This method does not require V_{ID}. See " Software Command Definitions" for details on using the auto-select mode.

7.2 Software Command Definitions

Writing specific address and data commands or sequences into the command register initiates the device operations. Table 4 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data.

All addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later. All data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Refer to the corresponding timing diagrams in the AC Characteristics section.

Table 4. F49B002UA Software Command Definitions

Command	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (4)	1	RA	RD	-	-	-	-	-	-	-	-	-	-
Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Boot block lock	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	40H
Reset 1(5)	1	XXXH	F0H	-	-	-	-	-	-	-	-	-	-
Reset 2(5)	3	5555H	AAH	2AAAH	55H	5555H	F0H	-	-	-	-	-	-
Auto-select		See Table 5.											

Notes:

1.   X = don't care
    RA = Address of memory location to be read.
    RD = Data to be read at location RA.
    PA = Address of memory location to be programmed.
    PD = Data to be programmed at location PA.
    SA = Address of the sector.
2. Except Read command and Auto-select command, all command bus cycles are write operations.
3. Address bits A17–A16 are don't cares.
4. No command cycles required when reading array data.
5. The two Reset command sequences have exactly the same effect, two are provided to meet the requirements of difference companies and a range of applications.

Table 5. F49B002UA Auto-Select Command

Command	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Manufacture ID	4	5555H	AAH	2AAAH	55H	5555H	90H	XX04H	7FH	-	-	-	-
	4	5555H	AAH	2AAAH	55H	5555H	90H	XX08H	7FH	-	-	-	-
	4	5555H	AAH	2AAAH	55H	5555H	90H	XX0CH	7FH	-	-	-	-
	4	5555H	AAH	2AAAH	55H	5555H	90H	XX00H	8CH	-	-	-	-
Device ID, Upper boot	4	5555H	AAH	2AAAH	55H	5555H	90H	XX01H	00H	-	-	-	-

Notes :

1. The fourth cycle of the auto-select command sequence is a read cycle.

Read Command

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

See the "Read Mode" in the "Read Operations" section for more information. Refer to AC Read Operation Table 9. & Figure 5 for the timing diagram.

Program Command

The program command sequence programs one byte into the device. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 and DQ6. See "Write Operation Status" section for more information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. The Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit can't be programmed from a "0" back to a "1". Attempting to do so may halt the operation or cause the Data Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

Chip Erase Command

Chip erase is a six-bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm.

The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase.

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a hardware reset during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure the data integrity.

The system can determine the status of the erase operation by using DQ7 or DQ6, See "Programming & Erasing Operation Status" section for more information on these status bits.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. See the Erase/Program Operations Table 10,11 in "AC Characteristics" for parameters.

Sector Erase Command

Sector erase is a six-bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command.

The device does not require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure the data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6 (Refer to "Programming & Erasing Operation Status" section for more information on these status bits.)
Refer to the Erase/Program Operations Table 10,11 in the "AC Characteristics" section for parameters.

Auto-select Command

The auto-select command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table 5 shows the address and data requirements. This method is an alternative to that shown in Table 3, which is intended for PROM programmers and requires

V_{ID} on address bit A9.

The auto-select command sequence is initiated by writing two unlock cycles, followed by the auto-select command. The device then enters the auto-select mode, and the system may read at any address any number of times, without initiating another command sequence. The read cycles at address 04H, 08H, 0CH, and 00H retrieves the EFST manufacturer ID. A read cycle at address 01H retrieves the device ID. .

7.3 Programming & Erasing Operation Status

The device provides several bits to determine the status of a programming & Erasing operation: DQ7, DQ6, Table 6 and the following subsections describe the functions of these bits. DQ7, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress.

Table 6. Write Operation Status

Operation			DQ7 (Note1)	DQ6
Standard Mode	Embedded Program Algorithm		$\overline{DQ7}$	Toggle
	Embedded Erase Algorithm	Sector erase	0	Toggle
		Chip erase	0	Toggle

Notes:

1. DQ7 require a valid address when reading status information. Refer to the appropriate subsection for further details.

DQ7: Data Polling

During a programming operation, DQ7 returns the complement of the programmed value. During an erase operation, a "0" is produced on DQ7, with this switching to a "1" following the operation. On completion of a programming operation, reading the device after the rising edge of the last – the sixth - write enable ($\overline{WE}$) pulse, returns the value just programmed ("0") on DQ7.

If $\overline{OE}$ is asserted low before the operation is completed, the value of DQ7 many change and it may not represent the correct value. The correct value will be return on the next read cycle, after the system has detected that the value has changed from its complement to the actual value.

Figure 14: Data polling flow chart opposite illustrates the actual process. Relevant signal pulse timings are given in Figure 16 : Data polling timing diagram.

DQ6:Toggle BIT I

During program and erase operations, the toggle bit on DQ6 switches between "0" and "1" on successive bus read attempts at any address. The toggling can be detected after the last rising edge of the write enable

($\overline{WE}$) pulse of an erase or program command sequence and is terminated when the operation is completed. In the case of programming, the last write enable pulse is the fourth; for both the sector erase and chip erase commands, it is the sixth. Figure 15 shows an example use of this function. Relevant signal pulse timings are given in Figure 17: Toggle Bit timing diagram.

7.4 More Device Operations

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes. In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than VLKO, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 15 ns (typical) on $\overline{CE}$ or $\overline{WE}$ do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IH}. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power Supply Decoupling

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between
its V_{CC} and GND.

Power-Up Sequence

The device powers up in the Read Mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

Power-Up Write Inhibit

If $\overline{WE}$ = $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IH} during power up, the device does not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to reading array data on power-up.

8. ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . –65°C to +150°C
Ambient Temperature
with Power Applied. . . . . 0°C to +70°C
Voltage with Respect to Ground
V_{CC} (Note 1) . . . .   –0.5 V to +6.5 V
A9 (Note 2) . . . . –0.5 V to +12.5 V
All other pins (Note 1). . . . . –0.5 V to V_{CC} +0.5 V
Output Short Circuit Current (Note 3) .. . .. 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 1. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 2.

2. Minimum DC input voltage on pins A9 is -0.5 V. During voltage transitions, A9 may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 1. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.

3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

### Figure 1. Maximum Negative Overshoot Waveform
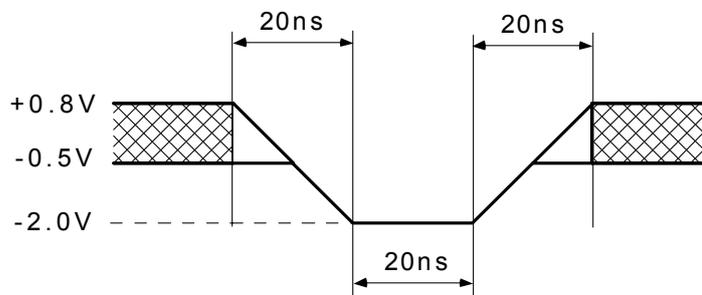
Figure 2. Maximum Positive Overshoot Waveform
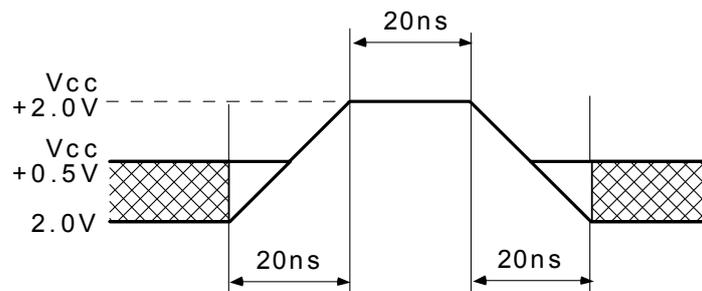
9. OPERATING RANGES

Commercial (C) Devices Ambient Temperature (TA) . . . . 0°C to +70°C

V_{CC} Supply Voltages V_{CC} for all devices . . . . .4.5 V to 5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Table 7. Capacitance T_A = 25°C , f = 1.0 MHz

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
C_{IN1}	Input Capacitance	V_{IN} = 0V			6	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0V			12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V			12	pF

10. DC CHARACTERISTICS

**Table 8. DC Characteristics T_A = 0C to 70C, V_{CC} = 4.5V to 5.5V**

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} or V_{CC}, V_{CC} = V_{CC} max.	-	-	10	uA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} or V_{CC}, V_{CC} = V_{CC} max	-	-	10	uA
I_{CC1}	V_{CC} Active Read Current	$\overline{CE}$= V_{IL}, $\overline{OE}$ = $V_{IH,}$ f = 5MHz	-	-	25	mA
I_{CC2}	V_{CC} Active Write Current	$\overline{CE}$ = V_{IL} ± $\overline{OE}$ = V_{IH}	-	15	30	mA
I_{CC3}	CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3V	-	25	50	uA
I_{CC4}	TTL Standby Current	$\overline{CE}$ = V_{IH}	-	0.2	5	mA
V_{IL}	Input Low Voltage(Note 1)	-	-0.3	-	0.8	V
V_{IH}	Input High Voltage	-	2.0	-	VDD + 0.5	V
V_{ID}	Voltage for Auto-Select and Temporary Sector Unprotect	V_{CC} =5.0V	11.5	-	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	-	-	0.45	V
V_{OH1}	Output High Voltage(TTL)	I_{OH} = 0.4mA	2.4	-	-	V
V_{LKO}	Low V_{CC} Lock-out Voltage	-	3.2	-	-	V

## 11. AC CHARACTERISTICS
TEST CONDITIONS

Figure 3. Test Setup
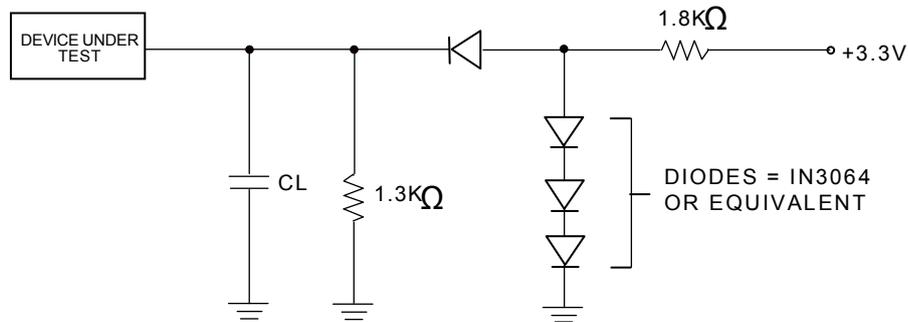
CL = 100pF Including jig capacitance
CL = 30pF for F49B002UA

Figure 4. Input Waveforms and Measurement Levels
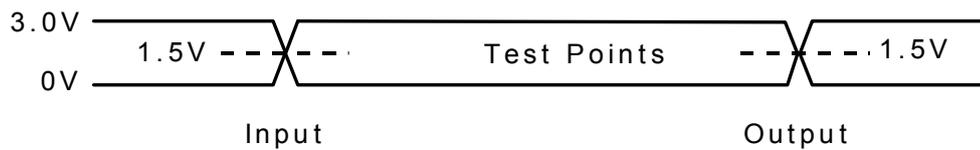
AC TESTING : Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0"
Input pulse rise and fall times are < 5ns.

11.1 Read Operation

TA = 0C to 70C, V$_{CC}$ = 4.5V~5.5V

Table 9. Read Operations

Symbol	Description		Conditions	-70		-90		Unit
				Min.	Max.	Min.	Max.	
t$_{RC}$	Read Cycle Time (Note 1)			70		90		ns
t$_{ACC}$	Address to Output Delay		$\overline{CE}$=$\overline{OE}$ = V$_{IL}$		70		90	ns
t$_{CE}$	$\overline{CE}$ to Output Delay		$\overline{OE}$ = V$_{IL}$		70		90	ns
t$_{OE}$	$\overline{OE}$ to Output Delay		$\overline{CE}$= V$_{IL}$		30		35	ns
t$_{DF}$	$\overline{OE}$ High to Output Float (Note1)		$\overline{CE}$= V$_{IL}$		25		30	ns
t$_{OEH}$	Output Enable	Read		0		0		ns
	Hold Time	Toggle and Data Polling		10		10		ns
t$_{OH}$	Address to Output hold		$\overline{CE}$=$\overline{OE}$= V$_{IL}$	0		0		ns

Notes :
1. Not 100% tested.
2. t$_{DF}$ is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Figure 5. Read Timing Waveform
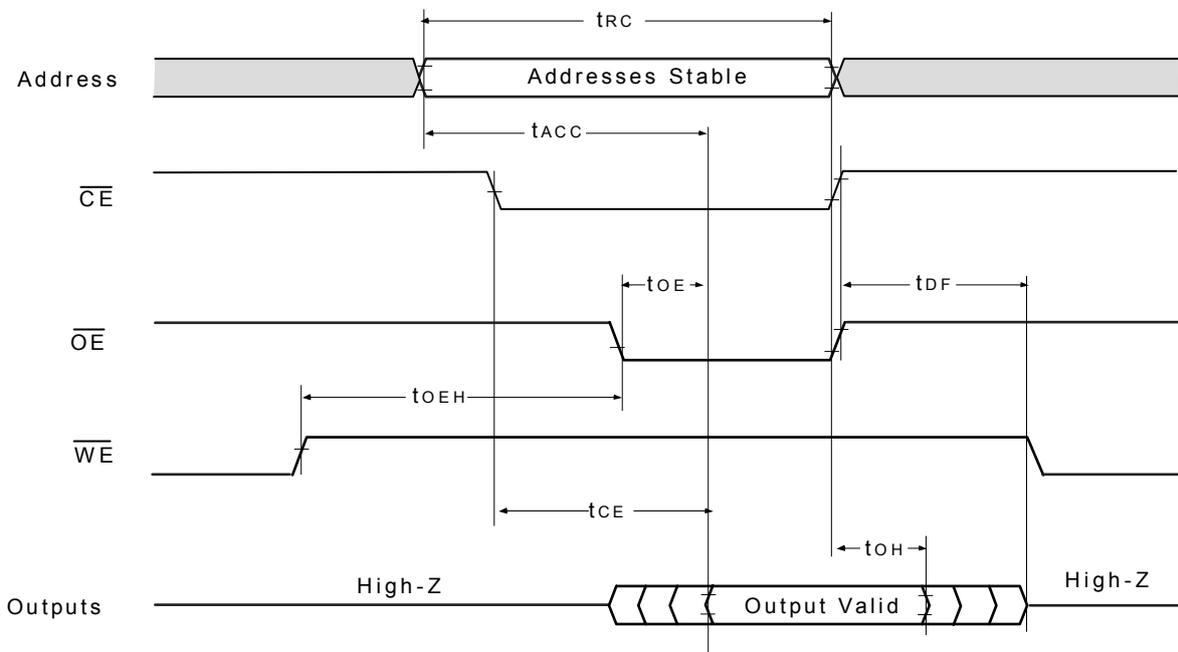
11.2 Program/Erase Operation

Table 10. $\overline{WE}$ Controlled Program/Erase Operations(T_A = 0C to 70C, V_{CC} = 4.5V~5.5V)

Symbol	Description	-70		-90		Unit
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time (Note 1)	70		90		ns
t_{AS}	Address Setup Time	0		0		ns
t_{AH}	Address Hold Time	45		45		ns
t_{DS}	Data Setup Time	30		30		ns
t_{DH}	Data Hold Time	0		0		ns
t_{OES}	Output Enable Setup Time	0		0		ns
t_{GHWL}	Read Recovery Time Before Write ($\overline{OE}$ High to $\overline{WE}$ low)	0		0		ns
t_{CS}	$\overline{CE}$ Setup Time	0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		ns
t_{WP}	Write Pulse Width	35		35		ns
t_{WPH}	Write Pulse Width High	20		20		ns

Notes :
1. Not 100% tested.
2. See the "Programming & Erasing Operation Performance" section for more information.

Table 11. $\overline{CE}$ Controlled Program/Erase Operations(T_A = 0C to 70C, V_{CC} = 4.5V~5.5V)

Symbol	Description	-70		-90		
		Min.	Max.	Min.	Max.	Unit
t_{WC}	Write Cycle Time (Note 1)	70		90		ns
t_{AS}	Address Setup Time	0		0		ns
t_{AH}	Address Hold Time	45		45		ns
t_{DS}	Data Setup Time	35		35		ns
t_{DH}	Data Hold Time	0		0		ns
t_{OES}	Output Enable Setup Time	0		0		ns
t_{GHEL}	Read Recovery Time Before Write	0		0		ns
t_{WS}	$\overline{WE}$ Setup Time	0		0		ns
t_{WH}	$\overline{WE}$ Hold Time	0		0		ns
t_{CP}	$\overline{CE}$ Pulse Width	35		35		ns
t_{CPH}	$\overline{CE}$ Pulse Width High	30		30		ns
t_{WHWH1}	Programming Operation(note2)	10(typ.)		10(typ.)		us
t_{WHWH2}	Sector Erase Operation (note2)	1.5(typ.)		1.5(typ.)		sec

Notes :
1. Not 100% tested.
2. See the "Programming & Erasing operation performance" section for more information.

Figure 6. $\overline{\text{CE}}$ Controlled Program Timing Waveform
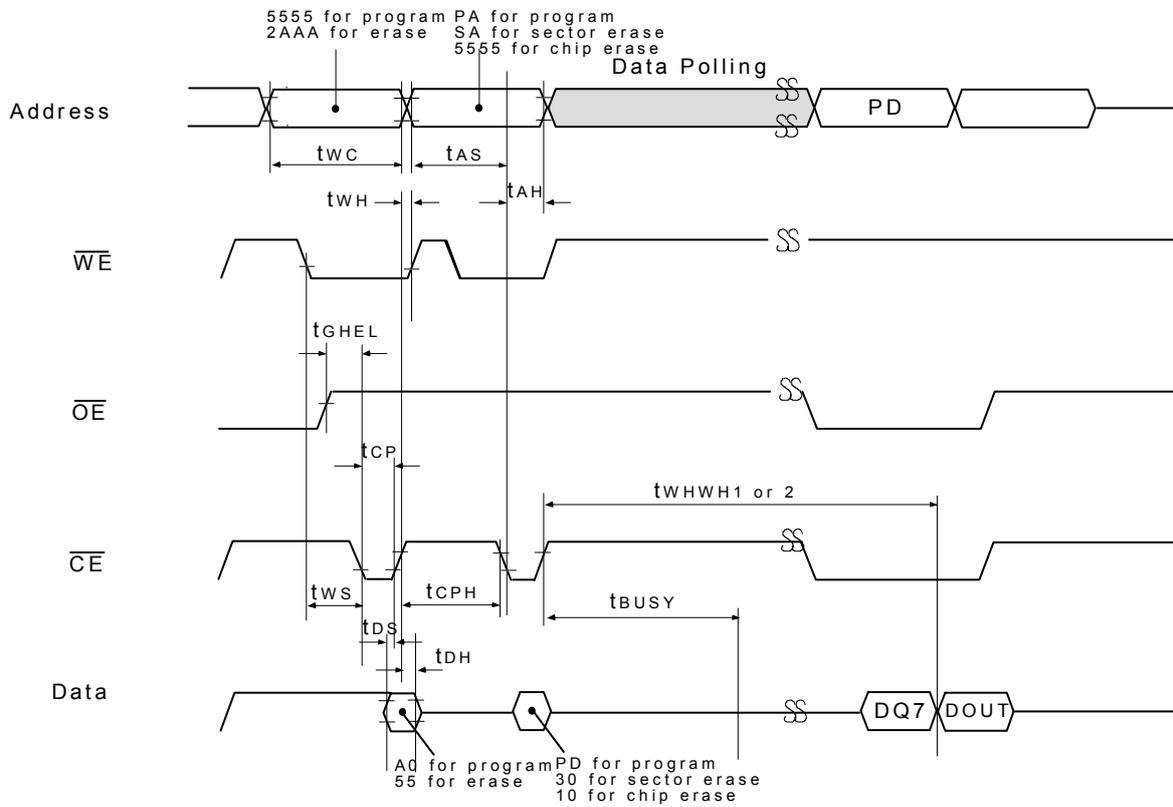
Notes :

   1. PA = Program Address, PD = Program Data, DOUT = Data Out , DQ7 = complement of data written to device
   2. Figure indicates the last two bus cycles of the command sequence..

**Figure 7. Write Command Timing Waveform**
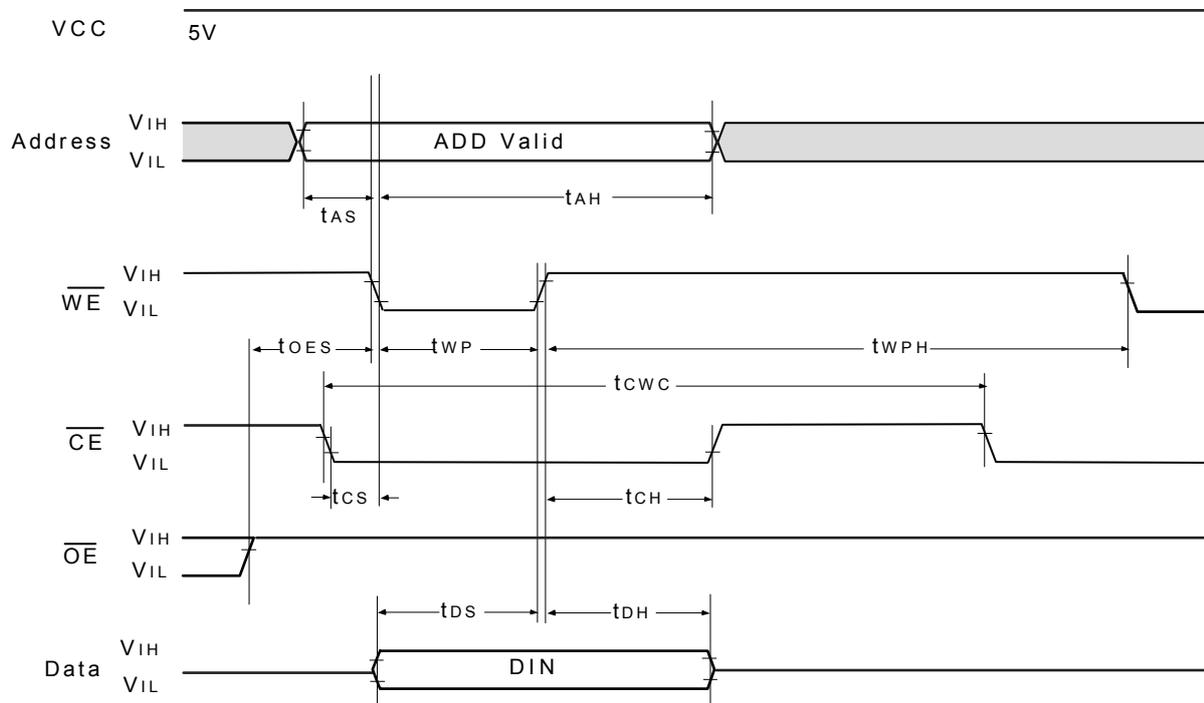
Figure 8. Embedded Programming Timing Waveform
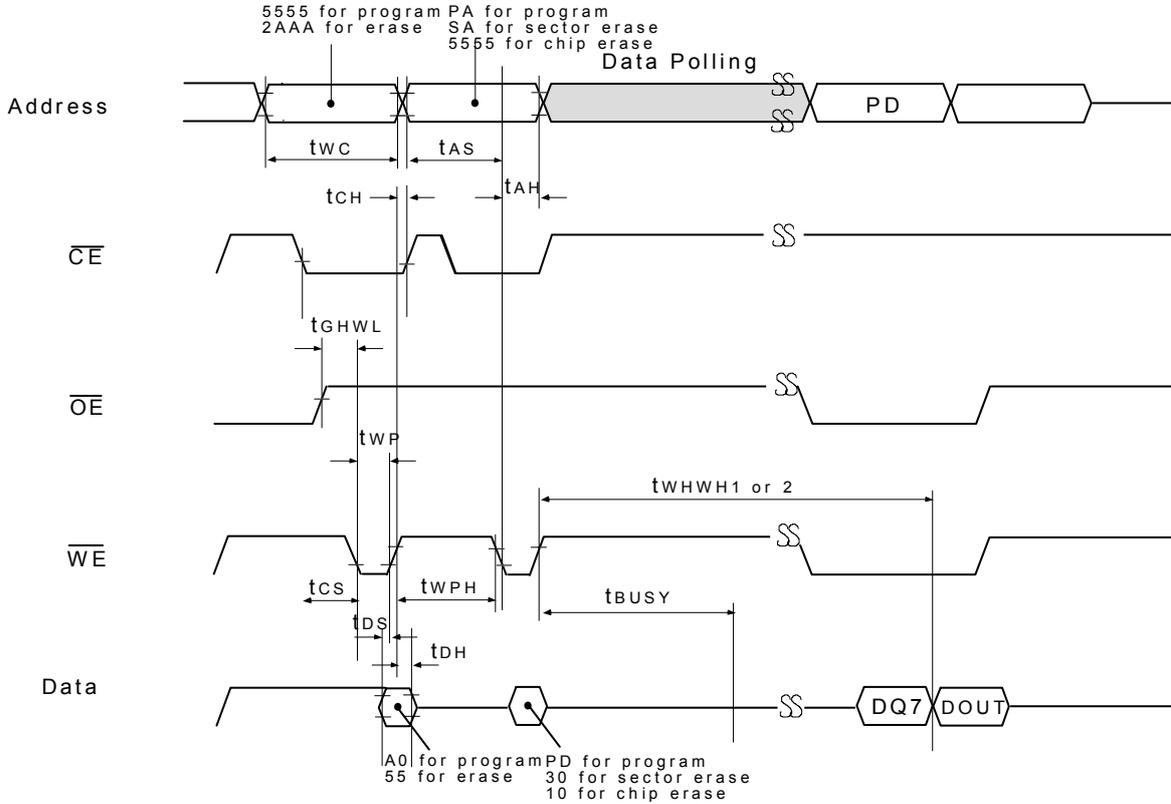
Notes :

1. PA = Program Address, PD = Program Data, DOUT = Data Out , DQ7 = complement of data written to device
2. Figure indicates the last two bus cycles of the command sequence..

Figure 9. Embedded Programming Algorithm Flowchart
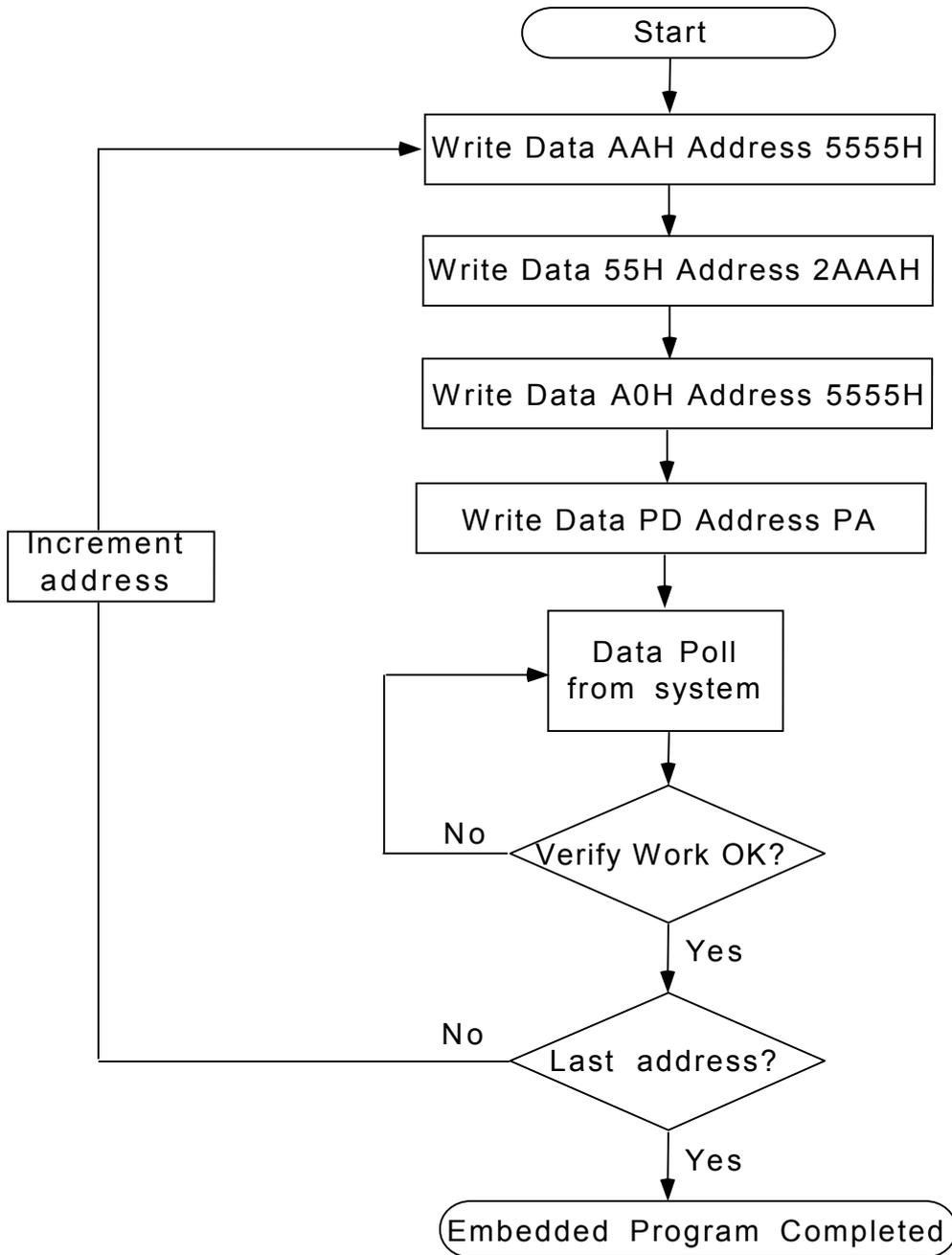
12. PROGRAMMING & ERASING OPERATION PERFORMANCE

Table 12. Erase And Programming Performance (Note.1)

Parameter	Limits		Unit
	Typ.(2)	**Max.(3)**	
Sector Erase Time	1.5	5	sec
Chip Erase Time	3	35	sec
Byte Programming Time	10	200	Us
Chip Programming Time	2	5	Sec
Erase/Program Cycles (1)	100,000	-	Cycles

Notes:

    1.Not 100% Tested, Excludes external system level over head.
    2.Typical values measured at 25°C, 5V.
    3.Maximum values measured at 85°C, 4.5V.

Figure 10. Embedded Chip Erase Timing Waveform
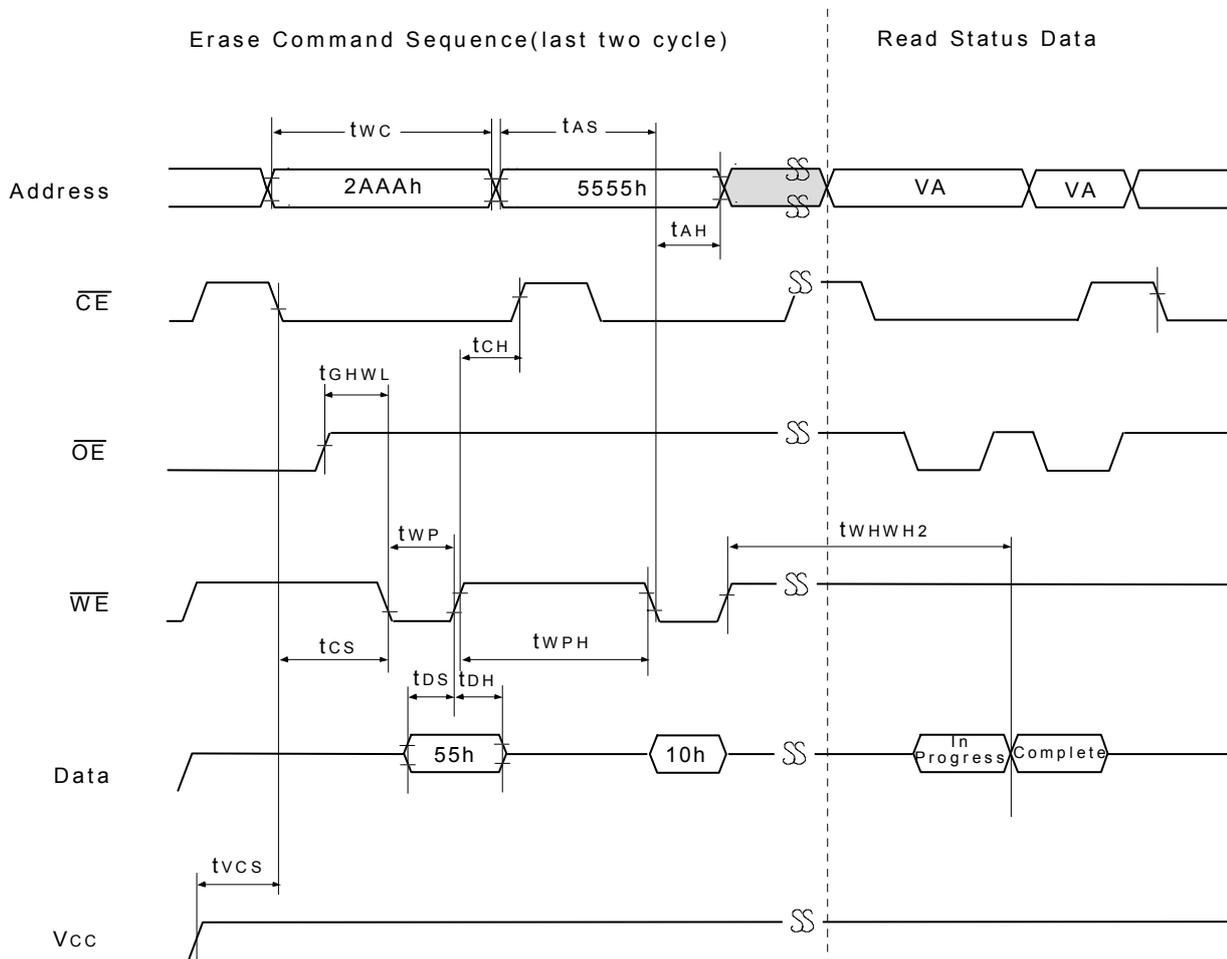
Notes :

SA = Sector Address (for Sector Erase, VA = Valid Address for reading status data
(see "Write Operation Status")

Figure 11. Embedded Chip Erase Algorithm Flowchart

```
                    ┌─────────────┐
                    │    Start    │
                    └─────────────┘
                           │
                           ▼
          ┌──────────────────────────────────┐
          │  Write Data AAH Address 5555H     │
          └──────────────────────────────────┘
                           │
                           ▼
          ┌──────────────────────────────────┐
          │  Write Data 55H Address 2AAAH     │
          └──────────────────────────────────┘
                           │
                           ▼
          ┌──────────────────────────────────┐
          │  Write Data 80H Address 5555H     │
          └──────────────────────────────────┘
                           │
                           ▼
          ┌──────────────────────────────────┐
          │  Write Data AAH Address 5555H     │
          └──────────────────────────────────┘
                           │
                           ▼
          ┌──────────────────────────────────┐
          │  Write Data 55H Address 2AAAH     │
          └──────────────────────────────────┘
                           │
                           ▼
          ┌──────────────────────────────────┐
          │  Write Data 10H Address 5555H     │
          └──────────────────────────────────┘
                           │
                           ▼
  ┌──────► ┌──────────────────────────────────┐
  │        │   Data Polling from System        │
  │        └──────────────────────────────────┘
  │                        │
  │                        ▼
  │   No              ◇ Data = FFh? ◇
  └───────────────────
                           │ Yes
                           ▼
          ┌──────────────────────────────────┐
          │  Embedded Chip Erease Completed   │
          └──────────────────────────────────┘
```
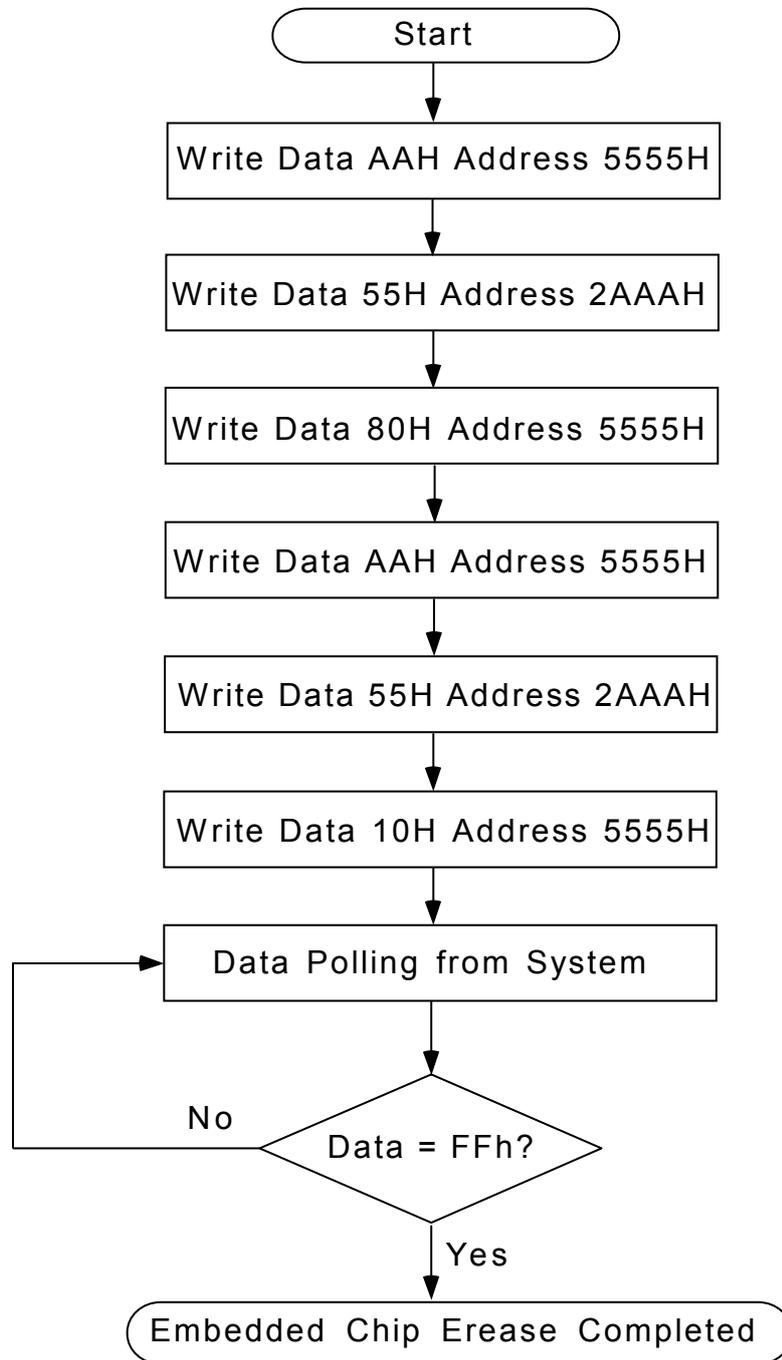
Figure 12. Embedded Sector Erase Timing Waveform
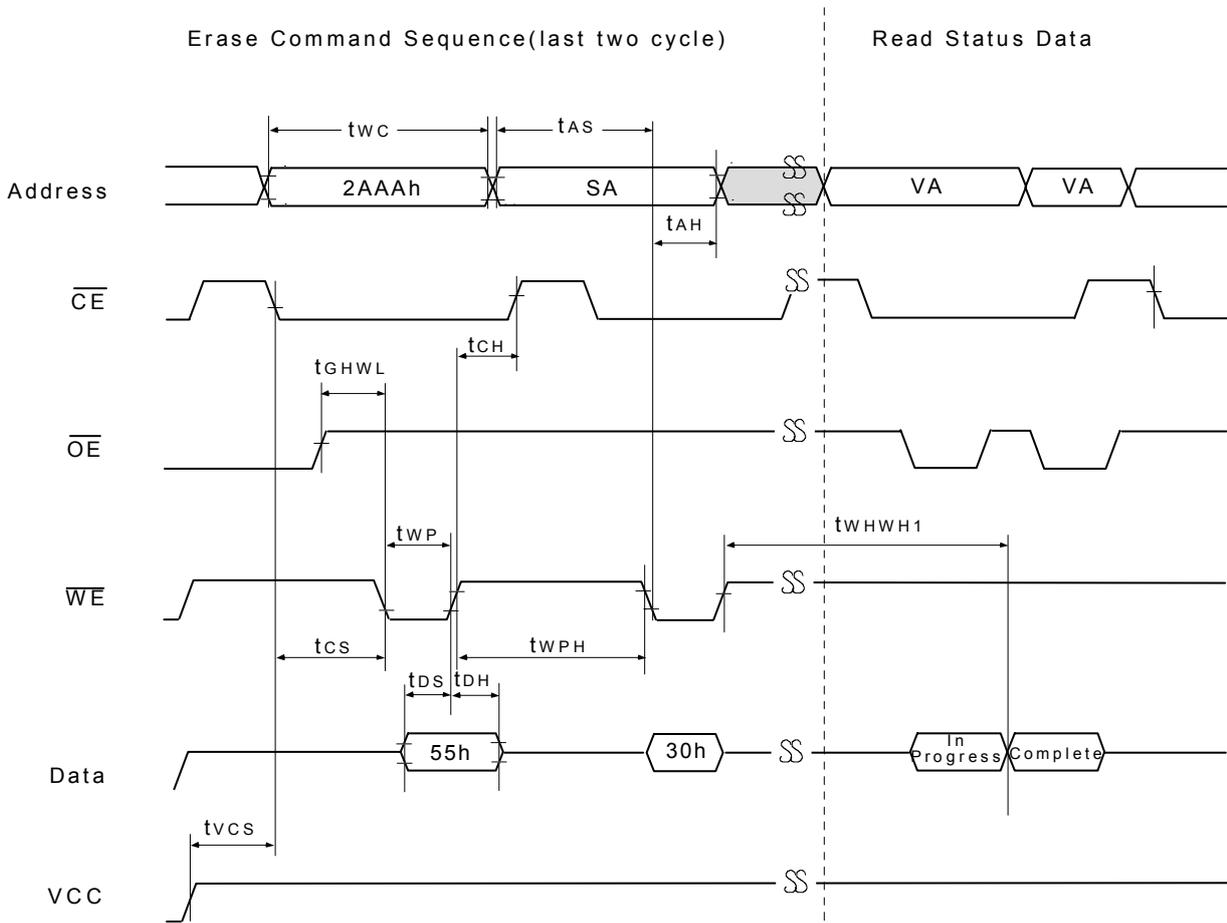
Notes :

    SA = Sector Address (for Sector Erase, VA = Valid Address for reading status data
        (see "Programming & Erasing Operation Status")

Figure 13. Embedded Sector Erase Algorithm Flowchart

```
                    ┌─────────────────┐
                    (     Start       )
                    └────────┬────────┘
                             │
           ┌─────────────────────────────────┐
           │ Write Data AAH Address 5555H     │
           └────────────────┬────────────────┘
                            │
           ┌─────────────────────────────────┐
           │ Write Data 55H Address 2AAAH     │
           └────────────────┬────────────────┘
                            │
           ┌─────────────────────────────────┐
           │ Write Data 80H Address 5555H     │
           └────────────────┬────────────────┘
                            │
           ┌─────────────────────────────────┐
           │ Write Data AAH Address 5555H     │
           └────────────────┬────────────────┘
                            │
           ┌─────────────────────────────────┐
           │ Write Data 55H Address 2AAAH     │
           └────────────────┬────────────────┘
                            │
           ┌─────────────────────────────────┐
           │ Write Data 30H Address SA        │
           └────────────────┬────────────────┘
                          Yes
                            │
           ┌─────────────────────────────────┐◄──────┐
           │ Data Poll from System            │       │
           └────────────────┬────────────────┘       │
                            │                         │
                        ╱───────╲           No        │
                      ╱ Data = FFh? ╲────────────────┘
                        ╲───────╱
                            │
                    ┌─────────────────┐
                    ( Embedded Sector  )
                    ( Erease Completed )
                    └─────────────────┘
```
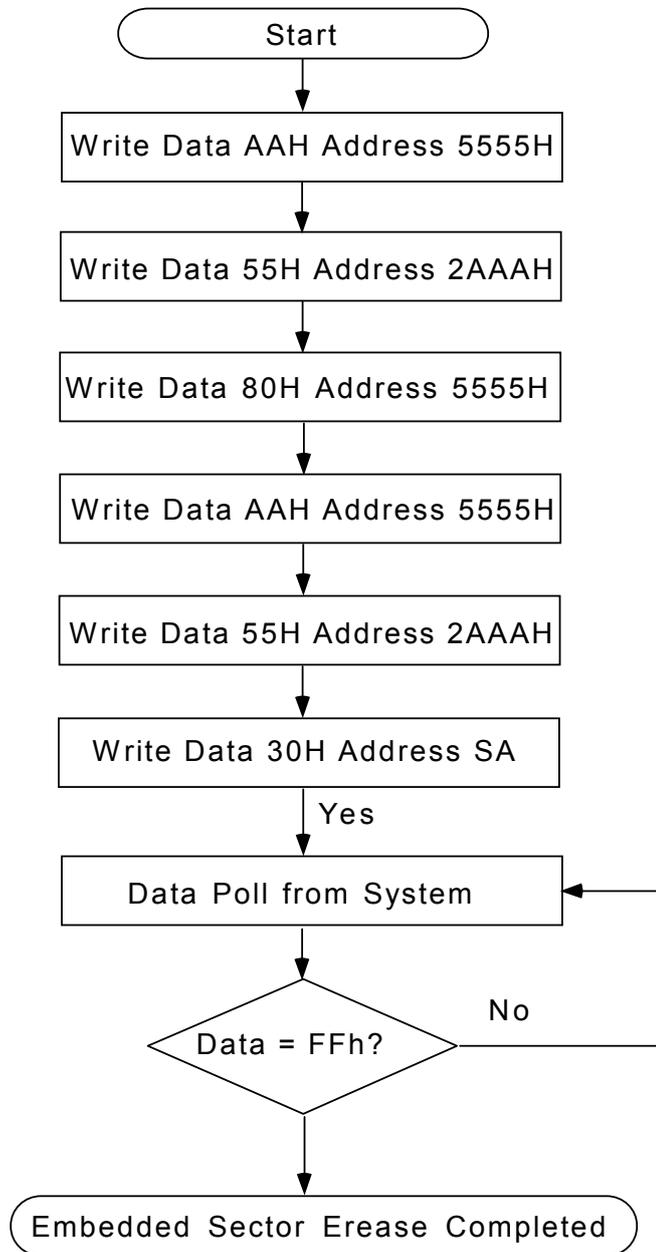
PROGRAMMING & ERASING OPERATION STATUS

Figure 14. Data Polling Algorithm

```
         ┌──────────────┐
         │    Start     │
         └──────┬───────┘
                │
                ▼
     ┌────────────────────┐
────▶│   Read DQ7~DQ0     │
│    │    Add. = VA(1)    │
│    └─────────┬──────────┘
│              │
│              ▼
│          ╱────────╲
│  No     ╱           ╲
└────────◀  DQ7 = Data? ╲
          ╲           ╱
           ╲─────────╱
                │ Yes
                ▼
         ┌──────────────┐
         │     Pass     │
         └──────────────┘
```
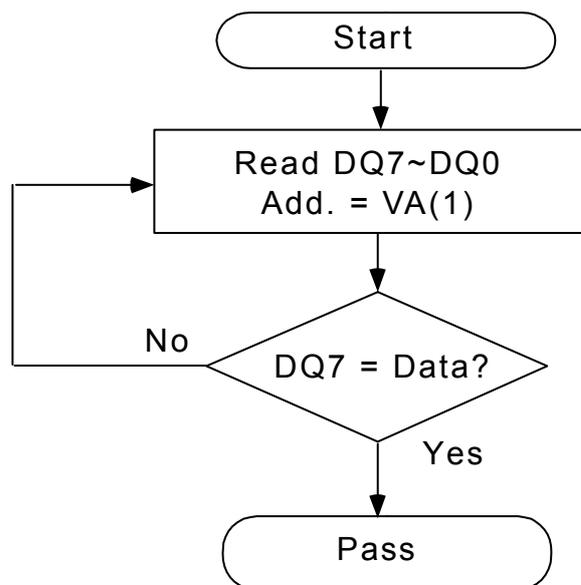
Notes :

     1. VA =Valid address for programming.

Figure 15. Toggle Bit Algorithm

```
                    ┌──────────┐
                    │  Start   │
                    └────┬─────┘
                         │
                         ▼
              ┌────────────────────┐
              │   Read DQ7~DQ0     │
              └──────────┬─────────┘
                         │
                         ▼
              ┌────────────────────┐
    ┌────────▶│   Read DQ7~DQ0     │  (Note1)
    │         └──────────┬─────────┘
    │                    │
    │                    ▼
    │ Yes        ╱───────────────╲
    └───────────╱  Toggle Bit = DQ6 ╲
                ╲   Toggle?         ╱
                 ╲─────────┬───────╱
                           │ No
                           ▼
                    ┌──────────┐
                    │  Pass    │
                    └──────────┘
```
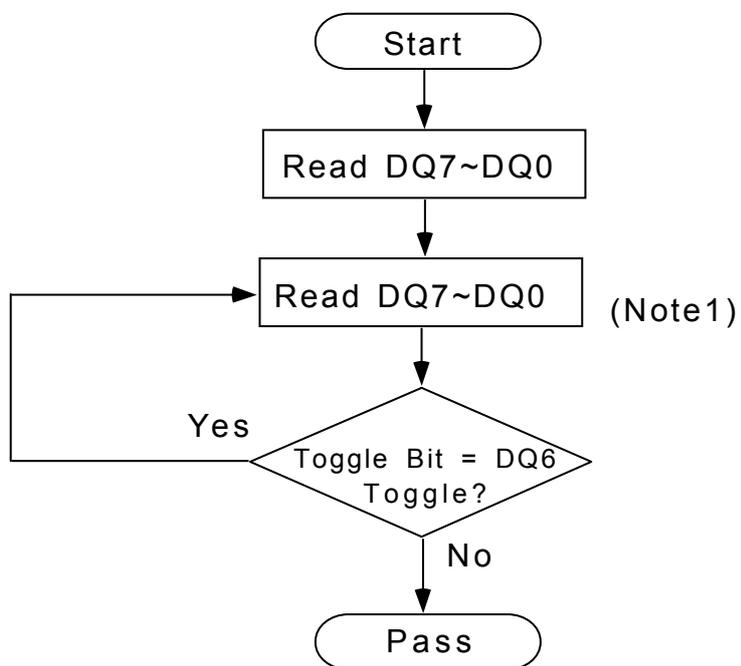
Note :

     1. Read toggle bit twice to determine whether or not it is toggle.

Figure 16. Data Polling Timings (During Embedded Algorithms)
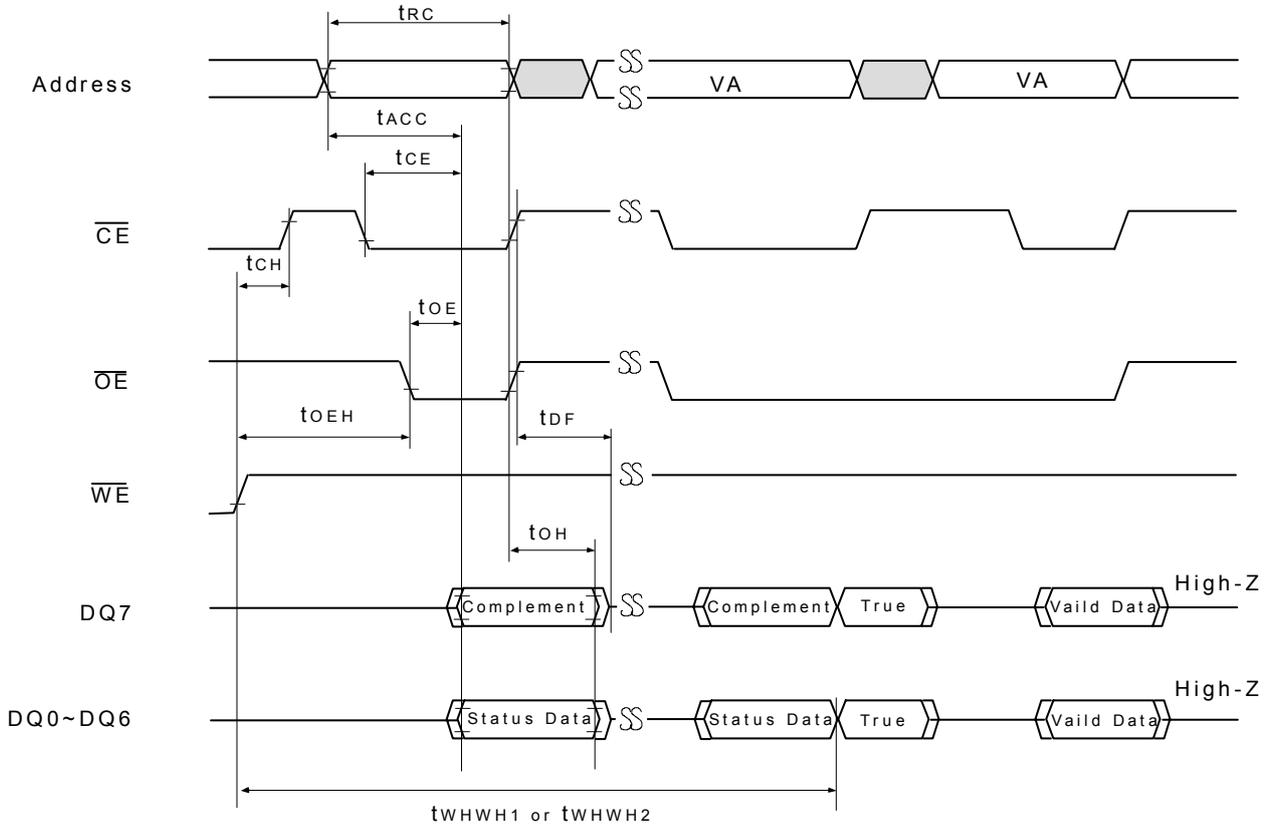
Notes :

VA = Valid Address. Figure shows first status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 17. Toggle Bit Timing Waveforms (During Embedded Algorithms)
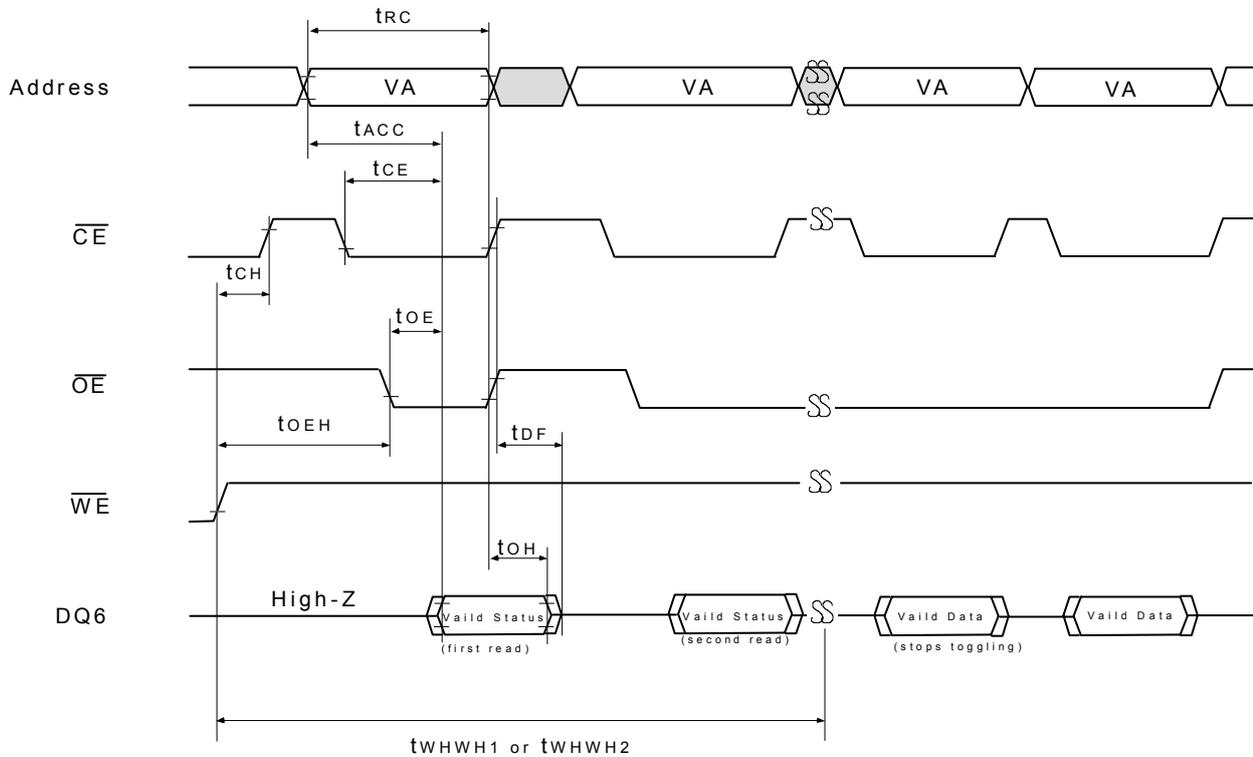
Notes :

VA = Valid Address; not required for DQ6. Figure shows first status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 18. ID Code Read Timing Waveform
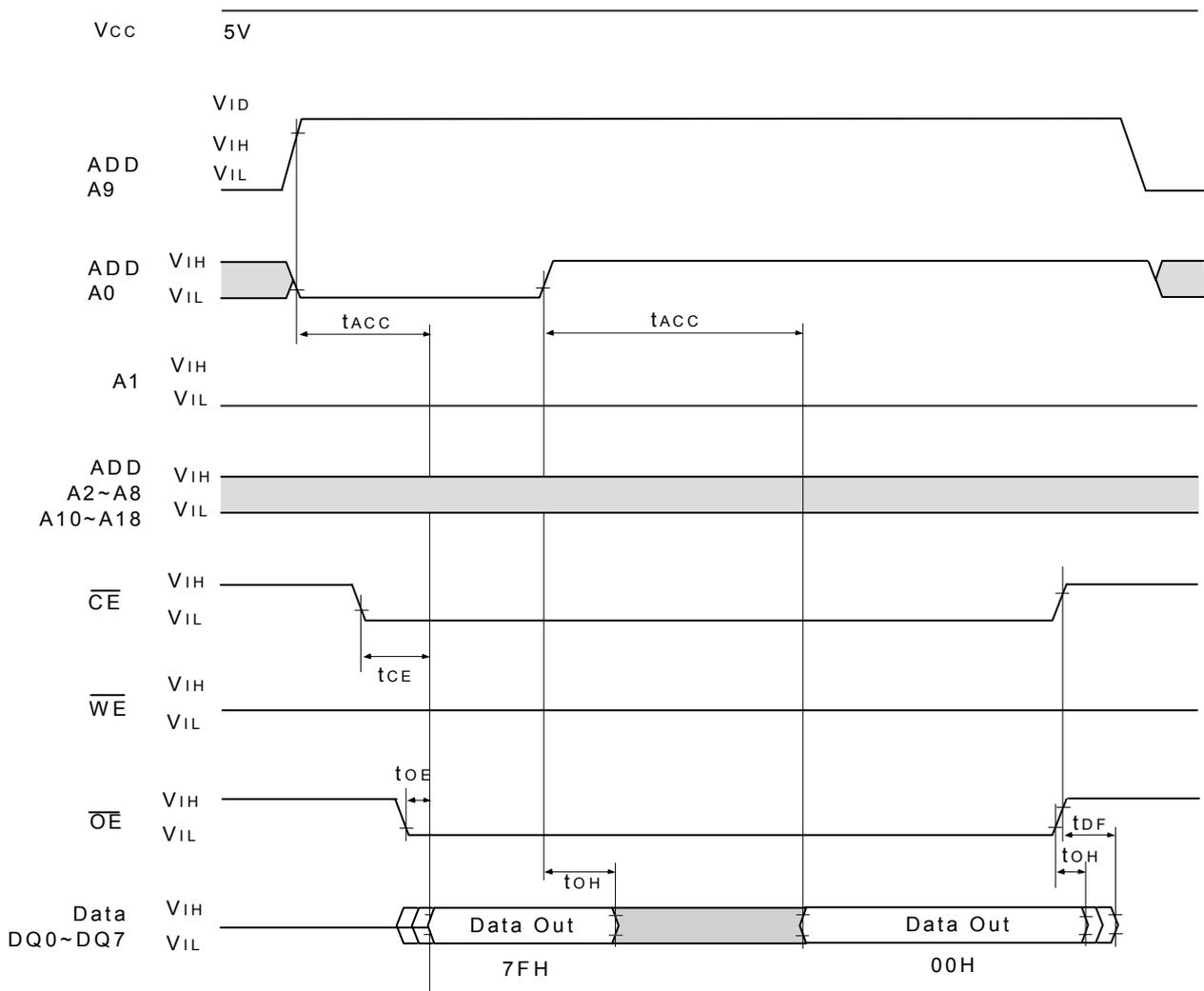
12. PACKAGE DIMENSION

32-LEAD   PDIP
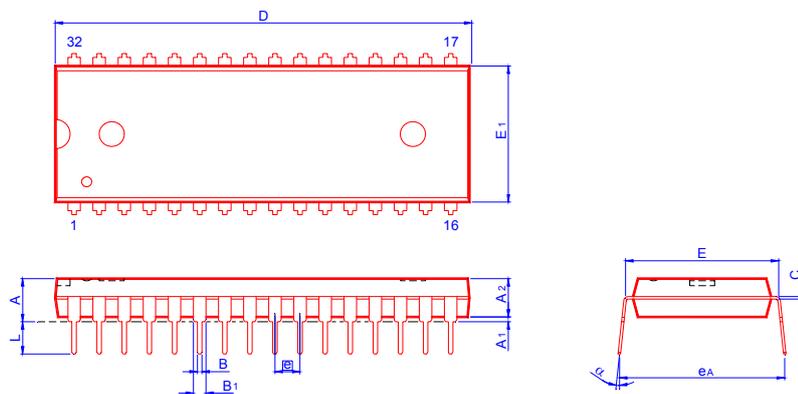
	Dimension in inch			Dimension in mm		
	Min	**Norm**	**Max**	**Min**	**Norm**	**Max**
A	-------	-------	0.210	-------	-------	5.33
A 1	0.015	-------	-------	0.381	-------	-------
A 2	0.149	0.154	0.159	3.785	3.912	4.039
B	0.018 TYP			0.457 TYP		
B1	0.050 TYP			1.270 TYP		
C	-------	0.010	-------	-------	0.254	-------
E	0.590	-------	0.625	14.986	-------	15.875
E 1	0.530	-------	0.560	13.462	-------	14.224
e A	0.600 BSC	15.240 BSC				
L	0.120	-------	0.150	3.048	-------	3.810
e	0.100 TYP			2.540 TYP		
α		-------	15°		-------	15°

32-LEAD   PLCC
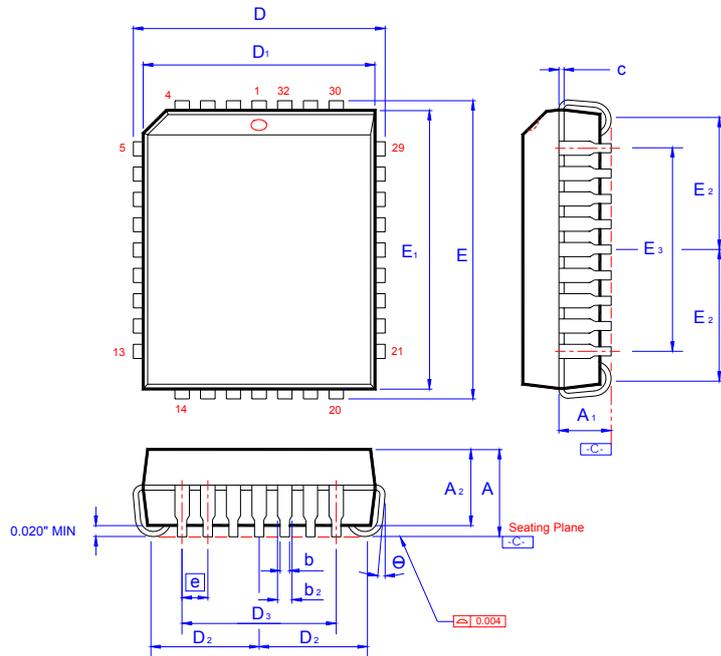
Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	3.18	-------	3.55	0.125	-------	0.140
A 1	1.53	-------	2.41	0.060	-------	0.095
A 2	2.79 REF			0.110 REF		
b	0.33	-------	0.54	0.013	-------	0.021
b2	0.66	-------	0.82	0.026	-------	0.032
c	0.20	-------	0.36	0.008	-------	0.014
e	1.27 BSC			0.050 BSC		
θ	0°	-------	10°	0°	-------	10°
E	14.86	14.99	15.11	0.585	0.590	0.595
E 1	13.90	13.97	14.04	0.547	0.550	0.553
E 2	6.05	-------	6.93	0.238	-------	0.273
E 3	10.16 BSC			0.400 BSC		
D	12.32	12.45	12.57	0.485	0.490	0.495
D 1	11.36	11.43	11.50	0.447	0.450	0.453
D 2	4.78	-------	5.66	0.188	-------	0.223
D 3	7.62 BSC			0.300 BSC		

Important Notice