EMIF03-SIM02F2

3-line IPAD™, EMI filter including ESD protection

Features

■ EMI symmetrical (I/O) low-pass filter

■ High efficiency in EMI filtering

■ Lead-free package

■ Very low PCB space consuming:
  1.42 mm x 1.42 mm

■ Very thin package: 0.65 mm

■ High efficiency in ESD suppression

■ High reliability offered by monolithic integration

■ High reduction of parasitic elements through integration and wafer level packaging

Complies with the following standards

■ IEC 61000-4-2, Level 4 on external and V_{cc} pins:
  – 15 kV (air discharge)
  – 8 kV (contact discharge)

■ IEC 61000-4-2, Level 1 on internal pins:
  – 2 kV (air discharge)
  – 2 kV (contact discharge)

■ MIL STD 883E - Method 3015-6 Class 3

Applications

EMI filtering and ESD protection for:

■ SIM Interface (Subscriber Identify Module)

■ UIM Interface (Universal Identify Module)

Description

The EMIF03-SIM02F2 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interference.The EMIF03 Flip Chip packaging means the package size is equal to the die size.

This filter includes an ESD protection circuitry which prevents damage to the application when subjected to ESD surges up 15kV.
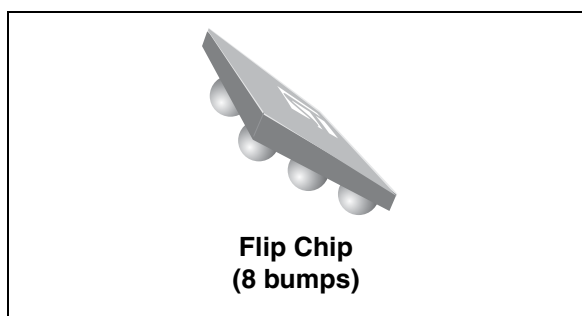

**Flip Chip
(8 bumps)**

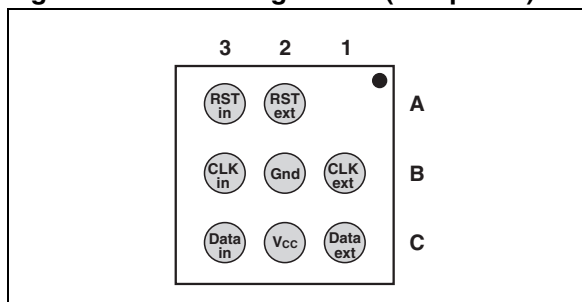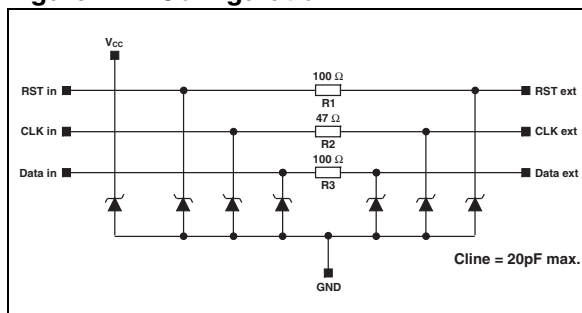**Figure 1.   Pin configuration (bump side)**

Figure 2.   Configuration

TM: IPAD is a trademark of STMicroelectronics.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	**Internal pins (A3, B3, C3):** ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharge **External pins (A2, B1, C2, C1):** ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharge	2 2 15 8	kV
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

Table 2. Electrical characteristics (T_{amb} = 25 °C)
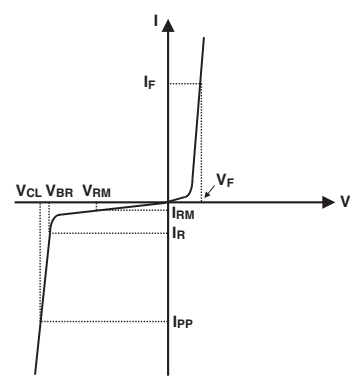
Symbol	Parameters
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
C_{line}	Input capacitance per line

Symbol	Test conditions	Min	Typ	Max	Unit
V_{BR}	I_R = 1 mA	6		20	V
I_{RM}	V_{RM} = 3V			0.2	µA
R_d			1.5		Ω
R_1, R_3	Tolerance ± 20%		100		Ω
R_2	Tolerance ± 20%		47		Ω
C_{line}	@ 0V			20	pF

Figure 3.   **S21 (dB) attenuation measurement (A2-A3 line)**
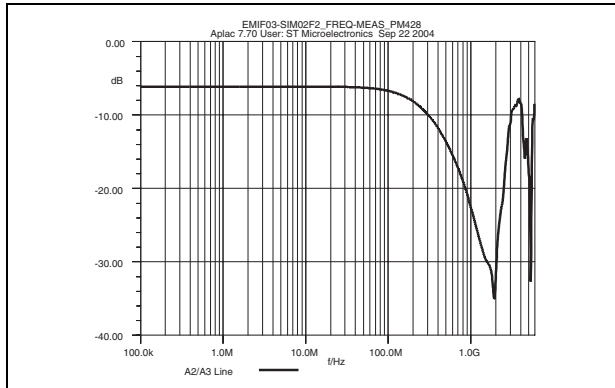

Figure 4.   **S21 (dB) attenuation measurement (B1-B3 line)**
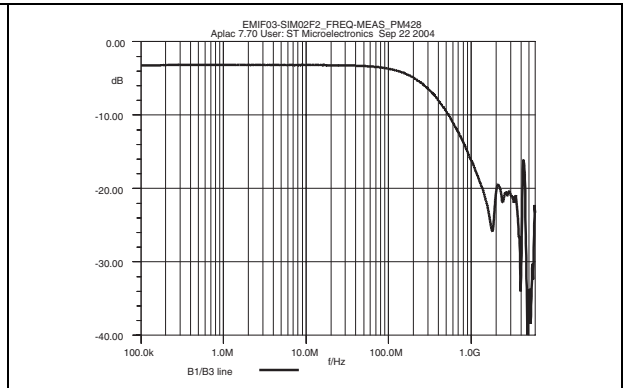

Figure 5.   **S21 (dB) attenuation measurement (C1-C3 line)**
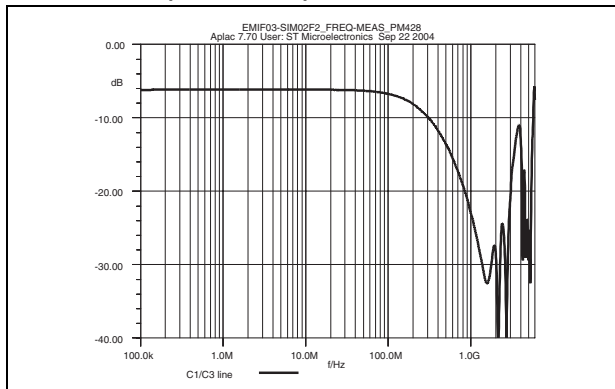

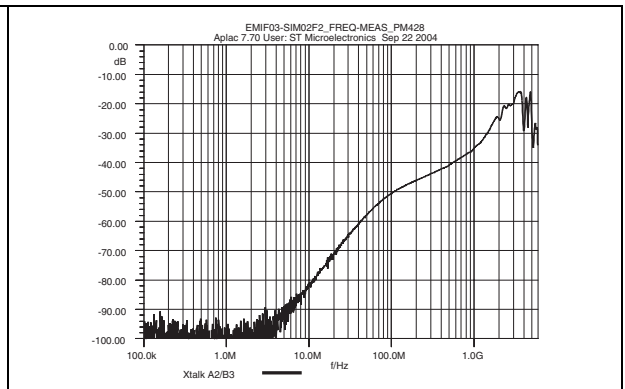**Figure 6.**   **Analog crosstalk measurements**

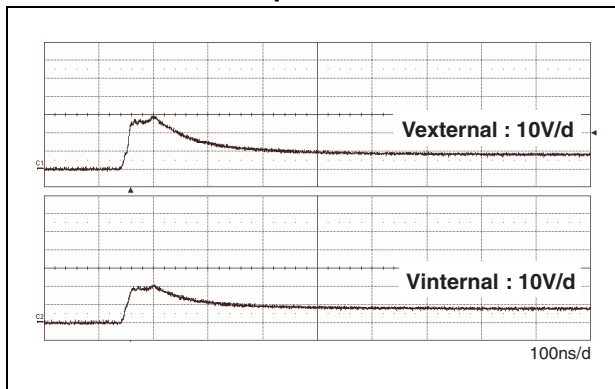**Figure 7.**   **Voltages when IEC61000-4-2 (+15 kV air discharge) applied to external pin**

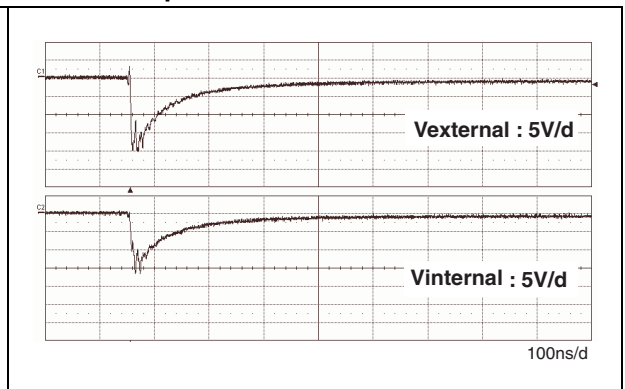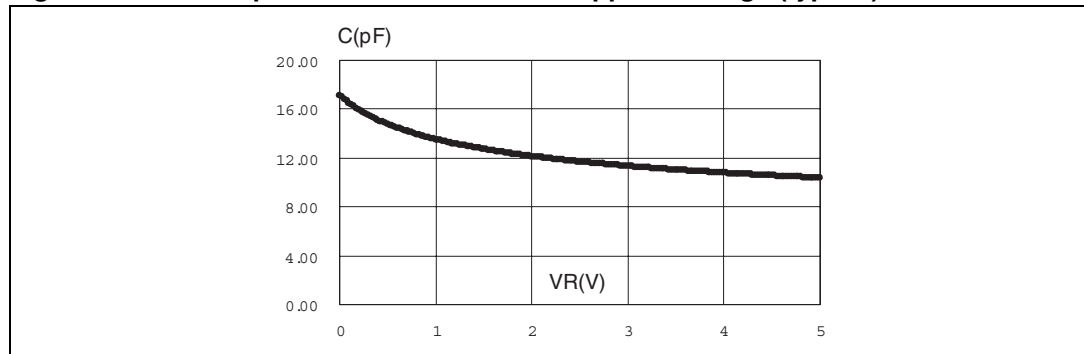**Figure 8.**   **Voltages when IEC61000-4-2 (-15 kV air discharge) applied to external pin**

Figure 9.   Line capacitance versus reverse applied voltage (typical)

2   Application information

Figure 10.   Aplac model
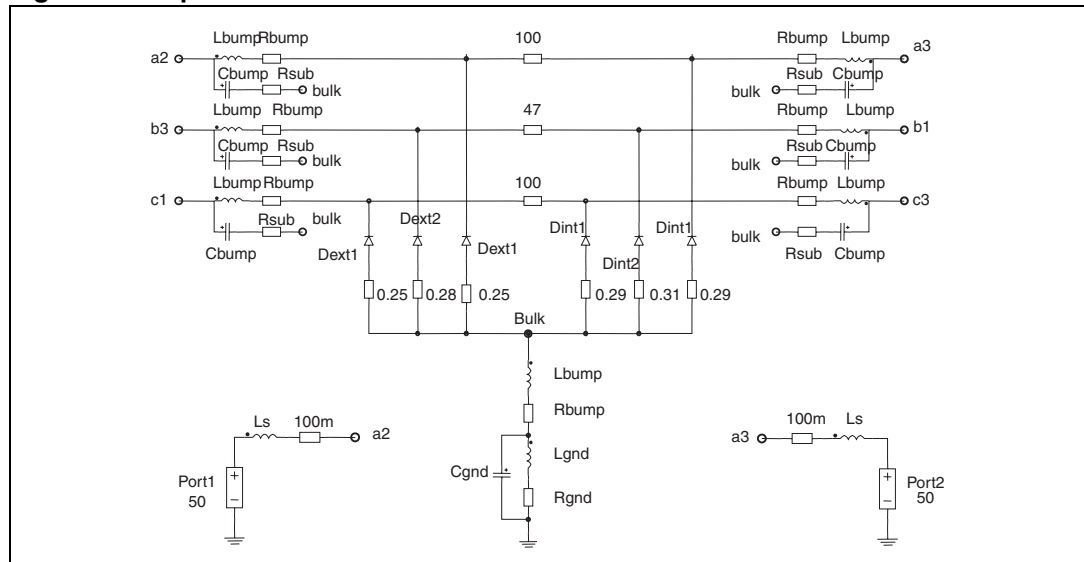
**Figure 11.   Aplac parameters**

Ls 950pH				
Rs 150m	**Model Dint1**	**Model Dext1**	**Model Dint2**	**Model Dext2**
Cext1 15pF	**BV=15**	**BV=15**	**BV=15**	**BV=15**
Cint1 4.5pF	**CJO=Cint1**	**CJO=Cext1**	**CJO=Cint2**	**CJO=Cext2**
Cext2 14pF	**IBV=1u**	**IBV=1u**	**IBV=1u**	**IBV=1u**
Cint2 4pF	**IKF=1000**	**IKF=1000**	**IKF=1000**	**IKF=1000**
Rbump 20m	**IS=10f**	**IS=10f**	**IS=10f**	**IS=10f**
Lbump 50pH	**ISR=100p**	**ISR=100p**	**ISR=100p**	**ISR=100p**
Cbump 0.15pF	**N=1**	**N=1**	**N=1**	**N=1**
Rgnd 500m	**M=0.3333**	**M=0.3333**	**M=0.3333**	**M=0.3333**
Lgnd 50pH	**RS=0.001m**	**RS=0.001m**	**RS=0.001m**	**RS=0.001m**
Cgnd 0.15pF	**VJ=0.6**	**VJ=0.6**	**VJ=0.6**	**VJ=0.6**
Rsub 100m	**TT=50n**	**TT=50n**	**TT=50n**	**TT=50n**

3   Ordering information scheme

Figure 12.   Ordering information scheme
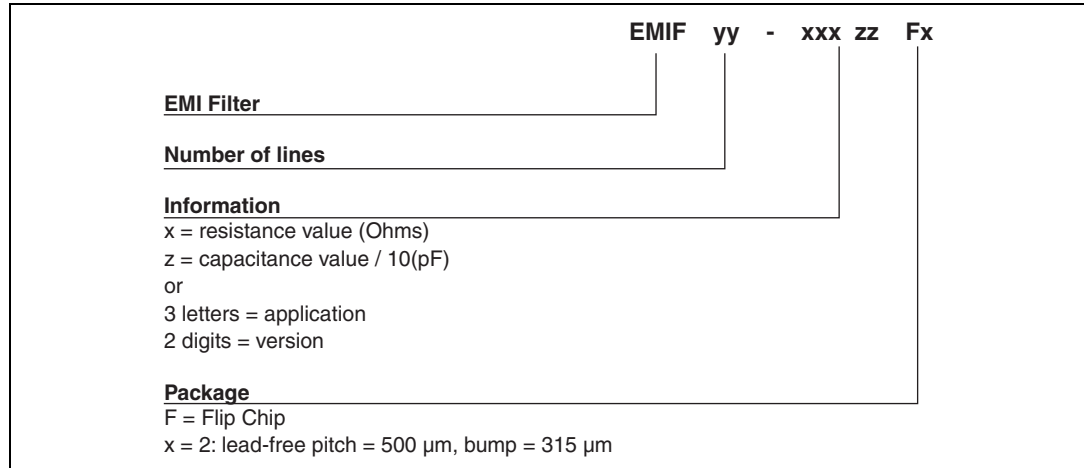
4   Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK®
packages. These packages have a lead-free second level interconnect. The category of
second level interconnect is marked on the inner box label, in compliance with JEDEC
Standard JESD97. The maximum ratings related to soldering conditions are also marked on
the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at
www.st.com.

Figure 13.   Package dimensions
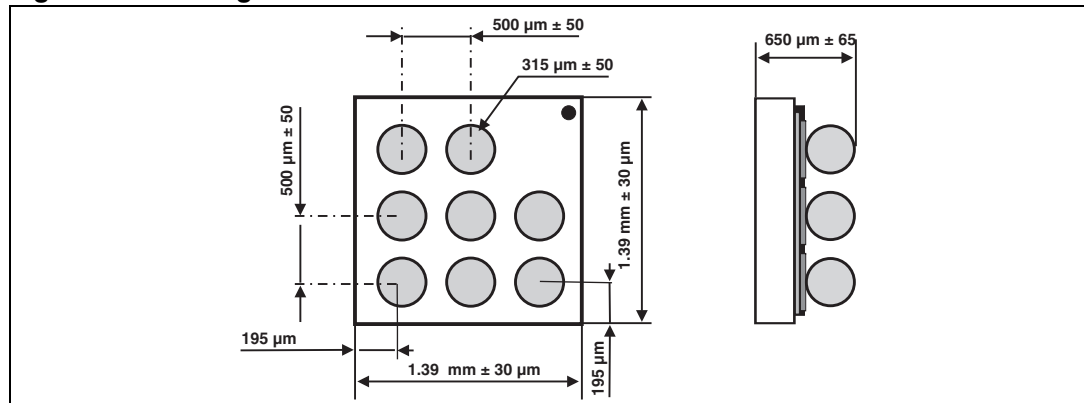
Figure 14.   Footprint
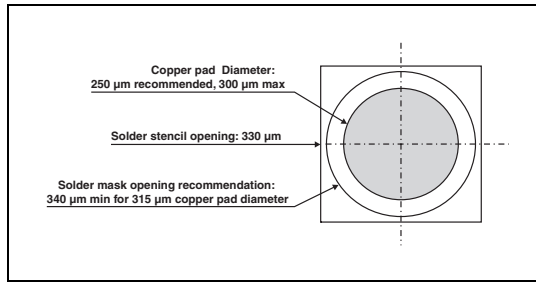
Figure 15.   Marking
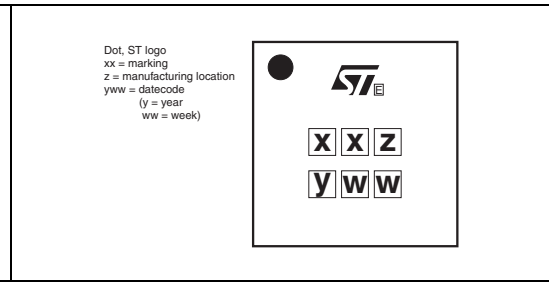
Figure 16.   Flip Chip tape and reel specification
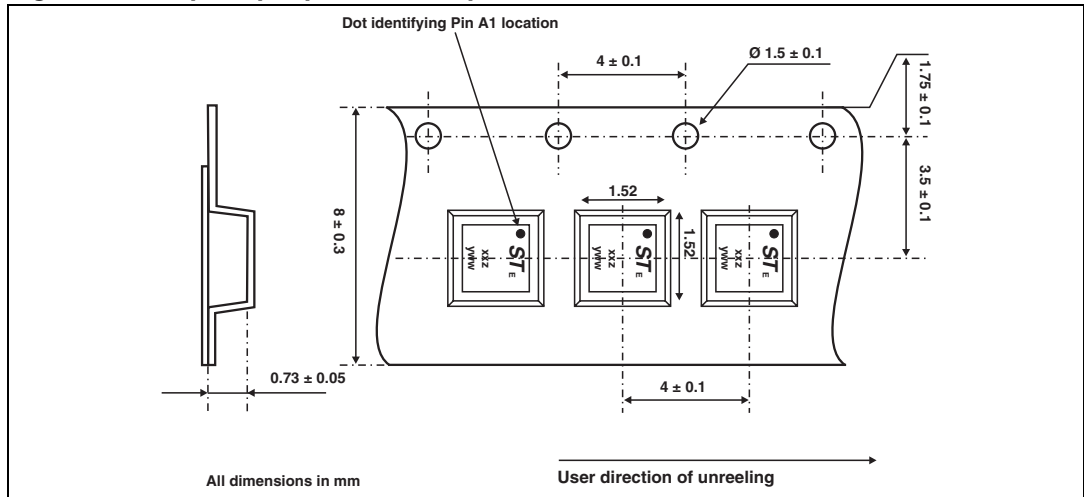
Note: *More information isavailable in the application notes:*

AN1235:"Flip Chip: Package description and recommendations for use"

AN1751: "EMI filters: Recommendations and measurements"

5   Ordering information

Table 3.   Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF03-SIM02F2	GJ	Flip Chip	2.65 mg	5000	Tape and reel 7"

6 Revision history

Table 4.   Document revision history

Date	Revision	Changes
08-Oct-2004	1	First issue.
20-Oct-2004	2	Minor layout update.
25-Mar-2005	3	Figure 1 on page 1: pin configuration definitions changed from RST out, CLK out and Data out to RST ext, CLK ext and Data ext.
13-Jun-2005	4	Titles in Figures 7 and 8 changed - No technical data changed
12-Sep-2005	5	"out" changed to "ext" in Figure 2.
24-Apr-2008	6	Updated ECOPACK statement. Updated *Figure 12*, *Figure 13*, *Figure 14*, *Figure 15* and *Figure 16.* Reformatted to current standards.

Please Read Carefully: