AL4CE211/221/231/241/251

512, 1K, 2K, 4K, 8K x 9 Advanced Synchronous FIFOs

Applications

- Multimedia System
- ATM Switches
- Routers
- Cable Modems
- Wireless Base Stations
- SONET(Synchronous Optical Network) Multiplexers
- TBC(Time Base Corrector)
- Hard Disk cache memory

Description

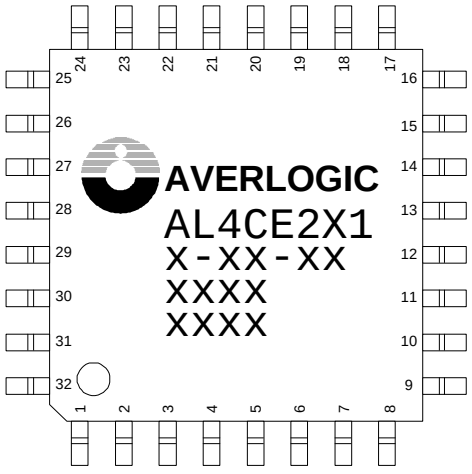
The AL4CE2x1 series memory products are high-performance, low-power 9bit read/write FIFO (First-In-First-Out) memory chip designed to buffer high speed streaming data for a wide range of applications. The AL4CE2x1 FIFO memories are the advanced version of AL4CS2x1. Retransmit is supported in this product series to reduce designing efforts.

Features

- High performance, low-power, FIFO(First-In First-Out) memory
- 512 x 9 bit I/O port (AL4CE211)
- 1K x 9 bit 1/O port (AL4CE221)
- 2K x 9 bit I/O port (AL4CE231)
- 4K x 9 bit I/O port (AL4CE241)
- 8K x 9 bit I/O port (AL4CE251)
- High clock speed (133MHz)
- Fully independent read/write access
- Retransmit the data (reread the data)
- Empty, Full, and programmable Almost Empty, Almost Full flags
- Output enable control (data skipping)
- 3.3V power with 5V signal tolerant input
- Standard 32-pin TQFP

Ordering Information

Part number	AL4CE211, AL4CE221, AL4CE231, AL4CE241, AL4CE251
Package	32-pin plastic TQFP
Power Supply	+3.3V±10%



TQFP PACKAGE TOP VIEW

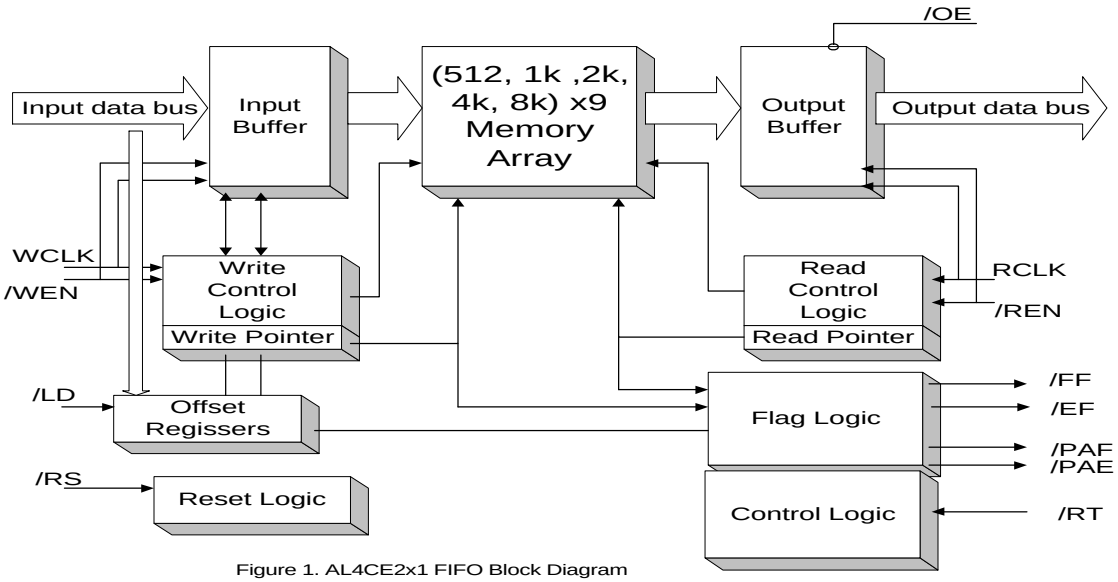


Figure 1. AL4CE2x1 FIFO Block Diagram

The 9bit input and output ports operate independently at a maximum speed of 133 MHz. The built-in address decoder and pointer managing circuits provide a straightforward bus interface to serially read/write memory that reduces inter-chip design efforts. The AL4CE2x1 embedded memory array and high performance process technologies with extended controller functions (read skip, fixed and programmable status flags.. etc.) offer flexible memory management.

These FIFOs support 9bit input and output data bus-width that is controlled by separate clock and enable signals respectively. The input data is acquired at each rising edge of a free running write clock while a write enable control pin is asserted. The output data is available after each rising edge of a free running read clock while a read enable and output enable control pins are asserted. When output enable (/OE) is LOW, the data output bus is active. If /OE is HIGH, the output data bus will be in a high-impedance. This signal can control whether the data is going to be skipped during the read operation.

The FIFO Full/Empty and programmable Almost Full/Almost Empty flags are functions that can help controlling software to manipulate the FIFO more easily or to do retransmit operation. And the Retransmit function allows data to be reread from the FIFO more than once.

These chips are available as a 32pin TQFP Package