

DESCRIPTION

The Accutek AK5816384 high density memory module is a CMOS DRAM organized in 16 Meg x 8 bit words. The assembly consists of eight 16 Meg x 1 DRAMs in plastic SOJ packages mounted to the front side of a printed circuit board in 30 pad SIM (leadless) or SIP (leaded) configuration. The module is only 0.8 inch high (same height as standard 1 Meg modules), making it ideally suited for applications with low height restrictions.

The operation of the AK5816384 is identical to eight 16 Meg x 1 DRAMs. The data input is tied to the data output and brought out separately for each device, with common RAS, CAS and WE control. This common I/O feature dictates the use of early-write cycles to prevent contention of D and Q. Since the Write-Enable (WE) signal must always go low before CAS in a write cycle, Read-Write and Read-Modify-Write operation is not possible.

FEATURES

- 16,777,216 x 8 bit organization
- Optional 30 Pad leadless SIM (Single In-Line Module) or 30 Pin leaded SIP (Single In-Line Package)
- · JEDEC standard pinout
- Each device (data bit) has common DQ lines with common CAS and RAS controls
- CAS-before-RAS refresh
- Downward compatible with AK584096, AK581024/481024, AK58256/48256
- TTL-Compatible Inputs and Outputs
- RAS-Only Refresh

PIN NOMENCLATURE

| DQ ₁ - DQ ₈ | Data In/Data Out |
|-----------------------------------|-----------------------|
| A ₀ - A ₁₁ | Address Inputs |
| CAS | Column Address Strobe |
| RAS | Row Address Strobe |
| WE | Write Enable |
| Vcc | 5v Supply |
| Vss | Ground |
| NC | No Connect |
| | |

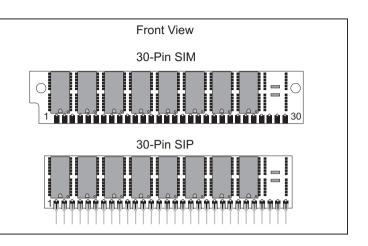
MODULE OPTIONS

| Leadless SIM: AK5816384S |
|--------------------------|
| Leaded SIP: AK5816384G |
| |

PIN ASSIGNMENT

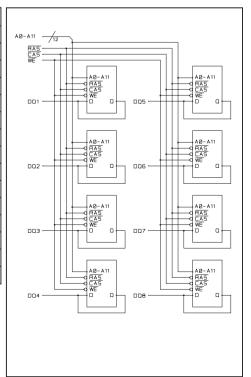
| | PIN # | SYMBOL | PIN # | SYMBOL |
|---|-------|--------|-------|--------|
| | 1 | Vcc | 16 | DQ5 |
| | 2 | CAS | 17 | A8 |
| е | 3 | DQ1 | 18 | A9 |
| | 4 | A0 | 19 | A10 |
| | 5 | A1 | 20 | DQ6 |
| | 6 | DQ2 | 21 | WE |
| | 7 | A2 | 22 | Vss |
| | 8 | A3 | 23 | DQ7 |
| | 9 | Vss | 24 | A11 |
| | 10 | DQ3 | 25 | DQ8 |
| | 11 | A4 | 26 | NC |
| | 12 | A5 | 27 | RAS |
| _ | 13 | DQ4 | 28 | NC |
| | 14 | A6 | 29 | NC |
| | 15 | A7 | 30 | Vcc |
| | | | | |

AK5816384S / AK5816384G 16,777,216 Word by 8 Bit CMOS Dynamic Random Access Memory



- 4096 Cycle Refresh every 64mSEC
- Power: 3.96 Watt Max Active (60 nS) 4.40 Watt Max Active (70 nS) 3.52 Watt Max Active (80 nS) 44 mWatt Max Standby
- Operating free air temperature 0°C to 70°C
- Fast Page Mode
- 9 Bit version (with parity bit) also available

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

| Po | ART NUMBER CODING INTERPRETATIONsition1234567 |
|--------|--|
| 1 | Product |
| | AK = Accutek Memory |
| 2 | Туре |
| | 4 = Dynamic RAM 5 = CMOS Dynamic RAM |
| | 6 = Static RAM |
| 3 | Organization/Word Width |
| | 1 = by 1 $16 = by 16$ |
| | 4 = by 4 32 = by 32 8 = by 8 36 = by 36 |
| | 9 = by 9 |
| 4 | Size/Bits Depth |
| | 64 = 64K 4096 = 4 MEG 256 = 256K 8192 = 8 MEG |
| | 1024 = 1 MEG 16384 = 16 MEG |
| 5 | Package Type |
| | G = Single In-Line Package (SIP) |
| | S = Single In-Line Module (SIM) D = Dual In-Line Package (DIP) W = .050 inch Pitch Edge Connect Z = Zig-Zag In-Line Package (ZIP) |
| 6 | D = Dual In-Line Package (DIP) |
| 6 | D = Dual In-Line Package (DIP) W = .050 inch Pitch Edge Connect Z = Zig-Zag In-Line Package (ZIP) Special Designation P = Page Mode |
| 6 | D = Dual In-Line Package (DIP) W = .050 inch Pitch Edge Connect Z = Zig-Zag In-Line Package (ZIP) Special Designation P = Page Mode N = Nibble Mode |
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| | D = Dual In-Line Package (DIP) W = .050 inch Pitch Edge Connect Z = Zig-Zag In-Line Package (ZIP) Special Designation P = Page Mode N = Nibble Mode K = Static Column Mode W = Write Per Bit Mode V = Video Ram Separator |
| 6 7 | D = Dual In-Line Package (DIP) W = .050 inch Pitch Edge Connect Z = Zig-Zag In-Line Package (ZIP) Special Designation P = Page Mode N = Nibble Mode K = Static Column Mode W = Write Per Bit Mode V = Video Ram Separator - = Commercial 0 ⁰ C to +70 ⁰ C M = Military Equivalent Screened |
| | D = Dual In-Line Package (DIP) W = .050 inch Pitch Edge Connect Z = Zig-Zag In-Line Package (ZIP) Special Designation P = Page Mode N = Nibble Mode K = Static Column Mode W = Write Per Bit Mode V = Video Ram Separator - = Commercial 0 ⁰ C to +70 ⁰ C M = Military Equivalent Screened (-55 ⁰ C to +125 ⁰ C) |
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| | D = Dual In-Line Package (DIP) W = .050 inch Pitch Edge Connect Z = Zig-Zag In-Line Package (ZIP) Special Designation P = Page Mode N = Nibble Mode K = Static Column Mode W = Write Per Bit Mode V = Video Ram Separator - = Commercial 0 ⁰ C to +70 ⁰ C M = Military Equivalent Screened (-55 ⁰ C to +125 ⁰ C) I = Industrial Temperature Tested (-45 ⁰ C to +85 ⁰ C) X = Burned In Speed (first two significant digits) |
| 7 | D = Dual In-Line Package (DIP) W = .050 inch Pitch Edge Connect Z = Zig-Zag In-Line Package (ZIP) Special Designation P = Page Mode N = Nibble Mode K = Static Column Mode W = Write Per Bit Mode V = Video Ram Separator - = Commercial 0 ⁰ C to +70 ⁰ C M = Military Equivalent Screened (-55 ⁰ C to +125 ⁰ C) I = Industrial Temperature Tested (-45 ⁰ C to +85 ⁰ C) X = Burned In |

The numbers and coding on this page do not include all variations available but are shown as examples of the most widely used variations. Contact Accutek if other information is required.

EXAMPLES:

AK5816384SP-70

16 Meg x 8, 70 nSEC, Leadless SIM, Fast Page Mode

AK5816384GP-60

16 Meg x 8, 60 nSEC, Leaded SIP, Fast Page Mode

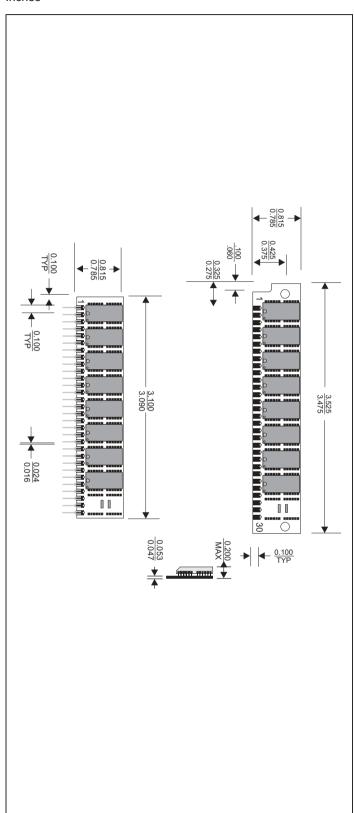


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MECHANICAL DIMENSIONS





Accutek reserves the right to make changes in specifications at any time and without notice. Accutek does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied. Preliminary data sheets contain minimum and maximum limits based upon design objectives, which are subject to change upon full characterization over the specific operating conditions.