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SEMICONDUTORES LTDA.

A3L:250DT.XXH

VOLTAGE RATINGS

Part Number	V_{RRM} , VR (V) Max. rep. peak reverse voltage		V_{RSM} , V_R (V) Max. non-rep. peak reverse voltage
	T_J = 0 to 125°C	T_J = -40 to 0°C	T_J = 25 to 125°C
A3L:250TD.02H	200	200	300
A3L:250TD.04H	400	400	500
A3L:250TD.06H	600	600	700
A3L:250TD.08H	800	800	900
A3L:250TD.10H	1000	1000	1100
A3L:250TD.12H	1200	1200	1300
A3L:250TD.14H	1400	1330	1500
A3L:250TD.16H	1600	1520	1700

MAXIMUM ALLOWABLE RATINGS

PARAMETER	VALUE	UNITS	NOTES
T_J Junction Temperature	-40 to 125	°C	-
T_{stg} Storage Temperature	-40 to 150	°C	-
$I_{F(AV)}$ Max. Av. current	250	A	180° half sine wave
$I_{F(AV)}$ @ Max. T_C	85	°C	180° half sine wave
$I_{F(RMS)}$ Nom. RMS current	555	A	-
I_{FSM} Max. Peak non-rep. surge current	7.16	kA	50 Hz half cycle sine wave; Initial T_J = 125°C, rated V_{RRM} applied after surge.
	7.81		60 Hz half cycle sine wave; Initial T_J = 125°C, rated V_{RRM} applied after surge.
	8.17		50 Hz half cycle sine wave; Initial T_J = 125°C, no voltage applied after surge.
	8.9		60 Hz half cycle sine wave; Initial T_J = 125°C, no voltage applied after surge.
I^2t Max. I^2t capability	265	kA^2s	t = 10ms; Initial T_J = 125°C, rated V_{RRM} applied after surge.
	289		t = 8.3 ms; Initial T_J = 125°C, rated V_{RRM} applied after surge.
	302		t = 10ms; Initial T_J = 125°C, no voltage applied after surge.
	329		t = 8.3 ms; Initial T_J = 125°C, no voltage applied after surge.
$I^2t^{1/2}$ Max. $I^2t^{1/2}$ capability	3610	$kA^2s^{1/2}$	Initial T_J = 125°C, no voltage applied after surge. I^2t for time $t_x = I^2t^{1/2} * t_x^{1/2}$. (0.1 < tx < 10ms).
di/dt Max. Non-repetitive rate-of-rise current	500	A/µs	T_J = 125°C, $V_D = V_{DRM}$, I_{TM} = 1600A. Gate pulse: 20V, 20Ω, 10µs, 0.5µs rise time, Max. repetitive di/dt is aproximately 40% of non-repetitive value.
P_GM Max. Peak gate power	10	W	tp < 5 ms
$P_{G(AV)}$ Max. Av. gate power	3	W	-
$+I_{GM}$ Max. Peak gate current	150	mA	tp < 5 ms
$-V_{GM}$ Max. Peak negative gate voltage	2	V	-
F Mounting Force	3(5)	N.m	Upper connectors(Heatsink)

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CHARACTERISTICS

PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{TM} peak on-state voltage	---	---	1.37	V	Initial T_J = 25℃, 50-60Hz half sine, I_{peak} = 785A.
$V_{T(TO)}$ Threshold voltage	---	---	0.89	V	T_J = 125℃ Av. power = $V_{T(TO)}$ * $I_{T(AV)}$ +r_T * $[I_{T(RMS)}]^2$, 180 Half Sine.
r_T Slope resistance	---	---	0.61	mΩ	Use low values for I_{TM} < π rated $I_{T(AV)}$
I_L Latching current	---	---	200	mA	T_C = 125°C, 12V anode. Gate pulse: 10V, 20Ω, 100μs.
I_H Holding current	---	---	500	mA	T_C = 25℃, 12V anode. Initial I_T = 15A.
t_d Delay time	---	0.7	1.5	μs	T_C = 25℃, V_D = V_{DRM}, 50A resistive load. Gate pulse: 10V, 20Ω, 10μs, 1μs rise time.
t_q Turn-off time	---	125	200	μs	T_J = 125℃, I_{TM} = 500A, di/dt = 25A/μs, V_R = 50V. dv/dt = 20 V/μs lin. to rated V_{DRM}. Gate: 0V, 100Ω.
dv/dt Critical rate-of-rise of off-state voltage	80	140	---	V/μs	T_J = 125℃. Exp. to 100% or lin. To 80% V_{DRM}, gate open. Higher dv/dt values avaliable.
	---	---	1000		T_J = 125℃, Exp. To 67% V_{DRM}, gate open.
I_{RM}, I_{DM} Peak reverse and off-state current	---	10	50	mA	T_J = 125℃, Rated V_{RRM} and V_{DRM}, gate open.
I_{GT} DC gate current to trigger	---	---	300	mA	T_C = -40℃
	50	80	150		T_C = 25℃ +12V anode-to-cathode. For recommended gate drive see "Gate Characteristics" figure.
V_{GT} DC gate voltage to trigger	4	---	---	V	T_C = -40℃
	2	---	2.5		T_C = 25℃
V_{GD} DC gate voltage not to trigger	---	---	0.3	V	T_C = 25℃, Max. Value which will not trigger with rated V_{DRM} anode.
R_{thJC} Thermal resistance, junction-to-case	---	---	0.07	℃/W	DC operation, single side cooled.
	---	---	0.071	℃/W	180 sine wave, single side cooled.
	---	---	0.075	℃/W	120 rectangular wave, single side cooled.
R_{thCS} Thermal resistance, case-to-sink	---	---	0.02	℃/W	Mtg. Surface smooth, flat and greased. Single side cooled.
wt Weight	---	500(18)	---	g(oz.)	---

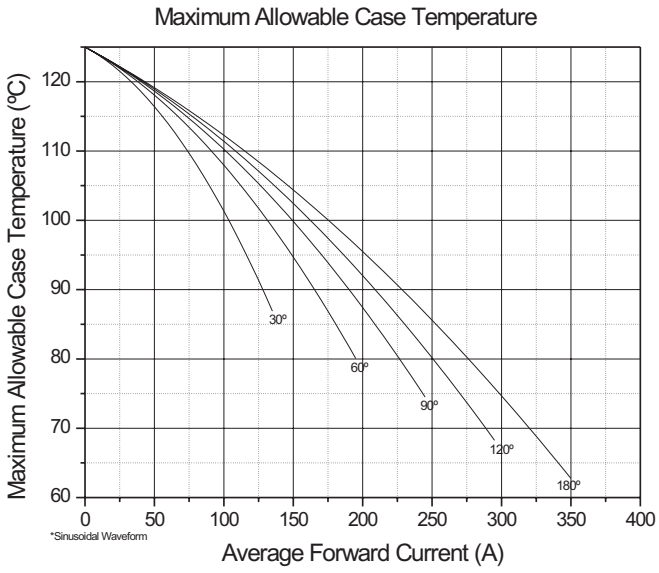

Fig. 1 - Current Ratings Characteristics

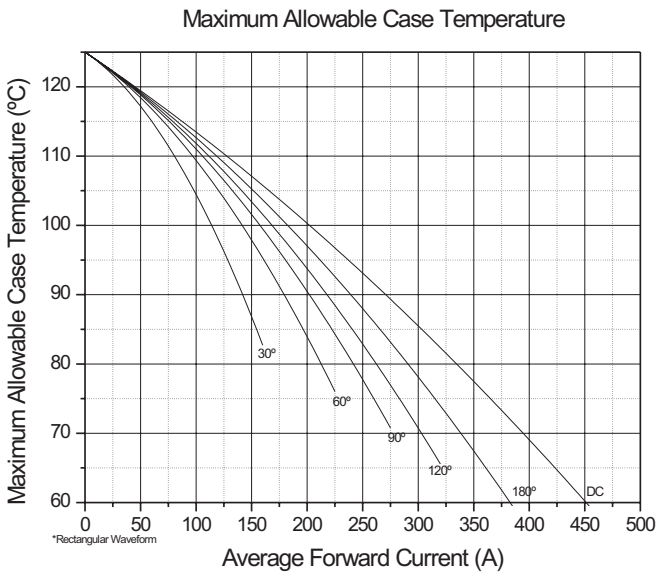

Fig. 2 - Current Ratings Characteristics

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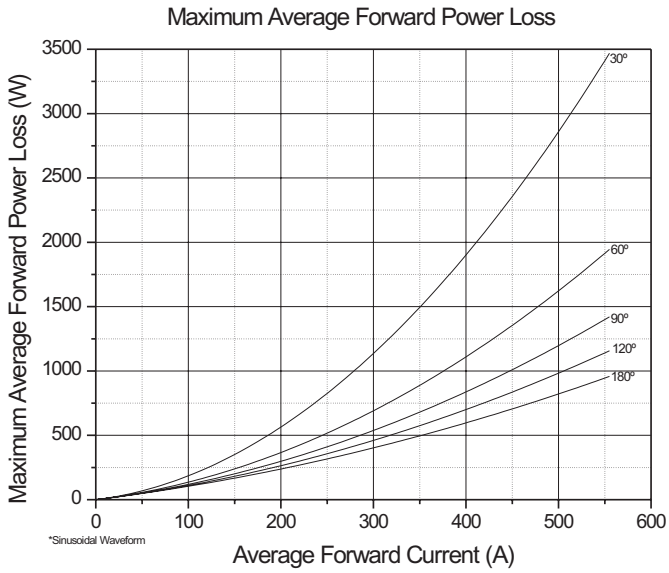

Fig.3 -Forward Power Loss Characteristics

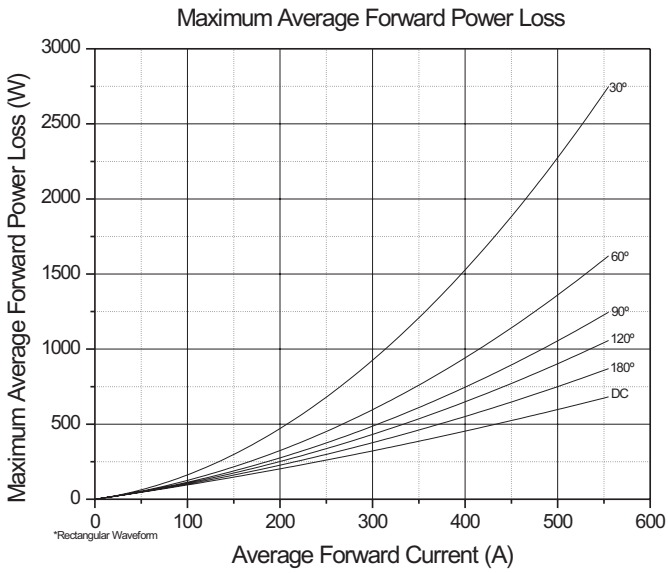

Fig. 4 - Forward Power Loss Characteristics

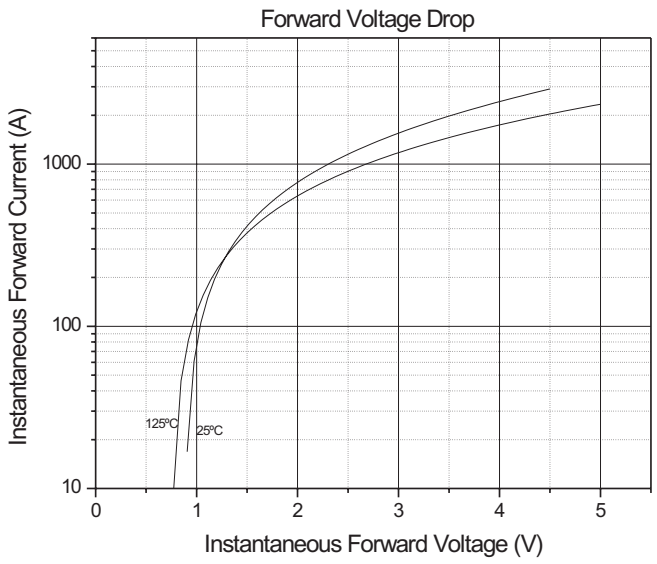

Fig. 5 - Forward Voltage Drop Characteristics

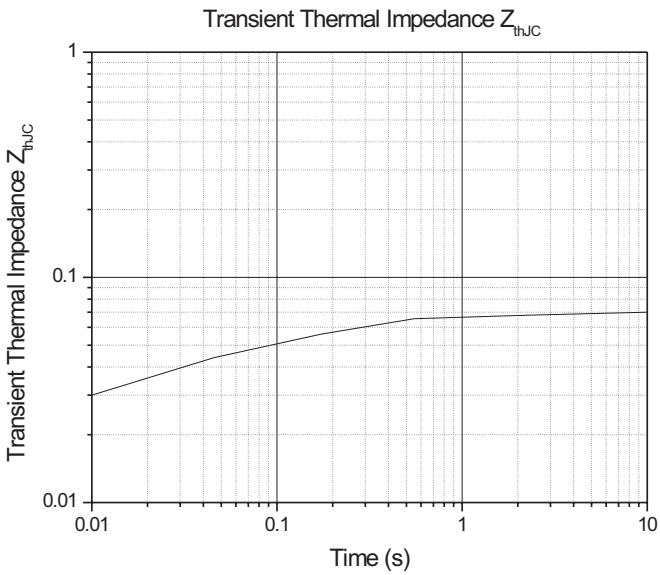

Fig. 6 - Transient Thermal Impedance

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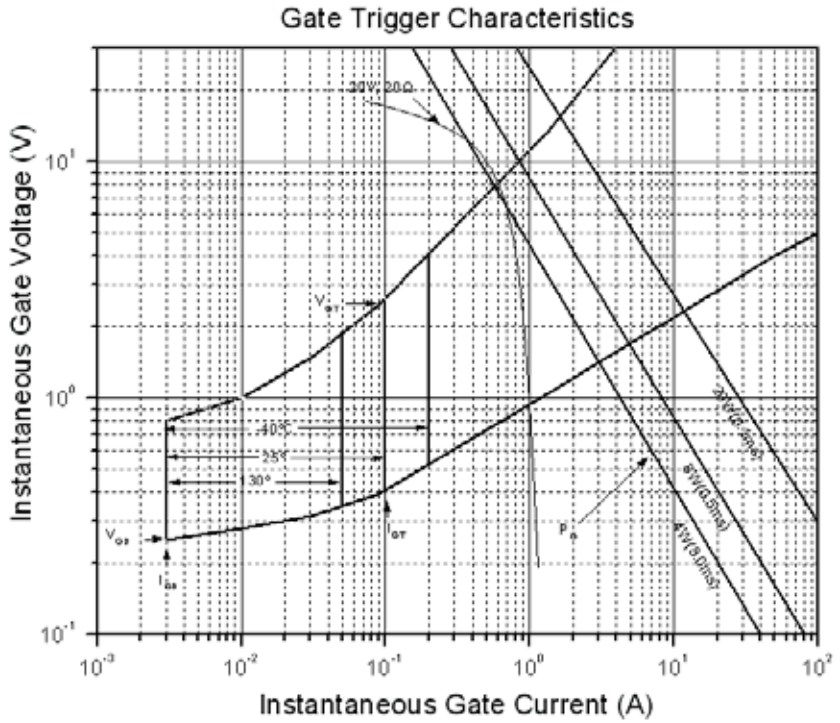

Fig. 7 - Gate Trigger Characteristics

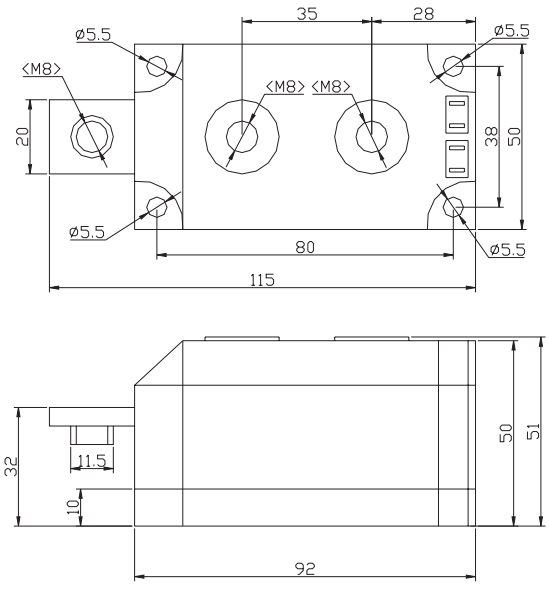

Fig. 8 - Outline Characteristics

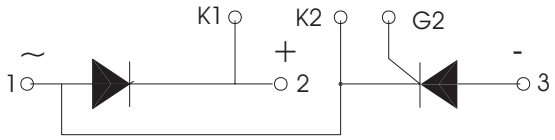

Fig. 9 - Circuit Layout