AMIS-42670 High-Speed CAN Transceiver
For Long Networks

Data Sheet

1.0 General Description

The AMIS-42670 CAN transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus and may be used in both 12V and 24V systems. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller. Due to the wide common-mode voltage range of the receiver inputs, the AMIS-42670 is able to reach outstanding levels of electromagnetic susceptibility (EMS). Similarly, extremely low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

The AMIS-42670 is the industrial version of the AMIS-30660 and primarily intended for applications where long network lengths are mandatory. Examples are elevators, in-building networks, process control and trains. To cope with the long bus delay the communication speed needs to be low. AMIS-42670 allows low transmit data rates down 10 Kbit/s or lower.

2.0 Key Features

- Fully compatible with the ISO 11898-2 standard
- Certified "Authentication on CAN Transceiver Conformance (d1.1)"
- Wide range of bus communication speed (0 up to 1 Mbit/s)
- Allows low transmit data rate in networks exceeding 1 km
- Ideally suited for 12V and 24V industrial and automotive applications
- Low electromagnetic emission (EME) common-mode choke is no longer required
- Differential receiver with wide common-mode range (+/- 35V) for high EMS
- No disturbance of the bus lines with an un-powered node
- Thermal protection
- Bus pins protected against transients
- Silent mode in which the transmitter is disabled
- Short circuit proof to supply voltage and ground
- Logic level inputs compatible with 3.3V devices

3.0 Technical Characteristics

Table 1: Technical Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CANH}	DC voltage at pin CANH	$0 < V_{CC} < 5.25V$; no time limit	-45	+45	V
V_{CANL}	DC voltage at pin CANL	$0 < V_{CC} < 5.25V$; no time limit	-45	+45	V
$V_{i(dif)(bus\_dom)}$	Differential bus output voltage in dominant state	$42.5\Omega < R_{LT} < 60\Omega$	1.5	3	V
$t_{pd(rec-dom)}$	Propagation delay TxD to RxD	See Figure 7	70	245	ns
$t_{pd(dom-rec)}$	Propagation delay TxD to RxD	See Figure 7	100	245	ns
$C_{M-range}$	Input common-mode range for comparator	Guaranteed differential receiver threshold and leakage current	-35	+35	V
$V_{CM-peak}$	Common-mode peak	See Figures 8 and 9 (Notes)	-500	500	mV
$V_{CM-step}$	Common-mode step	See Figures 8 and 9 (Notes)	-150	150	mV

Note: The parameters $V_{CM-peak}$ and $V_{CM-step}$ guarantee low electromagnetic emission.

4.0 Ordering Information

Ordering Code (Tubes)	Ordering Code (Tape)	Marketing Name	Package	Temp. Range
0ICAH-002-XTD	0ICAH-002-XTP	AMIS 42670NGA	SOIC-8 GREEN	-40°C…125°C

5.0 Block Diagram

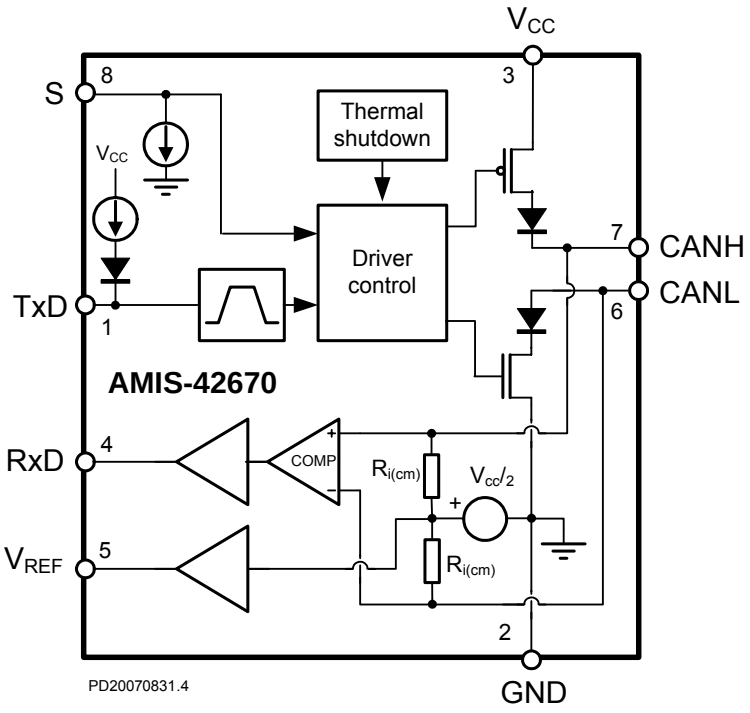


Figure 1: Block Diagram

6.0 Typical Application

6.1 Application Schematic

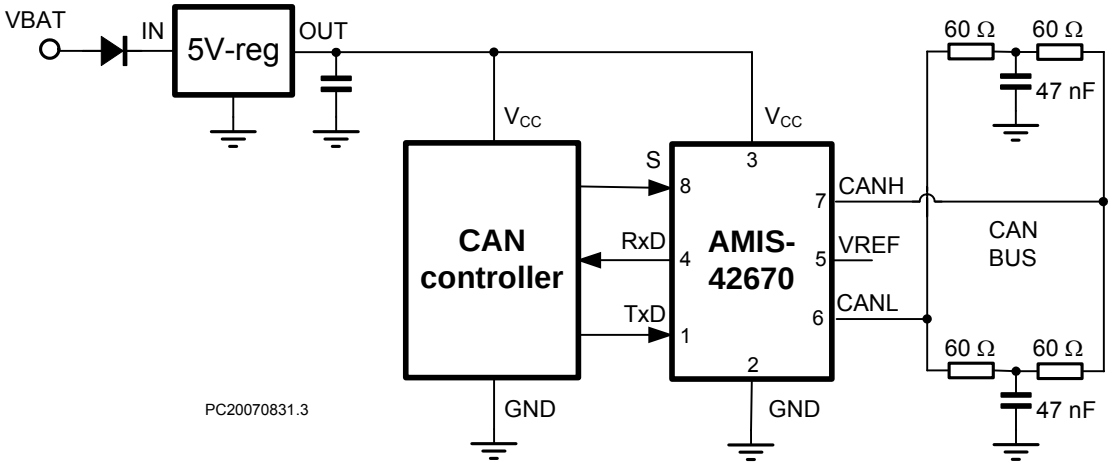


Figure 2: Application Diagram

6.2 Pin Description

6.2.1. Pin Out (Top View)

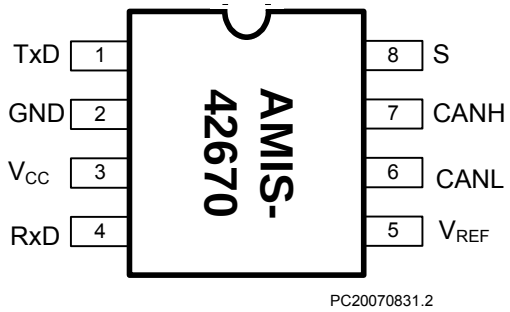


Figure 3: Pin Configuration

6.3 Pin Description

Table 2: Pin Out

Pin	Name	Description
1	TxD	Transmit data input; low input → dominant driver; internal pull-up current
2	GND	Ground
3	V_{CC}	Supply voltage
4	RxD	Receive data output; dominant transmitter → low output
5	V_{REF}	Reference voltage output
6	CANL	Low-level CAN bus line (low in dominant mode)
7	CANH	High-level CAN bus line (high in dominant mode)
8	S	Silent mode control input; internal pull-down current

7.0 Functional Description

7.1 Operating Modes

The behavior of AMIS-42670 under various conditions is illustrated in Table 3 below. In case the device is powered, one of two operating modes can be selected through pin S.

Table 3: Functional table of AMIS-42670; X = don't care

VCC	pin TxD	pin S	pin CANH	pin CANL	Bus state	pin RxD
4.75 to 5.25.V	0	0 (or floating)	High	Low	Dominant	0
4.75 to 5.25.V	X	1	VCC/2	VCC/2	Recessive	1
4.75 to 5.25.V	1 (or floating)	X	VCC/2	VCC/2	Recessive	1
VCC<PORL (unpowered)	X	X	0V<CANH<VCC	0V<CANL<VCC	Recessive	1
PORL<VCC<4.75V	>2V	X	0V<CANH<VCC	0V<CANL<VCC	Recessive	1

7.1.1. High-Speed Mode

If pin S is pulled low (or left floating), the transceiver is in its high-speed mode and is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD. The slopes on the bus line outputs are optimized to give extremely low electromagnetic emissions.

7.1.2. Silent Mode

In silent mode, the transmitter is disabled. All other IC functions continue to operate. The silent mode is selected by connecting pin S to VCC and can be used to prevent network communication from being blocked, due to a CAN controller which is out of control.

7.2 Over-temperature Detection

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 160°C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off-state resets when pin TxD goes high. The thermal protection circuit is particularly necessary when a bus line short-circuits.

7.3 High Communication Speed Range

The transceiver is primarily intended for industrial applications. It allows very low baud rates needed for long bus length applications. But also high speed communication is possible up to 1Mbit/s.

7.4 Fail-safe Features

A current-limiting circuit protects the transmitter output stage from damage caused by an accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

The pins CANH and CANL are protected from automotive electrical transients (according to "ISO 7637"; see Figure 4). Pin TxD is pulled high internally should the input become disconnected.

8.0 Electrical Characteristics

8.1 Definitions

All voltages are referenced to GND (pin 2). Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

8.2 Absolute Maximum Ratings

Stresses above those listed in the following table may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage		-0.3	+7	V
V_{CANH}	DC voltage at pin CANH	$0 < V_{CC} < 5.25V$; no time limit	-45	+45	V
V_{CANL}	DC voltage at pin CANL	$0 < V_{CC} < 5.25V$; no time limit	-45	+45	V
V_{TxD}	DC voltage at pin TxD		-0.3	V_{CC} + 0.3	V
V_{RxD}	DC voltage at pin RxD		-0.3	V_{CC} + 0.3	V
V_S	DC voltage at pin S		-0.3	V_{CC} + 0.3	V
V_{REF}	DC voltage at pin V_{REF}		-0.3	V_{CC} + 0.3	V
$V_{tran(CANH)}$	Transient voltage at pin CANH	Note 1	-150	+150	V
$V_{tran(CANL)}$	Transient voltage at pin CANL	Note 1	-150	+150	V
V_{esd}	Electrostatic discharge voltage at all pins	Note 2 Note 4	-4 -750	+4 +750	kV V
Latch-up	Static latch-up at all pins	Note 3		100	mA
T_{stg}	Storage temperature		-55	+155	°C
T_{amb}	Ambient temperature		-40	+125	°C
T_{junc}	Maximum junction temperature		-40	+150	°C

Notes:
1. Applied transient waveforms in accordance with ISO 7637 part 3, test pulses 1, 2, 3a, and 3b (see Figure 4).
2. Standardized human body model ESD pulses in accordance to MIL883 method 3015.7.
3. Static latch-up immunity: static latch-up protection level when tested according to EIA/JESD78.
4. Standardized charged device model ESD pulses when tested according to EOS/ESD DS5.3-1993.

8.3 Thermal Characteristics

Table 5: Thermal Characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(vj-a)}$	Thermal resistance from junction to ambient in SO8 package	In free air	150	K/W
$R_{th(vj-s)}$	Thermal resistance from junction to substrate of bare die	In free air	45	K/W

8.4 DC and Timing Characteristics

V_{CC} = 4.75 to 5.25V; T_{junc} = -40 to +150°C; R_{LT} =60Ω unless specified otherwise.

Table 6: DC and Timing Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply (Pin V_{CC})						
I_{CC}	Supply current	Dominant; V_{TXD} = 0V Recessive; V_{TXD} = V_{CC}	25 2	45 4	65 8	mA mA
Transmitter Data Input (Pin TxD)						
V_{IH}	High-level input voltage	Output recessive	2.0	-	V_{CC}+0.3	V
V_{IL}	Low-level input voltage	Output dominant	-0.3	-	+0.8	V
I_{IH}	High-level input current	V_{TxD} = V_{CC}	-1	0	+1	µA
I_{IL}	Low-level input current	V_{TxD} = 0V	-75	-200	-350	µA
C_i	Input capacitance	Not tested	-	5	10	pF
Mode Select (Pin S)						
V_{IH}	High-level input voltage	Silent mode	2.0	-	V_{CC}+0.3	V
V_{IL}	Low-level input voltage	High-speed mode	-0.3	-	+0.8	V
I_{IH}	High-level input current	V_S =2V	20	30	50	µA
I_{IL}	Low-level input current	V_S =0.8V	15	30	45	µA
Receiver Data Output (Pin RxD)						
V_{OH}	High-level output voltage	I_{RXD} = - 10mA	0.6 x V_{CC}	0.75 x V_{CC}		V
V_{OL}	Low-level output voltage	I_{RXD} = 6mA		0.25	0.45	V
Reference Voltage Output (Pin V_{REF})						
V_{REF}	Reference output voltage	-50µA < I_{VREF} < +50µA	0.45 x V_{CC}	0.50 x V_{CC}	0.55 x V_{CC}	V
V_{REF_CM}	Reference output voltage for full common mode range	-35V <V_{CANH}< +35V; -35V <V_{CANL}< +35V	0.40 x V_{CC}	0.50 x V_{CC}	0.60 x V_{CC}	V
Bus Lines (Pins CANH and CANL)						
$V_{o(reces)(CANH)}$	Recessive bus voltage at pin CANH	V_{TxD} = V_{CC}; no load	2.0	2.5	3.0	V
$V_{o(reces)(CANL)}$	Recessive bus voltage at pin CANL	V_{TxD} = V_{CC}; no load	2.0	2.5	3.0	V
$I_{o(reces)\ (CANH)}$	Recessive output current at pin CANH	-35V <V_{CANH}< +35V; 0V <V_{CC} < 5.25V	-2.5	-	+2.5	mA
$I_{o(reces)\ (CANL)}$	Recessive output current at pin CANL	-35V <V_{CANL} < +35V; 0V <V_{CC} < 5.25V	-2.5	-	+2.5	mA
$V_{o(dom)\ (CANH)}$	Dominant output voltage at pin CANH	V_{TxD} = 0V	3.0	3.6	4.25	V
$V_{o(dom)\ (CANL)}$	Dominant output voltage at pin CANL	V_{TxD} = 0V	0. 5	1.4	1.75	V
$V_{i(dif)\ (bus)}$	Differential bus input voltage (V_{CANH} - V_{CANL})	V_{TxD} = 0V; dominant; 42.5 Ω < R_{LT} < 60 Ω	1.5	2.25	3.0	V
		V_{TxD} =V_{CC}; recessive; No load	-120	0	+50	mV
$I_{o(sc)\ (CANH)}$	Short circuit output current at pin CANH	V_{CANH} = 0V; V_{TxD} = 0V	-45	-70	-95	mA
$I_{o(sc)\ (CANL)}$	Short circuit output current at pin CANL	V_{CANL} = 36V; V_{TxD} = 0V	45	70	120	mA
$V_{i(dif)(th)}$	Differential receiver threshold voltage	-5V <V_{CANL} < +10V; -5V <V_{CANH} < +10V; See Figure 5	0.5	0.7	0.9	V
$V_{ihcm(dif)\ (th)}$	Differential receiver threshold voltage for high common-mode	-35V <V_{CANL} < +35V; -35V <V_{CANH} < +35V; See Figure 5	0.25	0.7	1.05	V
$V_{i(dif)\ (hys)}$	Differential receiver input voltage hysteresis	-5V <V_{CANL} < +10V; -5V <V_{CANH} < +10V; See Figure 5	50	70	100	mV
$R_{i(cm)(CANH)}$	Common-mode input resistance at pin CANH		15	25	37	KΩ
$R_{i(cm)\ (CANL)}$	Common-mode input resistance at pin CANL		15	25	37	KΩ
$R_{i(cm)(m)}$	Matching between pin CANH and pin CANL common-mode input resistance	V_{CANH} =V_{CANL}	-3	0	+3	%
$R_{i(dif)}$	Differential input resistance		25	50	75	KΩ
$R_{i(cm)(m)}$	Matching between pin CANH and pin CANL common-mode input resistance	V_{CANH} =V_{CANL}	-3	0	+3	%
$R_{i(dif)}$	Differential input resistance		25	50	75	KΩ

Table 7: DC and Timing Characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$C_{i(CANH)}$	Input capacitance at pin CANH	V_{TxD} = V_{CC}; not tested		7.5	20	pF
$C_{i(CANL)}$	Input capacitance at pin CANL	V_{TxD} = V_{CC}; not tested		7.5	20	pF
$C_{i(dif)}$	Differential input capacitance	V_{TxD} = V_{CC}; not tested		3.75	10	pF
$I_{LI(CANH)}$	Input leakage current at pin CANH	V_{CC} = 0V; V_{CANH} = 5V	10	170	250	µA
$I_{LI(CANL)}$	Input leakage current at pin CANL	V_{CC} = 0V; V_{CANL} = 5V	10	170	250	µA
$V_{CM-peak}$	Common-mode peak during transition from dom → rec or rec → dom	See Figure 8 and Figure 9	-500		500	mV
$V_{CM-step}$	Difference in common-mode between dominant and recessive state	See Figure 8 and Figure 9	-150		150	mV
Power-on-Reset (POR)						
PORL	POR level	CANH, CANL, V_{ref} in tri-state below POR level	2.2	3.5	4.7	V
Thermal Shutdown						
$T_{i(sd)}$	Shutdown junction temperature		150	160	180	°C
Timing Characteristics (see Figure 6 and Figure 7)						
$t_{d(TxD-BUSon)}$	Delay TxD to bus active	V_s = 0V	40	85	130	ns
$t_{d(TxD-BUSoff)}$	Delay TxD to bus inactive	V_s = 0V	30	60	105	ns
$t_{d(BUSon-RxD)}$	Delay bus active to RxD	V_s = 0V	25	55	105	ns
$t_{d(BUSoff-RxD)}$	Delay bus inactive to RxD	V_s = 0V	65	100	135	ns
$t_{pd(rec-dom)}$	Propagation delay TxD to RxD from recessive to dominant	V_s = 0V	70		245	ns
$t_{d(dom-rec)}$	Propagation delay TxD to RxD from dominant to recessive	V_s = 0V	100		245	ns

8.5 Measurement Set-ups and Definitions

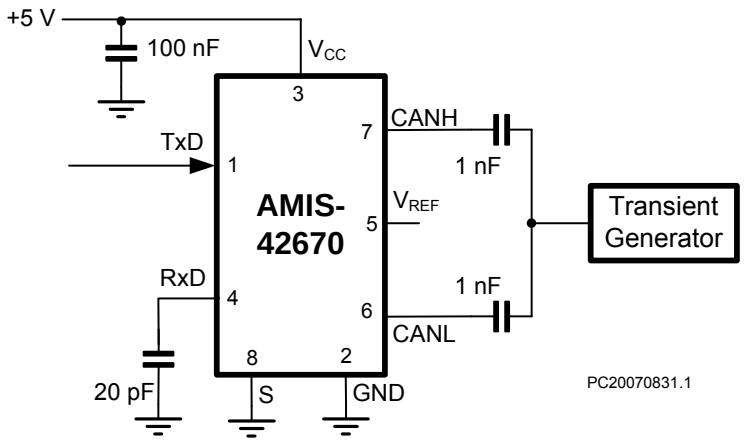


Figure 4: Test Circuit for Transients

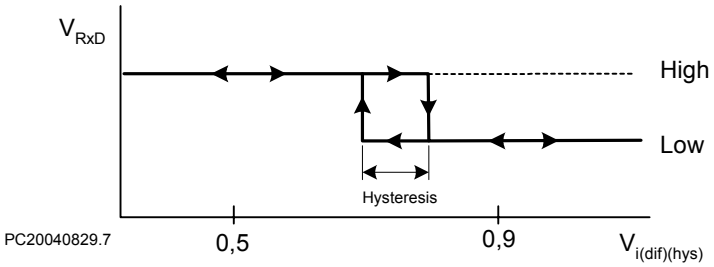


Figure 5: Hysteresis of the Receiver

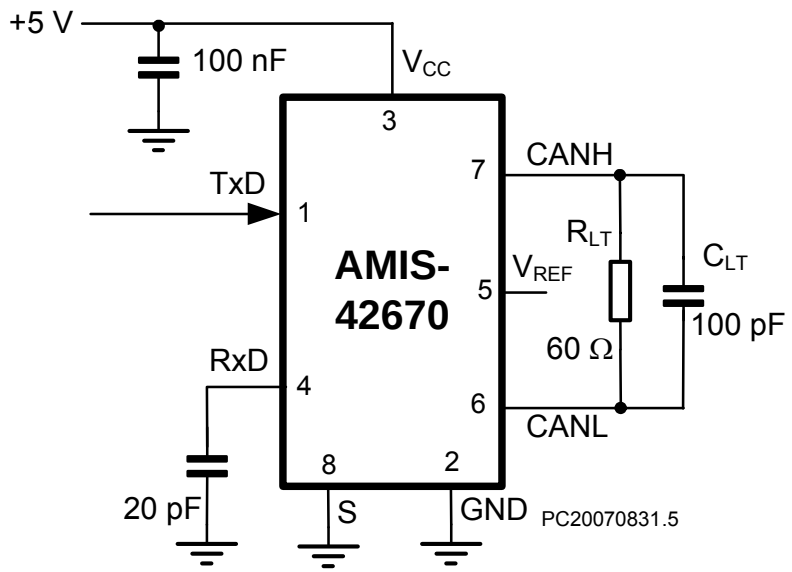


Figure 6: Test Circuit for Timing Characteristics

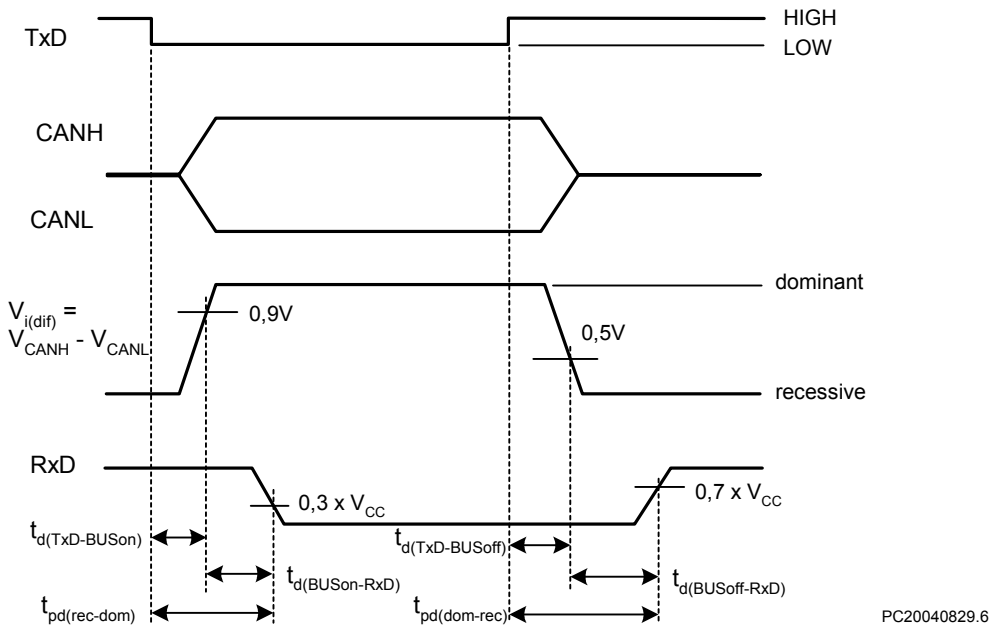


Figure 7: Timing Diagram for AC Characteristics

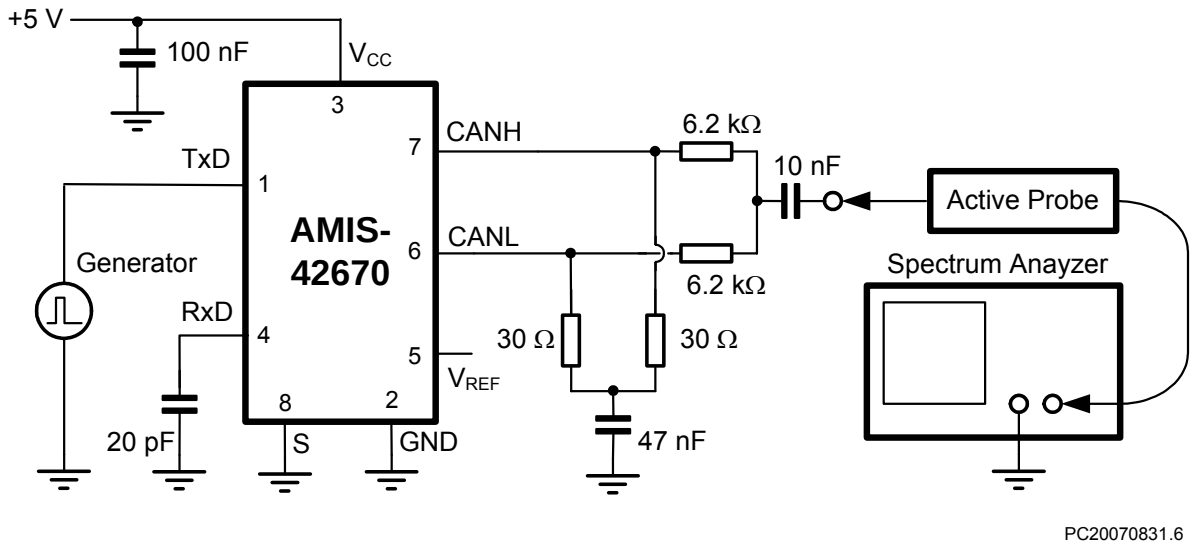


Figure 8: Basic Test Set-up for Electromagnetic Measurement

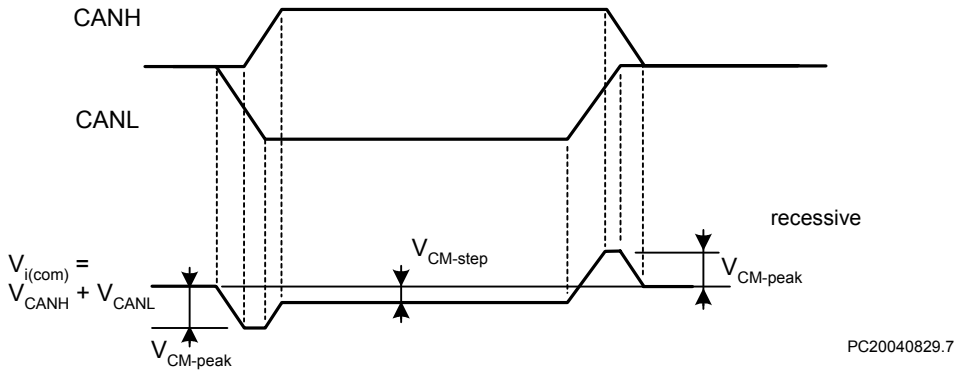
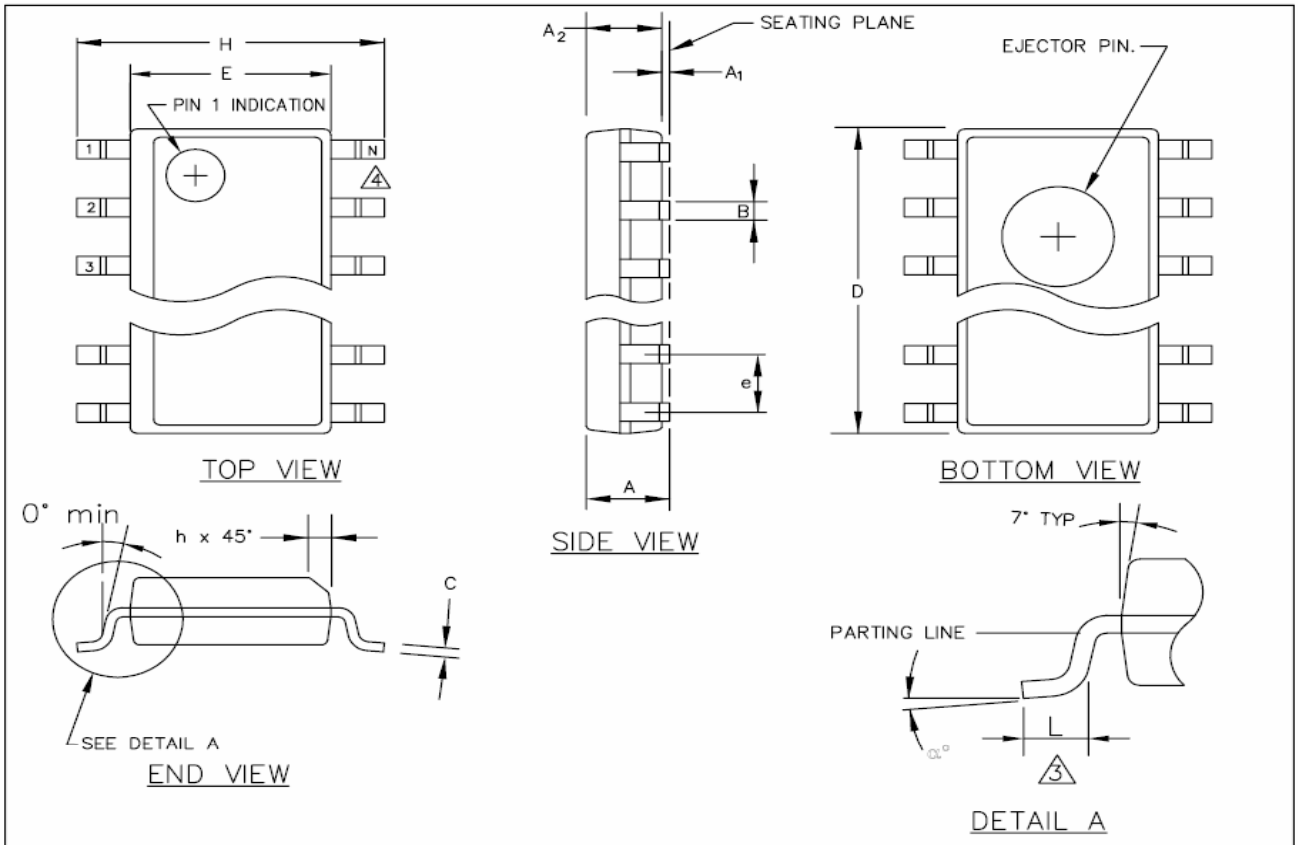


Figure 9: Common-mode Voltage Peaks (see measurement set-up Figure 8)

9.0 Package Outline

SOIC-8: Plastic small outline; eight leads; body width 150mil



SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	.061	.064	.068	
A_1	.004	.006	0.010	
A_2	.055	.058	.061	
B	.0138	.016	.020	
C	.0075	.008	.0098	
D	SEE VARIATIONS			1
E	.150	.155	.157	
e	.050 BSC			
H	.230	.236	.244	
h	.010	.013	.016	
L	.016	.025	.035	
N	SEE VARIATIONS			2
α°	0°	5°	8°	

VARIATIONS 1 D	MIN.	NOM.	MAX.	2 N
AA	.189	.194	.196	8
AB	.337	.342	.344	14
AC	.386	.391	.393	16

NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M – 1982.
3. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
4. "N" IS THE NUMBER OF TERMINAL POSITIONS.
5. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
6. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
7. CONTROLLING DIMENSION: INCHES.

Drawn: PJ 10/28/03
CAD Dwg. No. 6000209.DWG
Ref Dwg. No.

SOIC150
8, 14, 16 LEAD

AMI SEMICONDUCTOR, Inc.
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Drawing Number\CAD File: 6000209
Rev.: D
Scale:
Sheet

10.0 Soldering

10.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in the AMIS "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).
There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed circuit boards with high population densities. In these situations reflow soldering is often used.

10.2 Re-flow Soldering

Re-flow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.
Several methods exist for re-flowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds, depending on heating method.
Typical reflow peak temperatures range from 215 to 250°C. The top-surface temperature of the packages should preferably be kept below 230°C.

10.3 Wave Soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed circuit boards with a high component density, as solder bridging and non-wetting can present major problems.
To overcome these problems the double-wave soldering method was specifically developed.
If wave soldering is used, the following conditions must be observed for optimal results:

- Use a double-wave soldering method, comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
  For packages with leads on two sides and a pitch (e):
  - Larger than or equal to 1.27mm, the footprint longitudinal axis is preferred to be parallel to the transport direction of the printed-circuit board.
  - Smaller than 1.27mm, the footprint longitudinal axis must be parallel to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45 degree angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.
Typical dwell time is four seconds at 250°C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

10.4 Manual Soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to ten seconds at up to 300°C.
When using a dedicated tool, all other leads can be soldered in one operation within two to five seconds, between 270 and 320°C.

Table 8: Soldering

Package	Soldering Method	
	Wave	Reflow (1)
BGA, SQFP	Not suitable	Suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	Not suitable (2)	Suitable
PLCC (3) , SO, SOJ	Suitable	Suitable
LQFP, QFP, TQFP	Not recommended (3)(4)	Suitable
SSOP, TSSOP, VSO	Not recommended (5)	Suitable

Notes:

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods."
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heat sink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45 degree angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5mm.

11.0 Company or Product Inquiries

For more information about AMI Semiconductor's high-speed Industrial CAN transceivers, visit our Web site at: http://www.amis.com

12.0 Document History

Date	Revision	Change
October 2007	1.0	Initial release