

TC9122P

T-45-23-33

TC9122P HIGH-SPEED BCD PROGRAMMABLE COUNTER

TC9122P is high-speed programmable counter of C-MOS structure developed for PLL circuits and various frequency dividers, and is provided with the following features.

- Permits epoch-making high-speed operation for C-MOS structure.

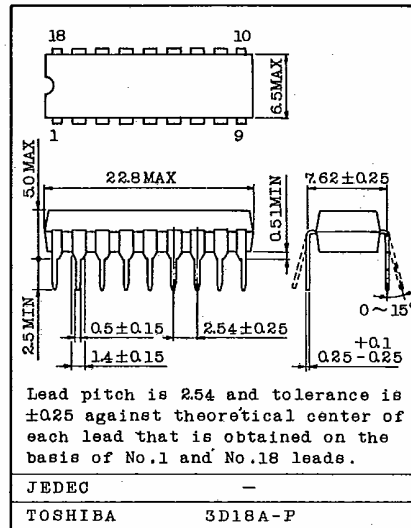
$$f_{\max} = 15\text{MHz} \quad \left(\begin{array}{l} V_{\text{DD}}=7.5\text{V} \\ T_a=-30 \sim 75^\circ\text{C} \\ V_{\text{IN}}=2.0\text{Vp-p} \end{array} \right)$$

- Program data are input by means of BCD code, allowing frequency division of 8 ~ 3999.
- Built-in self-bias type amplifier for divided frequency signal input is capable of operation by small signal in combination with capacitor.
- C-MOS structure provides wide range of operational supply voltage (4.5 ~ 8.5V) and simplification of design.

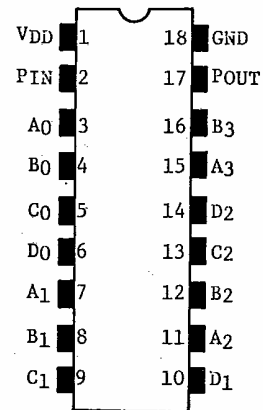
MAXIMUM RATINGS ($T_a=25^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	-0.3 ~ 10	V
Input Voltage	V _{IN}	-0.3 ~ V _{DD} +0.3	V
Operating Temp.	T _{opr}	-30 ~ 75	°C
Storage Temperature	T _{stg}	-55 ~ 125	°C

Unit in mm


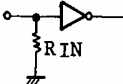


PIN CONNECTION

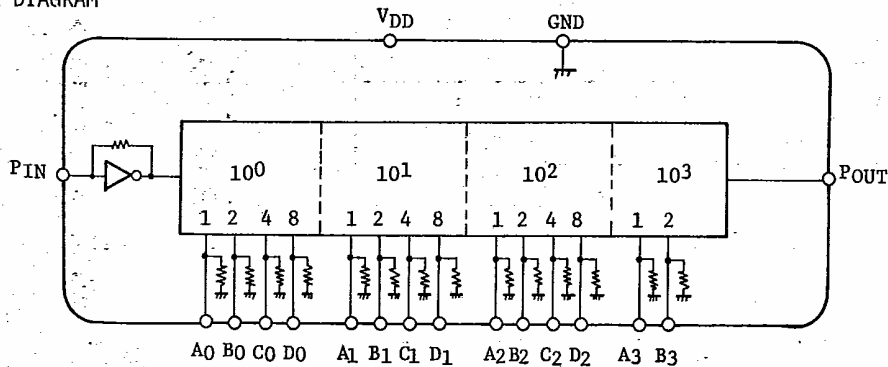


AUDIO DIGITAL IC

FUNCTIONAL DESCRIPTION OF EACH TERMINAL

PIN NO.	SYMBOL	NAME	FUNCTIONAL DESCRIPTION	REMARKS																																																																																																																
2	PIN	Programmable counter input terminal	Divided frequency signal input terminal of programmable counter. Built-in self-bias amplifier is capable of operation by small signal in combination with capacitor.	Built-in amplifier 																																																																																																																
3~16	A0 ~ D0 A1 ~ D2 A2 ~ D2 A3, B3	$\times 10^0$ $\times 10^1$ $\times 10^2$ Program input terminal $\times 10^3$	Input terminals to establish frequency division ratio N by BCD. Program data allow frequency division of 8~3999 by $3\frac{1}{2}$ -digit BCD. The following frequency division ratio combinations are inhibited. <table border="1" style="font-size: small;"> <tr> <td>A0</td><td>B0</td><td>C0</td><td>D0</td><td>A1</td><td>B1</td><td>C1</td><td>D1</td><td>A2</td><td>B2</td><td>C2</td><td>D2</td><td>A3</td><td>B3</td> </tr> <tr> <td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> <tr> <td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> <tr> <td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> <tr> <td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> <tr> <td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> <tr> <td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> <tr> <td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> </table>	A0	B0	C0	D0	A1	B1	C1	D1	A2	B2	C2	D2	A3	B3	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	Pull/down resistor contained in each terminal. 
A0	B0	C0	D0	A1	B1	C1	D1	A2	B2	C2	D2	A3	B3																																																																																																							
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17	POUT	Programmable counter output terminal	Output terminal of programmable counter. This terminal is for 1/N frequency output of PIN input frequency. Pulse width is for 5 bits of input.																																																																																																																	
1,18	VDD GND		Terminal to which supply voltage is applied.																																																																																																																	

BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS (Unless otherwise specified $T_a=25^\circ\text{C}$, $V_{DD}=7.5\text{V}$)

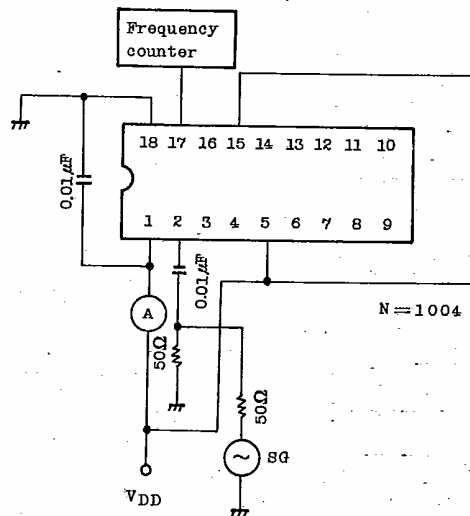
CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	V_{DD}	-	-	4.5	~	8.5	V
Operating Input Amplitude	V_{IN}	-	-	2.0	~	7.0	V _{p-p}
Operating Supply Current	I_{DD}	1	$f_{IN}=15\text{MHz}$, $V_{IN}=2.0\text{Vp-p}$	-	15	30	mA
Input Voltage	"H" Level	V_{IH}	-	5.5	-	-	V
	"L" Level	V_{IL}	-	-	-	2.0	V
Output Voltage	"H" Level	V_{OH}	$I_{OH}=-0.5\text{mA}$	6.5	-	-	V
	"L" Level	V_{OL}	$I_{OL}=0.5\text{mA}$	-	-	1.0	V
Operating Frequency Range	f_{opr}	1	(Note 1)	1	~	15	MHz
Input Pull Down Resistance	R_{IN}	-	-	20	-	80	k Ω
Amp. Feedback Resistance	R_F	-	-	100	-	500	k Ω

(Note 1) This operational frequency satisfies the specification during the following conditions.

$$V_{DD} = 7.5\text{V} \pm 10\%, \quad V_{IN} = 2.0\text{Vp-p}, \quad T_a = -30 \sim 75^\circ\text{C}$$

TEST CIRCUIT 1

I_{DD} , f_{opr}

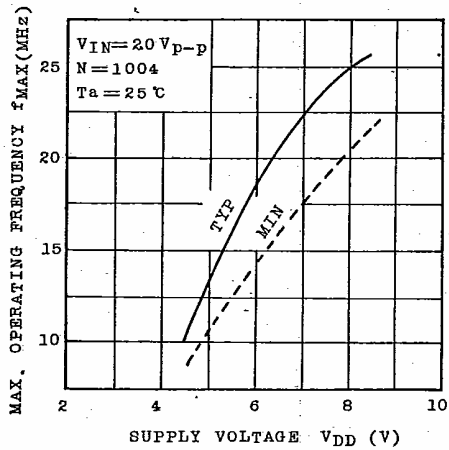


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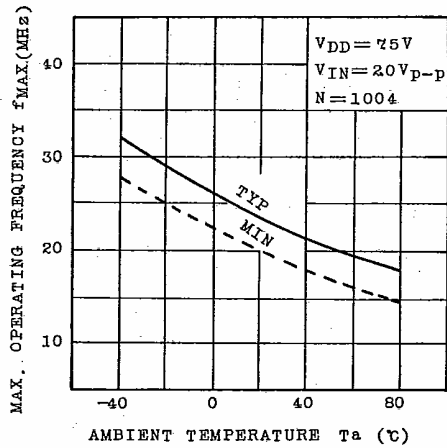
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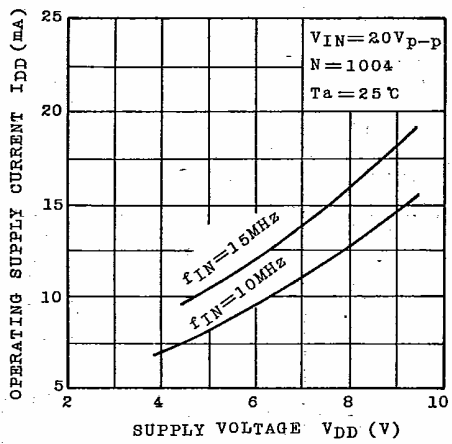
$V_{DD} - f_{MAX}$



$T_a - f_{MAX}$



$V_{DD} - I_{DD}$



TOSHIBA